

TRIACS
SILICON BIDIRECTIONAL THYRISTORS

FEATURES

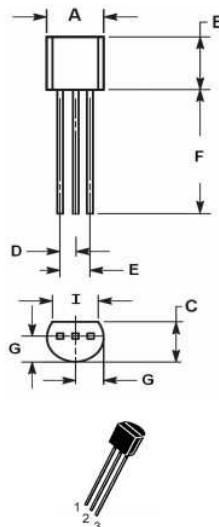
- Passivated die for reliability and uniformity
- Three-quadrant triggering Triac
- Over 800V V_{DRM}/V_{RRM}
- Low level triggering and holding characteristics
- Logic control compatible
- False turn-on voltage up 600V by dv/dt
- Qualified to AEC-Q101 Rev_C

APPLICATIONS

- General purpose motor control
- Small loads in washing machines
- Solenoid drivers
- Digital control drivers

TRIACS
1 AMPERES RMS
800 VOLTS

TO-92



TO-92		
DIM.	MIN.	MAX.
A	4.45	4.70
B	4.32	5.33
C	3.18	4.19
D	1.15	1.39
E	2.42	2.66
F	12.7	-----
G	2.04	2.66
I	3.43	-----

All Dimensions in millimeter

PIN ASSIGNMENT	
1	Main Terminal 1
2	Gate
3	Main Terminal 2

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$, unless otherwise specified.)

Absolute Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Peak repetitive off-state voltage ($T_j = -40$ to 125°C , Full sine wave, 50 to 60 Hz; Gate open) (Note 1)	V_{DRM} V_{RRM}	800	V
On-stage RMS current (Full sine wave, $T_c = 110^\circ\text{C}$)	$I_{T(RMS)}$	1	A
Peak non-repetitive surge current (one full cycle 60 Hz, $T_j = 25^\circ\text{C}$)	I_{TSM}	13.7	A
Circuit fusing consideration ($t = 8.3\text{ms}$)	I^2T	0.4	A^2s
Peak gate current	I_{GM}	2	A
Peak gate power	P_{GM}	5	W
Average gate power	$P_{G(AV)}$	0.1	W
Operating junction temperature range	T_j	-40 to +125	$^\circ\text{C}$
Storage temperature range	T_{STG}	-40 to +150	$^\circ\text{C}$

Note :

(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous basis.

Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

REV. 0, JUL-2016, KTXD27

T1M10T800A

CHARACTERISTIC & CURVES (T_j = 25°C, unless otherwise specified.)

Thermal Characteristics

PARAMETER	SYMBOL	VALUE	UNIT
Thermal resistance from junction	R _{th(j-c)}	60	°C/W
	R _{th(j-a)}	150	
Maximum lead temperature for soldering purposes (1/8" form case for 10 seconds)	T _L	260	°C

Static Characteristics

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Threshold Voltage ⁽¹⁾ @ T _j = 125°C	V _{to}	--	--	0.9	V
Dynamic resistors ⁽¹⁾ @ T _j = 125°C	R _d	--	--	390	mΩ
Peak repetitive forward or reverse blocking current (V _{AK} = rated V _{DRM} and V _{RRM} , gate open)	T _j = 25°C	I _{DRM}	--	5	uA
	T _j = 125°C	I _{RRM}	--	0.5	mA

1. For both polarities of A2 referenced to A1.

ON Characteristics

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Peak forward on-state voltage (I _{TM} = 1 A @ T _j = 25°C)	V _{TM}	--	1.2	1.5	V
V _D = V _{DRM} , R _L =100Ω, T _j =125°C	V _{GD}	0.3	--	--	V
Gate trigger current (V _{AK} = 12V, R _L =100Ω)	I _{GT1} I _{GT2} I _{GT3}	--	--	10	mA
Gate trigger voltage (V _{AK} = 12V, R _L =100Ω)	V _{GT1} V _{GT2} V _{GT3}	--	--	1	V
Holding current (V _{AK} = 12V, R _L =100Ω)	I _{H1} I _{H3}	--	--	12	mA
Latching current (V _{AK} = 12V, R _L =100Ω)	I _{L1}	--	--	12	mA
	I _{L2}	--	--	25	
	I _{L3}	--	--	12	

T1M10T800ACHARACTERISTIC & CURVES (T_j = 25°C, unless otherwise specified.)**LITEON**

Dynamic Characteristics

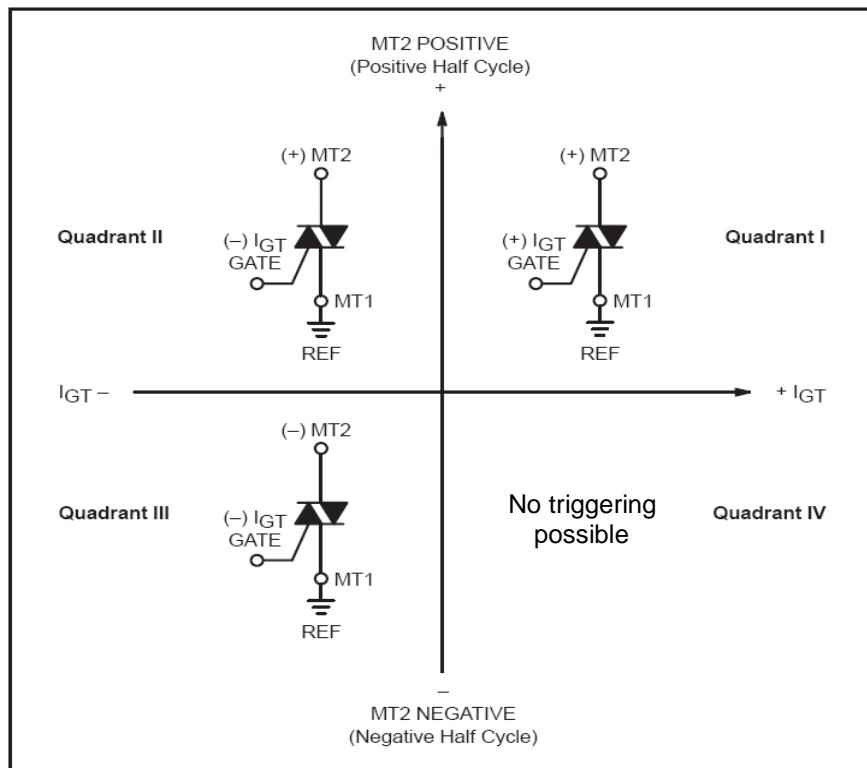
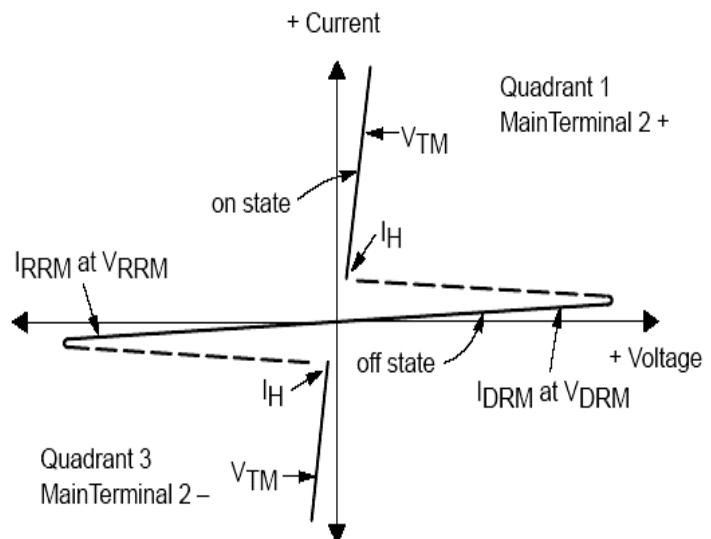
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Critical rate of rise of off-stage voltage (V _{AK} = 67% rated V _{DRM} , @ T _j = 125°C, gate open)	dv/dt	600	--	--	V/us
Rate of rise of on-state current (V _{DRM} =maximum V _{DRM} ,T _j = 125°C)	di/dt	--	--	100	A/us
Rate of change of commutating current	VD=400V, dv/dt(c)=10V/us,Tj=125°C	di/dt(c)	4	--	--
	Without snubber, VD=400V,Tj=125°C		3	--	--

T1M10T800A

CHARACTERISTIC & CURVES ($T_j = 25^\circ\text{C}$, unless otherwise specified.)

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Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On State Voltage
I_H	Holding Current



All polarities are referenced to MT1
With in -phase signal (using standard AC lines) quadrants I and III are used

T1M10T800A

CHARACTERISTIC & CURVES ($T_j = 25^\circ\text{C}$, unless otherwise specified.)

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Fig.1- Holding Current Variation

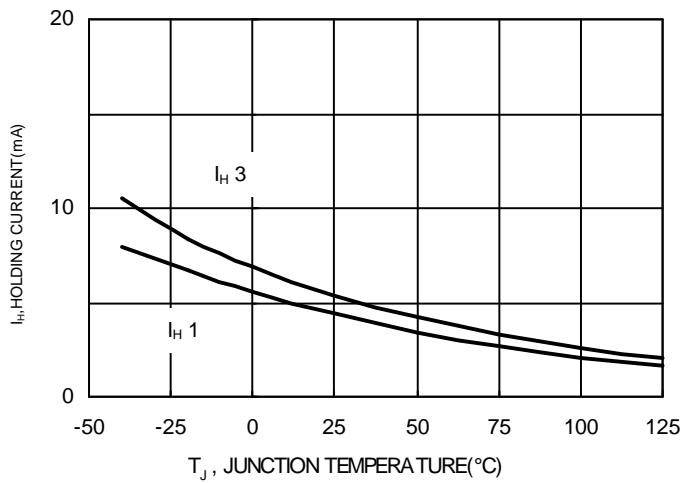


Fig.2- Gate Trigger Current Variation

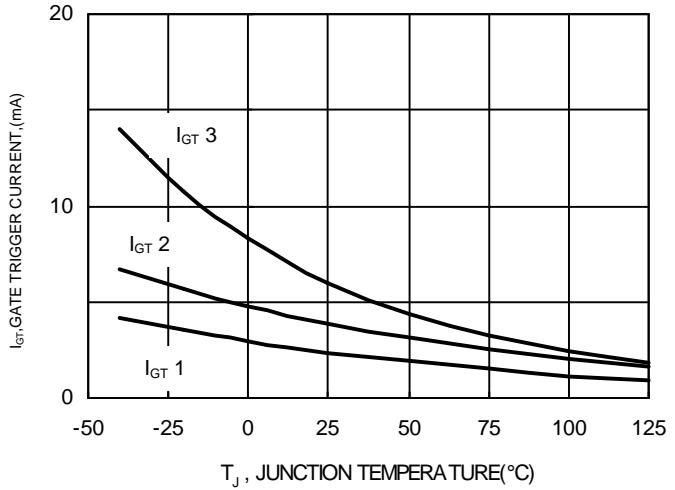


Fig.3- Gate Trigger Voltage Variation

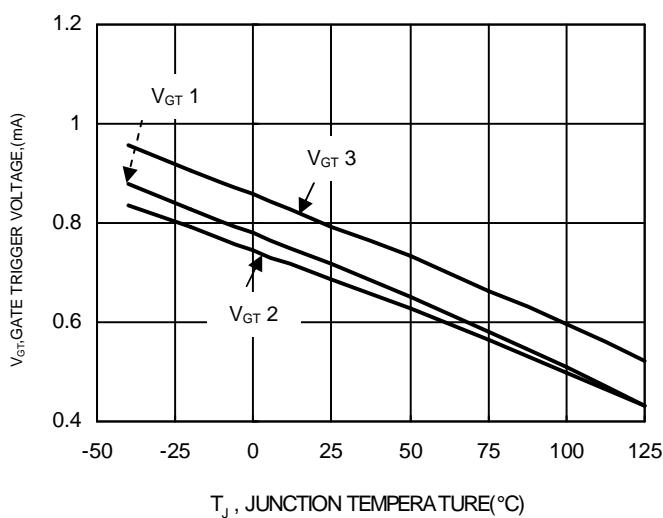


Fig.4- Typical Latching Current Versus Junction Temperature

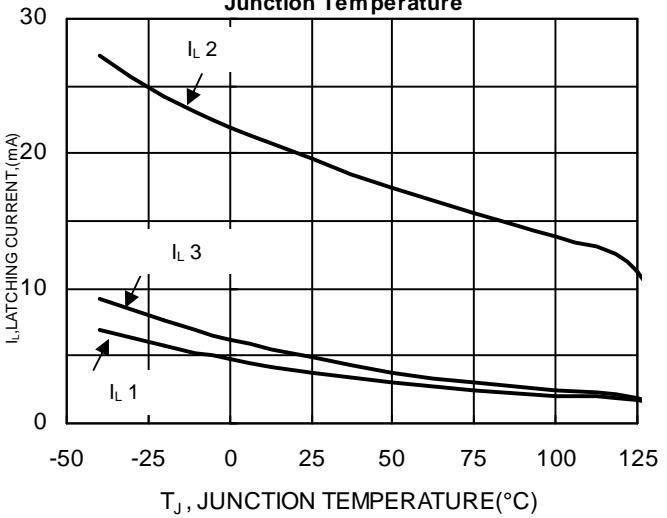


Fig.5- On-State Characteristics

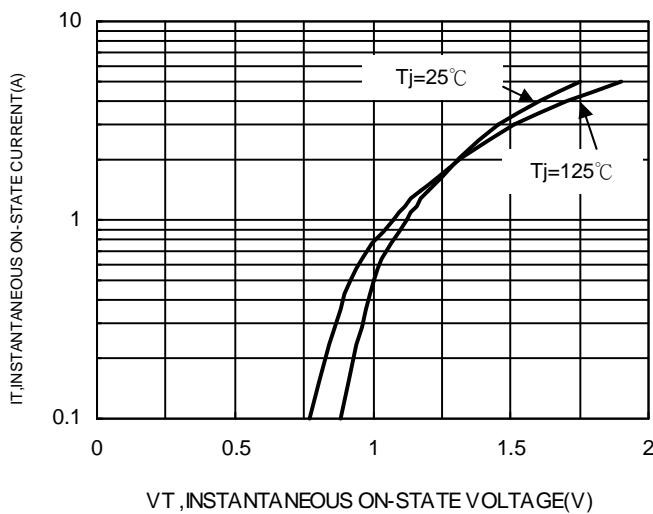
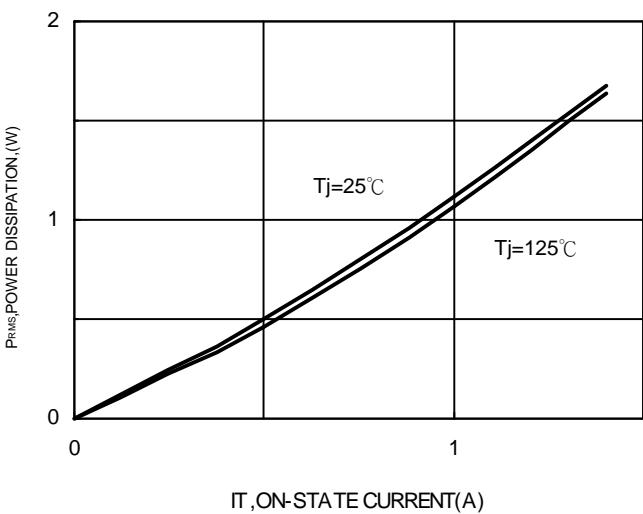


Fig.6- Power Dissipation versus IT



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