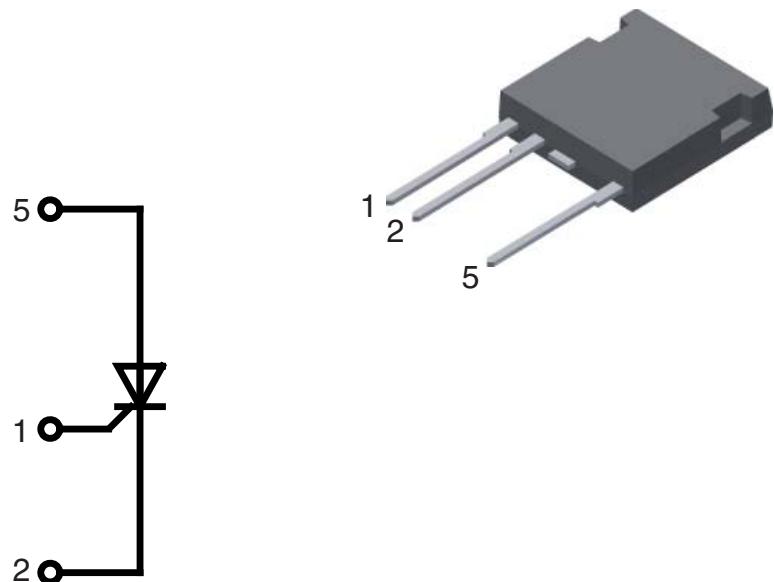


# High Voltage Phase Control Thyristor

in High Voltage  
ISOPLUS i4-PAC™

 $V_{DRM} = V_{RRM} = 2500 \text{ V}$   
 $I_{T(AV)} = 18 \text{ A}$   
 $I_{TSM} = 200 \text{ A}$ 

**Part number**  
CS 20-25mo1F



## Features / Advantages:

- high voltage thyristor
  - for line frequency
  - chip technology for long term stability
- ISOPLUS i4-PAC™
- high voltage package
  - isolated back surface
  - enlarged creepage towards heatsink
  - enlarged creepage between high voltage pins
  - application friendly pinout
  - high reliability
  - industry standard outline

## Applications:

- controlled rectifiers
  - power supplies
  - drives
- AC switches
- capacitor discharge control
  - flash tubes
  - X-ray and laser generators

## Package: i4-Pac

- Isolation Voltage: 3000 V~
- Industry convenient outline
- RoHS compliant
- Epoxy meets UL 94V-0
- Soldering pins for PCB mounting
- Backside: DCB ceramic
- Reduced weight
- Advanced power cycling

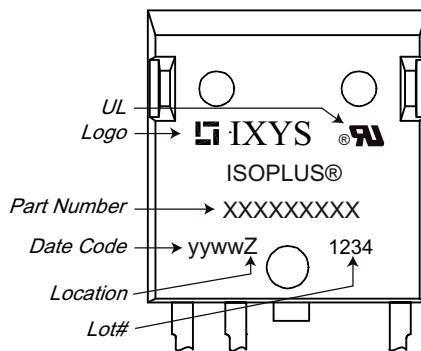
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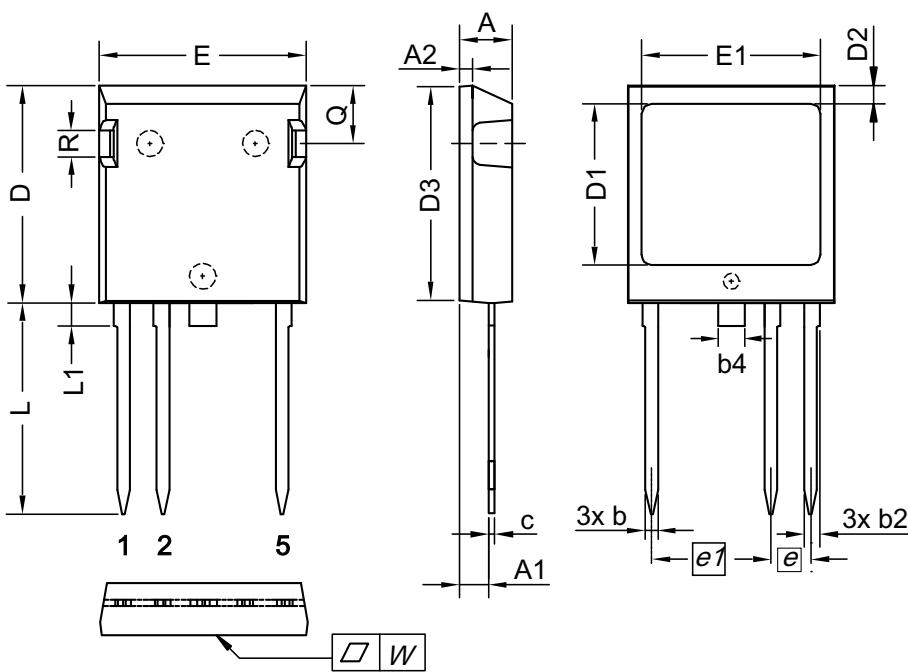
Thyristor			Ratings			
Symbol	Definitions	Conditions	min.	typ.	max.	Unit
$V_{DRM, RRM}$	max. repetitive blocking voltage				2500	V
$I_{T(AV)}$	average forward current	sine 180°	$T_C = 90^\circ C$		18	A
$I_{T(AV)}$		square; $d = \frac{1}{3}$	$T_C = 90^\circ C$		16	A
$I_{TSM}$	max. surge on-state current	sine 180°; $t = 10$ ms; $V_R = 0$ V	$T_{VJ} = 25^\circ C$		200	A
$(di/dt)_{cr}$	critical rate of rise of current	$T_{VJ} = T_{VJM}$ $f = 50$ Hz; $t_p = 200$ $\mu s$	repetitive, $I_T = 40$ A		100	A/ $\mu s$
		$V_D = \frac{2}{3} V_{DRM}$ $I_G = 0.45$ A $di_G/dt = 0.45$ A/ $\mu s$	non repetitive, $I_T = 20$ A		250	A/ $\mu s$
$(dv/dt)_{cr}$	critical rate of rise of voltage	$T_{VJ} = T_{VJM}$ ; $V_D = \frac{2}{3} V_{DRM}$ $R_{GK} = \infty$ ; method 1 (linear voltage rise)			2500	V/ $\mu s$
$V_T$	forward voltage	$I_T = 20$ A	$T_{VJ} = 25^\circ C$ $T_{VJ} = 125^\circ C$	1.3 1.3	1.5	V V
$V_{GT}$	gate trigger voltage	$V_D = 6$ V	$T_{VJ} = 25^\circ C$		2.3	V
$I_{GT}$	gate trigger current				250	mA
$V_{GD}$	gate non-trigger voltage	$V_D = \frac{2}{3} V_{DRM}$	$T_{VJ} = 125^\circ C$		0.2	V
$I_{GD}$	gate non-trigger current				5	mA
$I_L$	latching current	$t_p = 10$ $\mu s$ ; $V_D = 6$ V $I_G = 0.45$ A; $di_G/dt = 0.45$ A/ $\mu s$	$T_{VJ} = 25^\circ C$		500	mA
$I_H$	holding current	$V_D = 6$ V; $R_{GK} = \infty$	$T_{VJ} = 25^\circ C$		150	mA
$t_{gd}$	gate controlled delay time	$V_D = \frac{1}{2} V_{DRM}$ $I_G = 0.45$ A; $di_G/dt = 0.45$ A/ $\mu s$	$T_{VJ} = 25^\circ C$		2	$\mu s$
$I_R$	reverse current	$V_R = V_{RRM}$ ; $V_D = V_{DRM}$	$T_{VJ} = 25^\circ C$		50	$\mu A$
$I_D$	drain current		$T_{VJ} = 125^\circ C$	2	mA	
$R_{thJC}$	thermal resistance junction to case	DC current			0.92	K/W
$R_{thCH}$	thermal resistance case to heatsink	DC current		0.15		K/W

Package I4-Pac			Ratings			
Symbol	Definitions	Conditions	min.	typ.	max.	Unit
$I_{RMS}$	RMS current	per terminal			70	A
$T_{vJ}$	virtual junction temperature		-40		150	°C
$T_{op}$	operation temperature		-40		125	°C
$T_{stg}$	storage temperature		-40		150	°C
<b>Weight</b>				5.5		g
$F_c$	mounting force with clip		20		120	N
$d_{Spp/App}$ $d_{Spb/App}$	creepage distance on surface   striking distance through air	terminal to terminal terminal to backside	7.2 5.1			mm mm
$V_{ISOL}$	isolation voltage	$t = 1 \text{ second}$ $t = 1 \text{ minute}$	50/60 Hz, RMS, $I_{ISOL} \leq 1 \text{ mA}$		3000 2500	V V

### Product Marking



### Dimensions in mm (1 mm = 0.0394")



Dim.	Millimeter		Inches	
	min	max	min	max
A	4.83	5.21	0.190	0.205
A1	2.59	3.00	0.102	0.118
A2	1.17	2.16	0.046	0.085
b	1.14	1.40	0.045	0.055
b2	1.47	1.73	0.058	0.068
b4	2.54	2.79	0.100	0.110
c	0.51	0.74	0.020	0.029
D	20.80	21.34	0.819	0.840
D1	14.99	15.75	0.590	0.620
D2	1.65	2.03	0.065	0.080
D3	20.30	20.70	0.799	0.815
E	19.56	20.29	0.770	0.799
E1	16.76	17.53	0.660	0.690
e	3.81 BSC		0.150 BSC	
e1	11.43 BSC		0.450 BSC	
L	19.81	21.34	0.780	0.840
L1	2.11	2.59	0.083	0.102
Q	5.33	6.20	0.210	0.244
R	2.54	4.57	0.100	0.180
W	-	0.10	-	0.004

Die konvexe Form des Substrates ist typ. < 0.05 mm über der Kunststoffoberfläche der Bauteilunterseite  
The convex bow of substrate is typ. < 0.05 mm over plastic surface level of device bottom side