

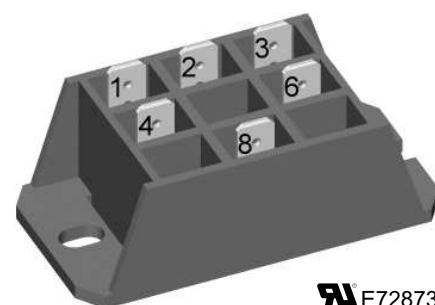
Half Controlled Single Phase Rectifier Bridge with Freewheeling Diode

$$I_{dAVM} = 32 \text{ A}$$

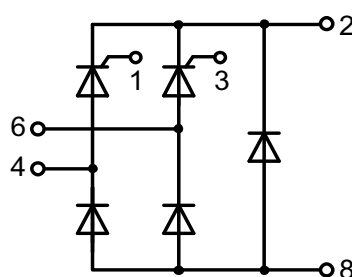
$$V_{RRM} = 800-1600 \text{ V}$$

Part numbers

V_{RSM} V_{DSM} V	V_{RRM} V_{DRM} V	Type
900	800	VHF 28-08io5
1300	1200	VHF 28-12io5
1700	1600	VHF 28-16io5



RL E72873



Features / Advantages:

- Planar passivated chips
- Space and weight savings
- Improved temperature & power cycling

Applications:

- Supply for DC power equipment
- DC motor control

Package: FO-F

- Isolation Voltage: 3600 V~
- DCB ceramic base plate
- 1/4" fast-on terminals
- Easy to mount with two screws
- RoHS compliant

Disclaimer Notice

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Diodes				Ratings			
Symbol	Definitions	Conditions		min.	typ.	max.	Unit
I_{dAV}	average DC output current	module	$T_K = 85^\circ\text{C}$			28	A
I_{dAVM}	max. average DC output current	for resistive load				32	A
I_{FRMS}, I_{TRMS}	RMS forward current	per leg				23	A
I_{FSM}, I_{TSM}	max. surge forward current	$t = 10\text{ ms (50 Hz), sine}$	$T_{VJ} = 45^\circ\text{C}$			300	A
		$t = 8.3\text{ ms (60 Hz), sine; } V_R = 0\text{ V}$				330	A
		$t = 10\text{ ms (50 Hz), sine}$	$T_{VJ} = 125^\circ\text{C}$			270	A
		$t = 8.3\text{ ms (60 Hz), sine; } V_R = 0\text{ V}$				300	A
I^2t	I^2t value for fusing	$t = 10\text{ ms (50 Hz), sine}$	$T_{VJ} = 45^\circ\text{C}$			440	A^2s
		$t = 8.3\text{ ms (60 Hz), sine; } V_R = 0\text{ V}$				455	A^2s
		$t = 10\text{ ms (50 Hz), sine}$	$T_{VJ} = 125^\circ\text{C}$			365	A^2s
		$t = 8.3\text{ ms (60 Hz), sine; } V_R = 0\text{ V}$				370	A^2s
$(di/dt)_{cr}$	critical rate of rise of current	$f = 50\text{ Hz, } t_p = 200\text{ }\mu\text{s, } V_D = 2/3 V_{DRM}, T_{VJ} = 125^\circ\text{C}$ $I_G = 0.3\text{ A, } di_G/dt = 0.3\text{ A}/\mu\text{s}$ repetitive, $I_T = 50\text{ A}$ non repetitive, $I_T = 1/2 I_{dAV}$				150 500	$\text{A}/\mu\text{s}$ $\text{A}/\mu\text{s}$
$(dv/dt)_{cr}$	critical rate of rise of voltage	$V_D = 2/3 V_{DRM}$ $R_{GK} = \infty$; method 1 (linear voltage rise)	$T_{VJ} = 125^\circ\text{C}$			1000	$\text{V}/\mu\text{s}$
V_{RGM}	max. reverse gate voltage					10	V
P_{GM}	max. gate power dissipation	$I_T = I_{TAVM}$ $t_p = 30\text{ }\mu\text{s}$ $t_p = 500\text{ }\mu\text{s}$ $t_p = 10\text{ ms}$	$T_{VJ} = 125^\circ\text{C}$			10	W
						5	W
						1	W
P_{GAVM}	max. average gate power dissipation					0.5	W

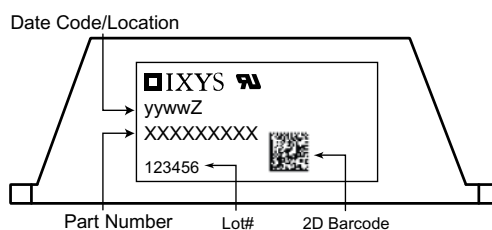
Thyristors				Ratings			
Symbol	Definitions	Conditions		min.	typ.	max.	Unit
I_R, I_D	reverse, drain current	$V_R = V_{RRM}; V_D = V_{DRM}$	$T_{VJ} = 25^\circ\text{C}$			0.3	mA
			$T_{VJ} = 125^\circ\text{C}$			5	mA
V_T, V_F	forward voltage	$I_T, I_F = 45\text{ A}$	$T_{VJ} = 25^\circ\text{C}$			1.6	V
V_{TO}		For power-loss calculations only	$T_{VJ} = 125^\circ\text{C}$		0.9		V
r_T					15		$\text{m}\Omega$
V_{GT}	gate trigger voltage	$V_D = 6\text{ V}$	$T_{VJ} = 25^\circ\text{C}$			1.0	V
			$T_{VJ} = -40^\circ\text{C}$			1.2	V
I_{GT}	gate trigger current	$V_D = 6\text{ V}$	$T_{VJ} = 25^\circ\text{C}$			65	mA
			$T_{VJ} = -40^\circ\text{C}$			80	mA
			$T_{VJ} = 125^\circ\text{C}$			50	mA
V_{GD}	gate non-trigger voltage	$V_D = 2/3 V_{DRM}$	$T_{VJ} = 125^\circ\text{C}$			0.2	V
I_{GD}	non-trigger gate current					5	mA
I_L	latching current	$I_G = 0.3\text{ A, } t_G = 30\text{ }\mu\text{s}$ $di_G/dt = 0.3\text{ A}/\mu\text{s}$	$T_{VJ} = 25^\circ\text{C}$			150	mA
			$T_{VJ} = -40^\circ\text{C}$			200	mA
			$T_{VJ} = 125^\circ\text{C}$			100	mA
I_H	holding current	$V_D = 6\text{ V, } R_{GK} = \infty$	$T_{VJ} = 25^\circ\text{C}$			100	ns
t_{gd}	gate controlled delay time	$V_D = 1/2 V_{DRM}$ $I_G = 0.3\text{ A, } di_G/dt = 0.3\text{ A}/\mu\text{s}$	$T_{VJ} = 25^\circ\text{C}$		2		μs
t_q	turn-off time	$I_T = 15\text{ A, } t_p = 300\text{ }\mu\text{s, } V_R = 100\text{ V; } T_{VJ} = 125^\circ\text{C}$ $di/dt = -10\text{ A}/\mu\text{s, } dv/dt = 20\text{ V}/\mu\text{s, } V_D = 2/3 V_{DRM}$			150		μs
Q_r	reverse recovery charge				75		μC
R_{thJC}	thermal resistance junction to case	per thyristor (diode); DC current per module				1.4	K/W
						0.35	K/W
R_{thJH}	thermal resistance junction to heatsink	per thyristor (diode); DC current per module			2.0		K/W
					0.5		K/W

Data according to IEC 60747 and refer to a single thyristor/diode unless otherwise stated.

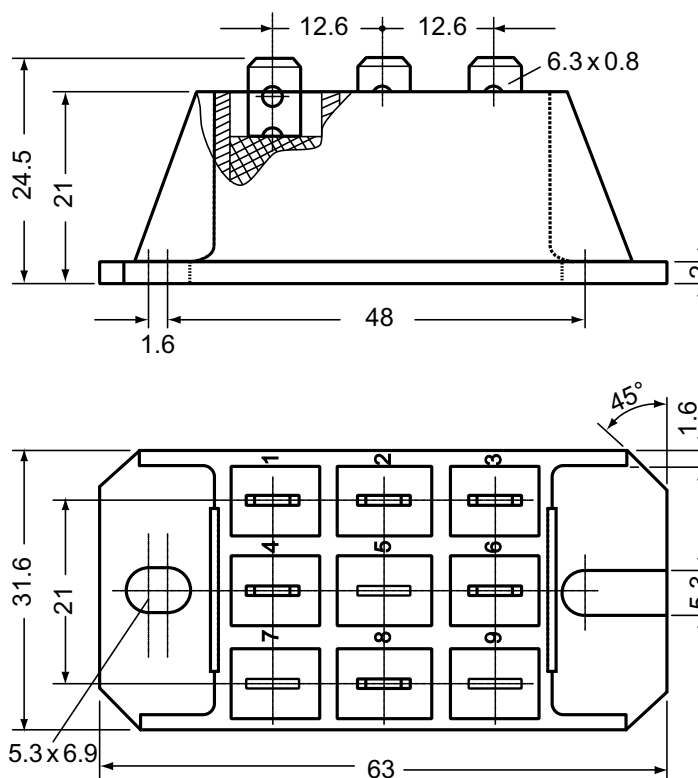
IXYS reserves the right to change limits, test conditions and dimensions.

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Package FO-F			Ratings			
Symbol	Definitions	Conditions	min.	typ.	max.	Unit
I_{RMS}	RMS current	per terminal			100	A
T_{VJ}	virtual junction temperature		-40		125	°C
T_{op}	operation temperature		-40		100	°C
T_{stg}	storage temperature		-40		125	°C
Weight				45		g
M_D	mounting torque		2		2.5	Nm
$d_{Spp/App}$	creepage distance on surface / striking distance through air	terminal to terminal	18.0	6.0		mm
$d_{Spb/Appb}$		terminal to backside	26.0	20.0		mm
V_{ISOL}	isolation voltage	t = 1 second	3600			V
		t = 1 minute	3000			V



Dimensions in mm (1 mm = 0.0394")



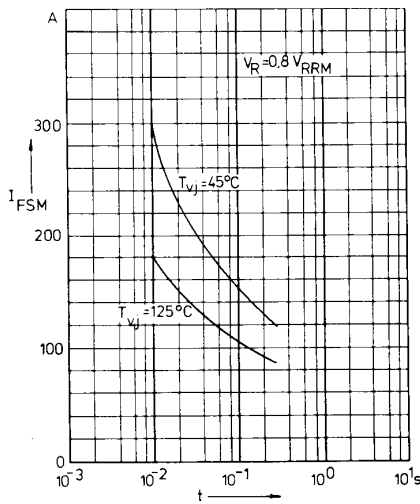


Fig. 1 Surge overload current per chip
 I_{FSM} : Crest value, t : duration

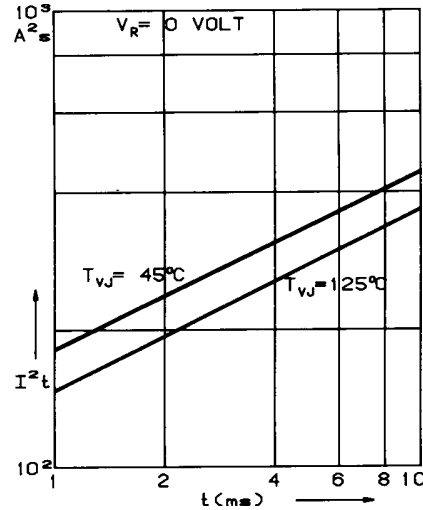


Fig. 2 I^2t versus time (1-10 ms)
per chip

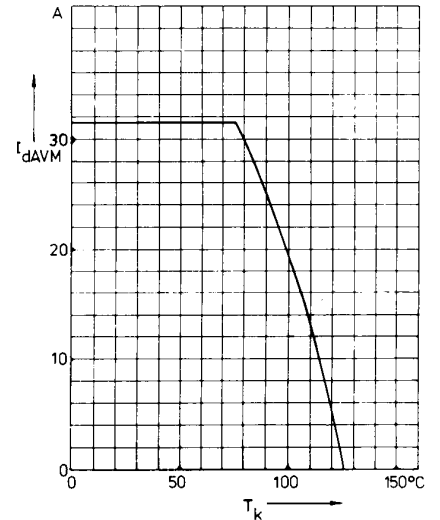


Fig. 3 Max. forward current at
heatsink temperature

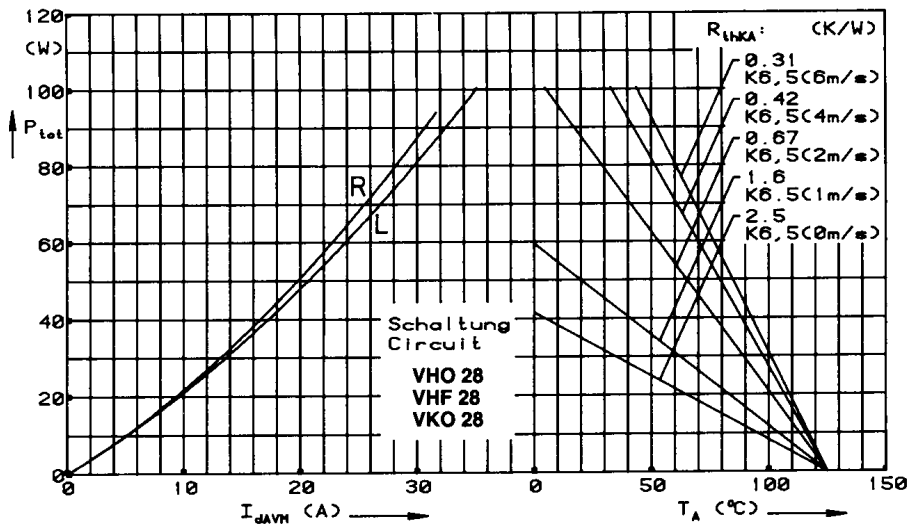


Fig. 4 Power dissipation versus direct output current and ambient temperature

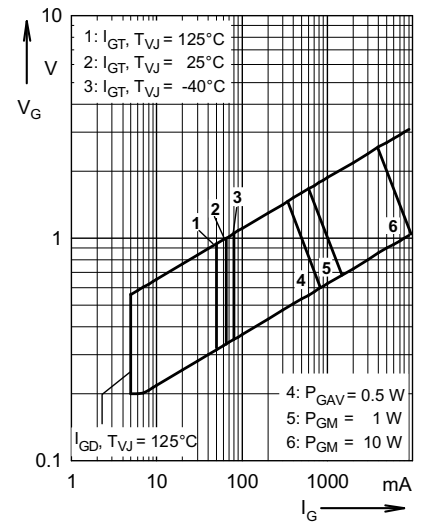


Fig. 5 Gate trigger range

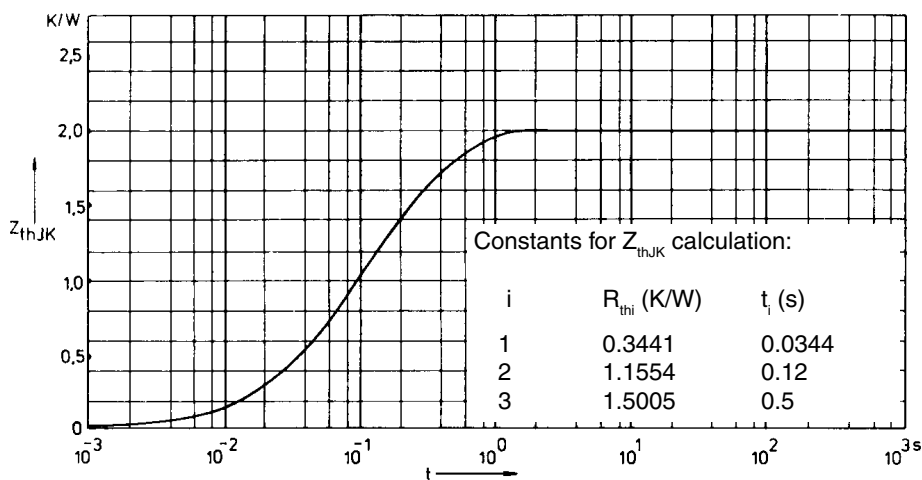


Fig. 7 Transient thermal impedance junction to heatsink per chip

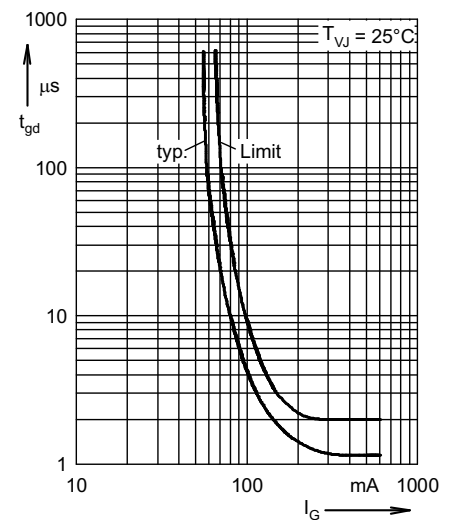


Fig. 7 Gate controlled delay time