

Transceiver Phase Noise Teardown Informs Performance Capability with an External LO

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Abstract

Software-defined radios are one of the leading topics in the industry today. The software-defined radio's performance capability has been fueled by the release of radio frequency (RF) transceivers offering complete radio solutions in monolithic integrated circuits (ICs). The Analog Devices transceiver product line provides an enabling IC, proliferating into many radio designs that are completely software controlled. One of the areas still to be explored with these devices is the capability for low phase noise applications. This article evaluates the phase noise performance of these highly integrated radio frequency integrated circuits (RFICs) with emphasis on cases wherein external frequencies are provided.

Measurements on the Analog Devices [ADRV9009](#) transceiver when using an external local oscillator (LO) indicate significant phase noise improvement is possible when a low noise LO is used. The transceiver architecture is presented from a phase noise contribution point of view. Through a series of measurements, the residual or additive phase noise is extracted as a function of the frequency programmed at the DAC output. Using this noise contribution along with phase noise of the input frequencies, both the LO and the reference, the total phase noise at the transmit output can be estimated. These estimates are compared with measured results.

Introduction/Motivation

Phase noise is one of the critical metrics of signal quality characterized in radio designs. Much effort is placed during the architecture definition phase to ensure the phase noise requirements are achieved in the most economical manner possible.

Measurements on the ADRV9009 transceiver indicate there are a wide range of possible noise performance outcomes depending on the implementation chosen. When using the internal LO capability, the phase noise is determined by the internal, IC-based phase-locked loop (PLL) and voltage controlled oscillator (VCO). The internal LO has been designed to meet the majority of communications applications. For applications demanding improved phase noise performance, when a low phase noise source is used as an external LO, a significant phase noise improvement can be realized.

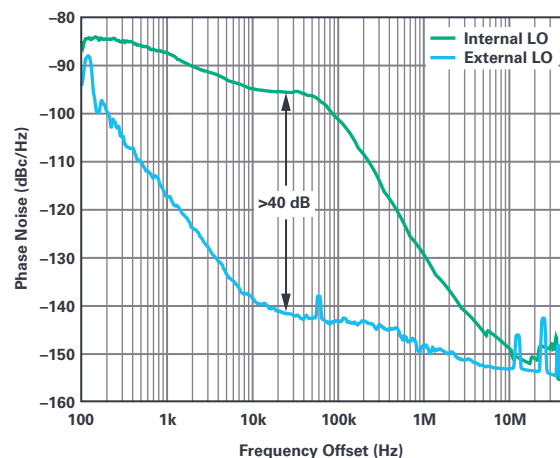


Figure 1. ADRV9009 transceiver phase noise measurements. When using the internal LO capability, the phase noise is limited by the IC-based PLL/VCO. If using a low phase noise external LO, a significant phase noise improvement can be realized.

Figure 1 demonstrates a potential for over 40 dB of phase noise improvement over the 10 kHz to 100 kHz offsets for the ADRV9009 transceiver. The conditions under which these measurements were taken are as follows: For the internal LO measurement the LO frequency is set to 2.6 GHz, with a DAC output of 8 MHz. For the external LO measurements, a Rohde & Schwarz SMA100B was used as the LO source. There is an internal frequency divider on the LO path, so for an LO frequency of 2.6 GHz, the generator was set to 5.2 GHz. Measurements were taken with the Holzworth HA7402 phase noise analyzer.

ADRV9009 Transceiver

The ADRV9009 is the latest release to the Analog Devices transceiver product line. The transceiver architecture is shown in Figure 2. The transceivers are dual channel radios, with both transmit and receive, implemented with direct conversion architectures,¹ in monolithic ICs. The digital processing includes quadrature error correction, dc offset, and LO leakage algorithms that enable the performance that has been achieved in a direct conversion architecture. The transceiver provides a complete RF to digital functionality. RF frequencies are supported up to 6 GHz and a JESD204B interface provides a high speed data interface to an ASIC- or FPGA-based processor.

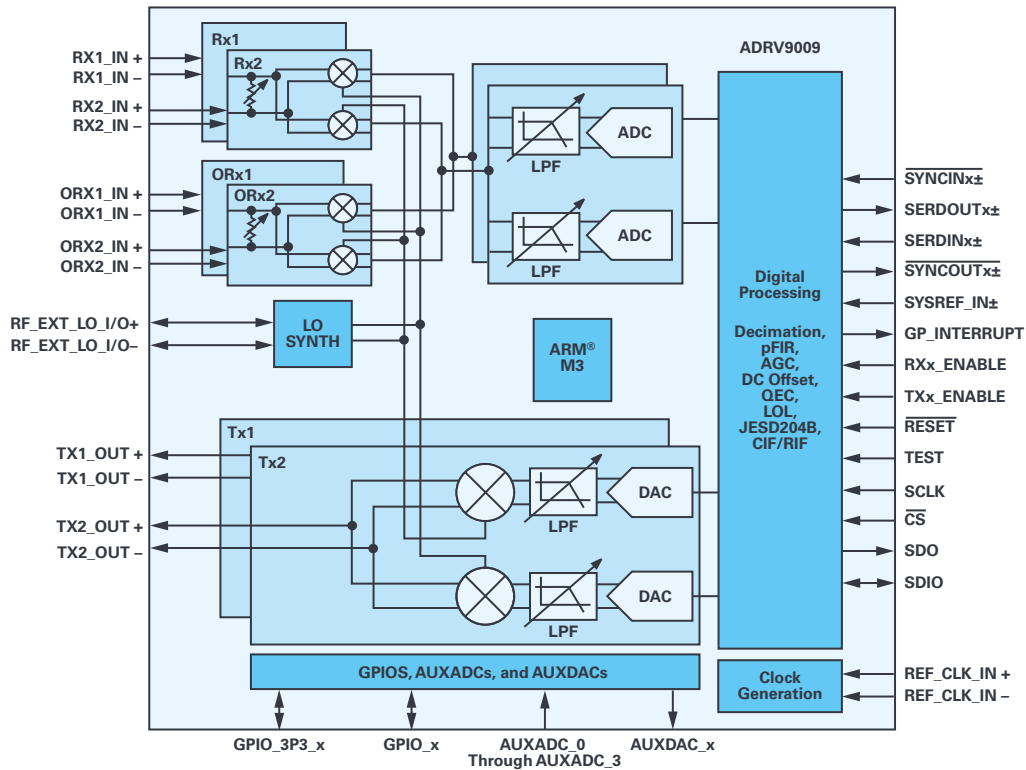


Figure 2. ADRV9009 transceiver functional block diagram.

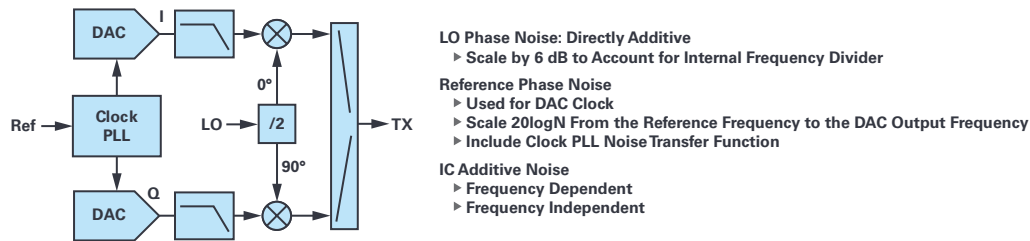


Figure 3. Direct upconversion block diagram and associated phase noise contributors.

The radio is synchronized to a reference frequency input. Several PLLs phase lock to the reference including the converter clocks, the LO, and digital clocks. Provisions for an external LO are offered to allow bypassing the internal LO PLL. The LO path has a frequency divider between the PLL or external LO input and the mixer ports. This is used to generate the quadrature LO signals needed for the direct conversion architecture. The converter clocks and LO have a direct impact on the achievable phase noise and are discussed further as phase noise contributors are evaluated.

Examining the Phase Noise Contributors

The phase noise at the transmit output is comprised of several contributors. Figure 3 illustrates a simplified block diagram of the direct conversion waveform generator architecture used along with the primary phase noise contributors.

Before dissecting the transceiver phase noise, a couple fundamental principles are worth reviewing. In a frequency multiplier or divider, phase noise scales $20\log N$, where N is the input to output frequency ratio.² This also applies to a direct digital synthesizer (DDS) where the clock noise contribution scales $20\log N$ with the DDS output frequency. The second area to consider is the phase noise transfer functions in a PLL.³ A reference frequency injected into a PLL will scale to the output both as a function of the frequency ratio (similar to a multiplier), but will have a low-pass filter effect applied based on the loop bandwidth (BW) and type of loop filter chosen.

Applying these principles to the transceiver, various contributors can be examined. There are two frequencies, the LO frequency and the reference frequency, that are injected into the transceiver. The LO frequency has a direct contribution to the phase noise output but is reduced by 6 dB in the internal frequency divider used to create the quadrature LO signals to the mixer. The reference frequency contribution is determined from several factors. It is used to create the DAC clock in the clock PLL. The noise on the clock output due to the reference frequency will scale by the noise transfer function of the PLL. Then this contribution will be scaled again by the ratio of the DAC clock to the DAC output frequency. This effect can be simplified to a scaling of the reference frequency to the DAC output frequency with a low-pass transfer function applied based on the PLL BW.

Next, consider the transceiver IC phase noise contribution. There is a residual noise added from all of the circuit components in the transmit path. One of the IC noise contributors is an additive noise at the DAC output that varies as a function of the DAC output frequency. This can be summarized into two residual phase noise terms; a frequency dependent noise contribution and a frequency independent noise contribution. The frequency dependent noise will scale $20\log N$ with the DAC output frequency. The frequency independent noise is fixed and will set the phase noise floor contribution of the transceiver IC.

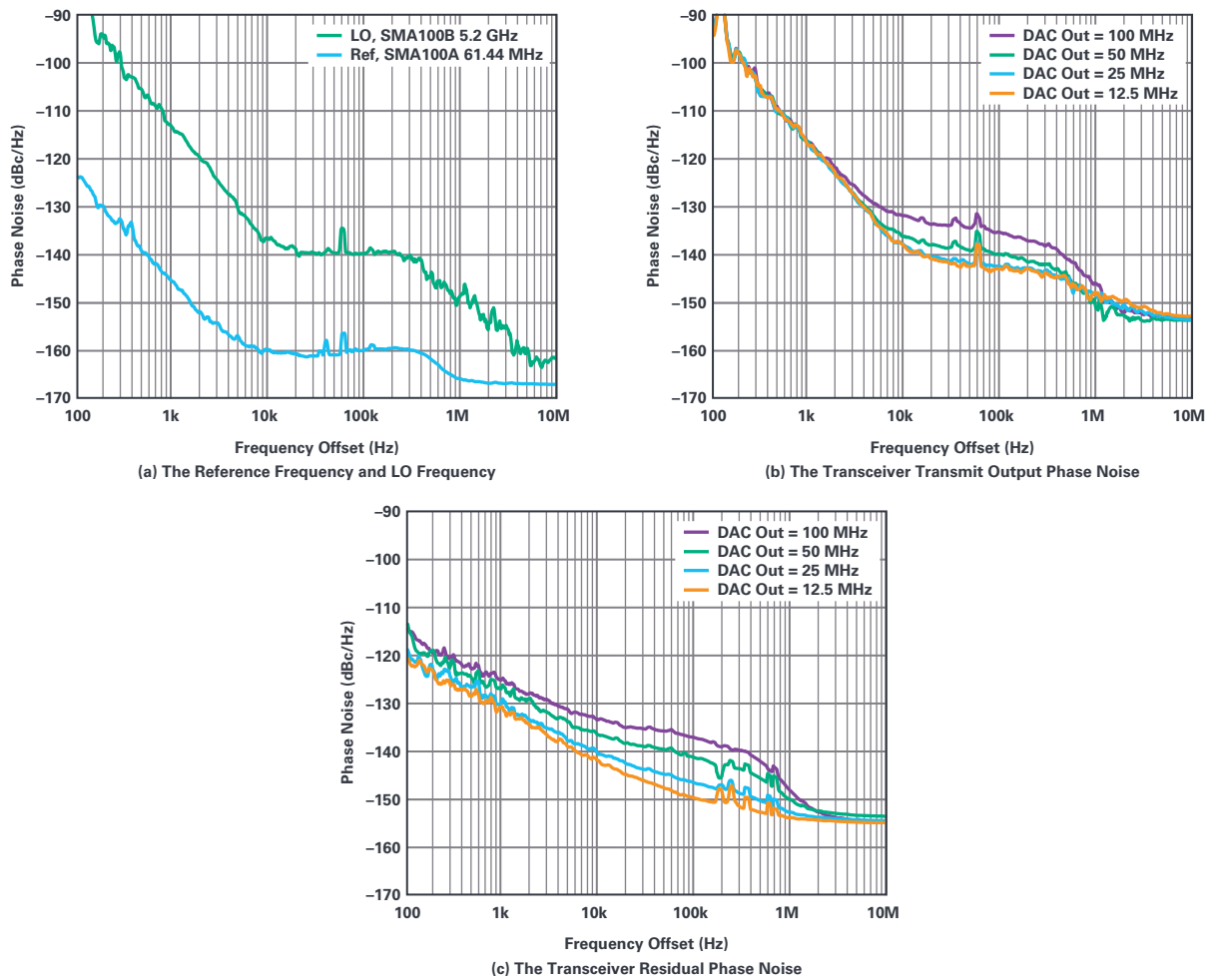


Figure 4. Phase noise measurements used to extract the varied phase noise contributors.

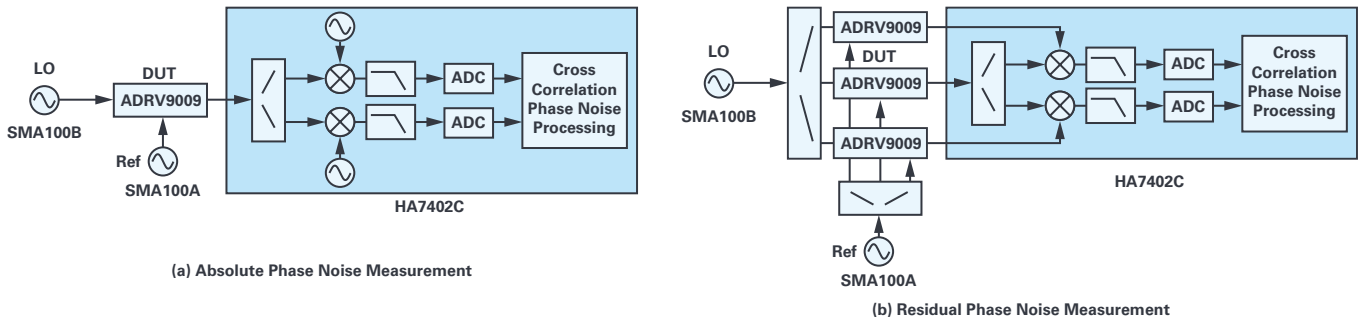


Figure 5. Test setups used for the phase noise measurements.

To extract the IC residual noise contribution as a function of frequency dependent and frequency independent contributors, a series of phase noise measurements were conducted as shown in Figure 4.

The test setups used for the phase noise measurements are shown in Figure 5. For the transceiver LO and reference frequency inputs, a Rohde & Schwarz SMA100B and 100 A were used, respectively. The Holzworth HA7402C was used as the phase noise test set. For absolute phase noise measurements, the transmit output of the transceiver is injected into the test set. For residual phase noise measurements, three transceivers are required, and when using the additional transceivers as the LO port of the mixer in the test set, the noise contribution of the reference frequency and LO frequency can be removed from the measurement.

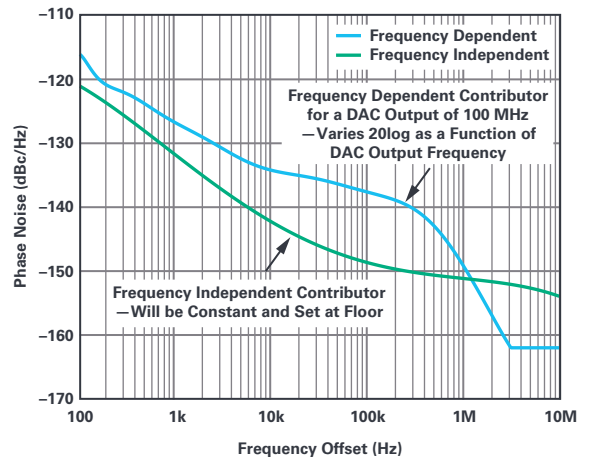


Figure 6. Transceiver residual phase noise contributors. These curves were extracted from the measured data of Figure 4.

By evaluating the measured data of Figure 4, frequency dependent and frequency independent phase noise contributors from the transceiver IC were extracted. The estimates are shown in Figure 6. The estimates were derived from both curve fits to the measured data and threshold settings applied to the phase noise floor at offset frequencies greater than 1 MHz.

Absolute Phase Noise Measurements vs. Predictions

By evaluating the different phase noise contributors as described, predictions based on the DAC output frequency and the oscillators used for the LO and reference can be calculated. Measured vs. predicted results are shown in Figure 7.

The contributors were calculated as follows:

- ▶ LO phase noise contribution: The measured LO phase noise of Figure 4 was used and reduced by 6 dB to account for the frequency divider inside the transceiver IC.
- ▶ Reference phase noise contribution: The measured reference noise of Figure 4 was used as the starting point. The clock PLL in the transceiver has a loop BW of several hundred kHz, so a second-order low-pass filter with a similar BW was applied against the reference noise. The noise was then scaled by $20\log$ of the ratio of the DAC output frequency to the reference frequency.
- ▶ IC contribution: The curves of Figure 6 were used.

The measured results very closely match the predictions and the graphs indicate which contributors dominate various offset frequencies. At offset

frequencies below ~5 kHz, the first LO dominates. At offsets above ~1 MHz, the IC residual noise dominates. At mid-offset frequencies between ~10 kHz and ~500 kHz, the DAC output frequency becomes a factor. At higher DAC output frequencies, the IC frequency dependent noise dominates. As the DAC output frequency is reduced, the IC contribution reduces to a point where the LO frequency again dominates the performance.

External LO Considerations

Some practical considerations for designs exploring use of an external LO are worth noting. There are two particular items that can be a limitation.

- ▶ With the internal frequency divider, there is a phase ambiguity on startup or when switching the external LO. An RF phase sync feature is included with the internal LO that this is not yet available with the external LO.
- ▶ When hopping an external LO, there is a settling time of the QEC algorithm that can spuriously affect images during moments directly after a frequency change.

Both of these items lead to a complication in multichannel systems, dynamically hopping across operating bands greater than the transceiver's instantaneous bandwidth. For future transceivers, these limitations may be overcome, but at the time of this writing these complications exist for the ADRV9009 when used with an external LO.

In spite of these complications, there are a variety of applications that could exploit the improved phase of an external LO. These include any single channel or low channel count systems with less stringent dynamic hopping requirements or any multichannel system with a fixed LO frequency.

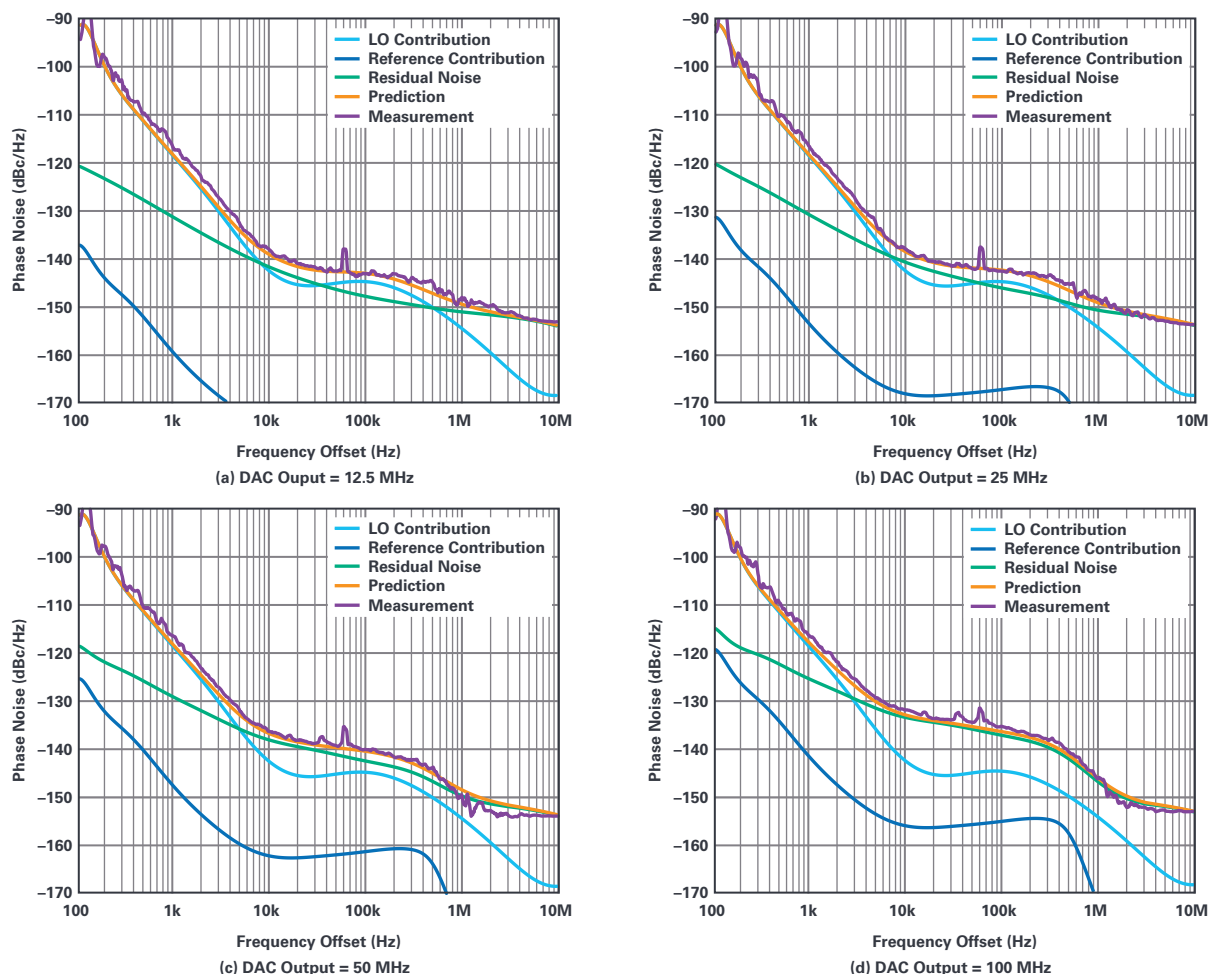


Figure 7. Measured vs. predicted phase noise with an external LO. The LO was set to 5.2 GHz for a transceiver center frequency of 2.6 GHz. The DAC output frequency was varied from 12.5 MHz to 100 MHz. Results are predictable and indicate the analysis method can be extended to additional frequencies.

A particular application that could benefit from the external LO phase noise performance is a relatively narrow-band phased array. In this application, it is practical to use the transceivers for a generic waveform generator and receiver design that can support a wide selection of operating frequencies, then during operation or final LO implementation a particular band is chosen.

For phased array systems with operating bands within the transceiver's instantaneous bandwidth, the external LO could be a single frequency and using the transceivers in a phased array with an external LO in this case could be a very practical option. When evaluating the system phase noise, the reference frequency source oscillator can be chosen such that the reference frequency noise contribution is much lower than the LO noise contribution. If there is a common LO distributed to an array of transceivers, as the quantity of transceivers coherently combined in a system increases, the noise contribution from the IC will reduce to a level where the system will be dominated by the external LO. This conclusion simplifies the system engineering noise analysis. With noise dominated by a common LO, engineering efforts could focus on the optimum cost/performance trade-off of the central LO design.

Summary

A method to predict the ADRV9009 transceiver phase noise when using an external LO has been provided. The method allows tracking contributions from the reference oscillator, the LO source, and the transceiver as a function of the DAC output frequency. Measured vs. predicted results are well matched, indicating that the approach can be extended to analyze the transceiver capability when used with other frequency sources. The approach is also quite general and could be extended to any waveform generator design.

The measured phase noise performance with an external LO offers a significant performance advantage once effort is placed on creating a low phase noise LO source. Our intention is to provide a range of options for system designers as architecture options are evaluated. For designs using the transceivers in low phase noise applications with an external LO input, the description provides a foundation to assess system level phase noise under varied conditions.

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About the Author

Peter Delos is a technical lead in the Aerospace and Defense Group at Analog Devices in Greensboro, North Carolina. He received his B.S.E.E. from Virginia Tech in 1990 and M.S.E.E. from NJIT in 2004. Peter has over 25 years of industry experience. Most of his career has been spent designing advanced RF/analog systems at the architecture level, PWB level, and IC level. He is currently focused on miniaturizing high performance receiver, waveform generator, and synthesizer designs for phased array applications. He can be reached at peter.delos@analog.com.

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