Data Sheet

# ADRF5048

## Silicon SP4T Switch, Nonreflective, 100 MHz to 45 GHz

## FEATURES

- Ultrawideband frequency range: 100 MHz to 45 GHz
- Nonreflective 50 Ω design
- Low insertion loss
  - 1.4 dB at 18 GHz typical
  - 2.4 dB at 40 GHz typical
  - 4.0 dB at 45 GHz typical
- High isolation
  - 41 dB at 18 GHz typical
  - 35 dB at 40 GHz typical
  - 35 dB at 45 GHz typical
- High input linearity
  - P0.1dB: >30 dBm typical
  - IP3: 52 dBm typical
- High power handling
  - 30 dBm through path
  - 18 dBm terminated path
- No low frequency spurious
- ESD ratings
  - HBM
    - ±1000 V for RFx pins
    - ±2000 V for supply and digital control pins
  - CDM: ±500 V for all pins
- On and off time (50% $V_{CTRL}$ to 90% of final $RF_{OUT}$): 20 ns
- RF settling time (50% $V_{CTRL}$ to 0.1 dB of final $RF_{OUT}$): 60 ns
- 3 mm x 3 mm, 24-terminal LGA package
- Pin compatible with the ADRF5049, ADRF5042, and ADRF5043

## APPLICATIONS

- Industrial scanners
- Test instrumentation
- Cellular infrastructure mmWave 5G
- Military radios, radars, and electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

## FUNCTIONAL BLOCK DIAGRAM

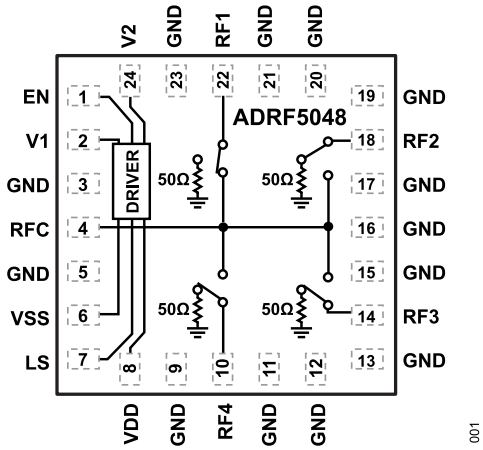


*Figure 1. Functional Block Diagram*

## GENERAL DESCRIPTION

The ADRF5048 is a nonreflective SP4T switch manufactured in the silicon on insulator (SOI) process.

This device operates from 100 MHz to 45 GHz with an insertion loss lower than 4.0 dB and isolation higher than 35 dB. The ADRF5048 has an RF input power handling capability of 30 dBm through path, 18 dBm terminated path, and 30 dBm hot switching at the RF common port.

The ADRF5048 requires a dual-supply voltage of +3.3 V and −3.3 V. The device employs complimentary metal-oxide semiconductor (CMOS)-/low-voltage transistor to transistor logic (LVTTL) logic-compatible controls.

The ADRF5048 has enable and logic select controls to feature all off state and mirror port selection, respectively.

The ADRF5048 is pin compatible with the ADRF5049, ADRF5042 and ADRF5043.

The ADRF5048 comes in a 24-terminal, 3 mm × 3 mm, RoHS compliant, land grid array (LGA) package and can operate from −40°C to +105°C.

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**11/2023—Rev. 0 to Rev. A**
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**8/2023—Revision 0: Initial Version**

## SPECIFICATIONS

VDD = 3.3 V, VSS = −3.3 V, V1 = 0 V or 3.3 V, V2 = 0 V or 3.3 V, $T_A$ = 25°C, and it is a 50 Ω system, unless otherwise noted. $V_{CTRL}$ is the voltages of the digital control inputs, V1 and V2.

***Table 1. Specifications***

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| FREQUENCY RANGE | | 0.1 | | 45 | GHz |
| INSERTION LOSS | | | | | |
| Between RFC and RF1 to RF4 (On) | 100 MHz to 18 GHz | | 1.4 | | dB |
| | 18 GHz to 26 GHz | | 1.7 | | dB |
| | 26 GHz to 35 GHz | | 2.1 | | dB |
| | 35 GHz to 40 GHz | | 2.4 | | dB |
| | 40 GHz to 45 GHz | | 4.0 | | dB |
| ISOLATION | | | | | |
| Between RFC and RF1 to RF4 (Off) | 100 MHz to 18 GHz | | 41 | | dB |
| | 18 GHz to 26 GHz | | 40 | | dB |
| | 26 GHz to 35 GHz | | 36 | | dB |
| | 35 GHz to 40 GHz | | 35 | | dB |
| | 40 GHz to 45 GHz | | 35 | | dB |
| RETURN LOSS | | | | | |
| RFC and RF1 to RF4 (On) | 100 MHz to 18 GHz | | 22 | | dB |
| | 18 GHz to 26 GHz | | 17 | | dB |
| | 26 GHz to 35 GHz | | 16 | | dB |
| | 35 GHz to 40 GHz | | 22 | | dB |
| | 40 GHz to 45 GHz | | 9 | | dB |
| RF1 to RF4 (Off) | 100 MHz to 18 GHz | | 22 | | dB |
| | 18 GHz to 26 GHz | | 19 | | dB |
| | 26 GHz to 35 GHz | | 16 | | dB |
| | 35 GHz to 40 GHz | | 16 | | dB |
| | 40 GHz to 45 GHz | | 16 | | dB |
| SWITCHING | | | | | |
| Rise Time and Fall Time ($t_{RISE}$, $t_{FALL}$) | 90% to 10% of RF output ($RF_{OUT}$) | | 4 | | ns |
| On Time and Off Time ($t_{ON}$, $t_{OFF}$) | 50% $V_{CTL}$ to 10% to 90% of $RF_{OUT}$ | | 20 | | ns |
| Settling Time | | | | | |
| 0.1dB | 50% $V_{CTL}$ to 0.1 dB of final $RF_{OUT}$ | | 60 | | ns |
| INPUT LINEARITY | | | | | |
| 0.1 dB Power Compression (P0.1dB) | f = 0.3 GHz to 40 GHz | | >30 | | dBm |
| Third-Order Intercept (IP3) | Two-tone input power = 14 dBm continuous wave per tone, f = 1 GHz to 40 GHz, Δf = 1MHz | | 52 | | dBm |
| SUPPLY CURRENT | VDD and VSS pins | | | | |
| Positive Supply Current ($I_{DD}$) | | | 150 | | µA |
| Negative Supply Current ($I_{SS}$) | | | 520 | | µA |
| DIGITAL CONTROL INPUTS | | | | | |
| Voltage | | | | | |
| Low ($V_{INL}$) | | 0 | | 0.8 | V |
| High ($V_{INH}$) | | 1.2 | | 3.45 | V |
| Current | | | | | |
| Low ($I_{INL}$) | | | <1 | | µA |
| High ($I_{INH}$) | V1 and V2 | | <1 | | µA |
| | EN and LS | | 33 | | µA |

## SPECIFICATIONS

*Table 1. Specifications (Continued)*

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RECOMMENDED OPERATING CONDITIONS | | | | | |
| Supply Voltage | | | | | |
| Positive (VDD) | | 3.15 | | 3.45 | V |
| Negative (VSS) | | −3.45 | | −3.15 | V |
| Digital Control Inputs Voltages (V1, V2) | | 0 | | VDD | V |
| RF Input Power | f = 0.3 GHz to 40 GHz, $T_{CASE}$ = 85°C, life time | | | | |
| Through Path | RF signal is applied to RFC or through connected RFx | | | 30 | dBm |
| Terminated Path | RF signal is applied to terminated RFx | | | 18 | dBm |
| Hot Switching | RF signal is present at RFC while switching between RFx | | | 30 | dBm |
| Case Temperature ($T_{CASE}$) | | –40 | | +105 | °C |

## ABSOLUTE MAXIMUM RATINGS

*Table 2. Absolute Maximum Ratings*

| Parameter | Rating |
|---|---|
| Supply Voltage | |
| VDD | –0.3 V to +3.6 V |
| VSS | –3.6 V to +0.3 V |
| Digital Control Inputs Voltage | –0.3 V to VDD + 0.3 V |
| RF Input Power (Frequency[1] = 0.3 GHz to 40 GHz, $T_{CASE}$ = 85°C[2]) | |
| Through Path | 30.5 dBm |
| Terminated Path | 18.5 dBm |
| Hot Switching | 30.5 dBm |
| Temperature | |
| Junction | 135°C |
| Storage | –65°C to +150°C |
| Reflow | 260°C |

[1] For power derating over frequency, see Figure 2 and Figure 3.

[2] For 105°C operation, the power handling degrades from the $T_{CASE}$ = 85°C specifications by 3 dB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JC}$ is the junction to case bottom (channel to package bottom) thermal resistance.

*Table 3. Thermal Resistance*

| Package Type | $\theta_{JC}$[1] | Unit |
|---|---|---|
| CC-24-14 | | |
| Through Path | 100 | °C/W |
| Terminated Path | 800 | °C/W |

[1] $\theta_{JC}$ was determined by simulation under the following conditions: the heat transfer is due solely to the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 105°C.

## ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

## ESD Ratings for the ADRF5048

*Table 4. ADRF5048, 24-Terminal LGA*

| ESD Model | Withstand Threshold (V) | Class |
|---|---|---|
| HBM | ±1000 for RFx Pins | 1C |
| | ±2000 for Supply and Digital Control Pins | 2 |
| CDM | ±500 for All Pins | C2A |

## POWER DERATING CURVES

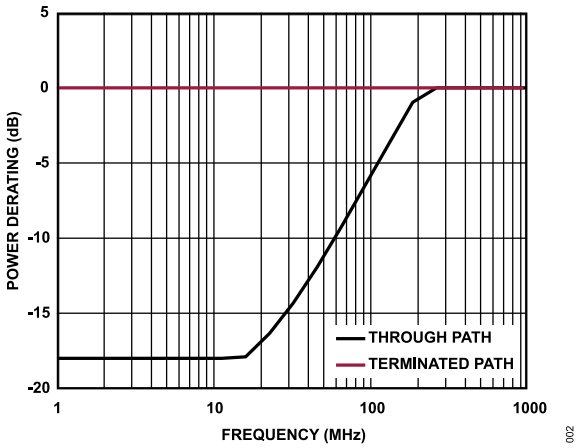


*Figure 2. Power Derating vs. Frequency, Low Frequency Detail, $T_{CASE}$ = 85°C*

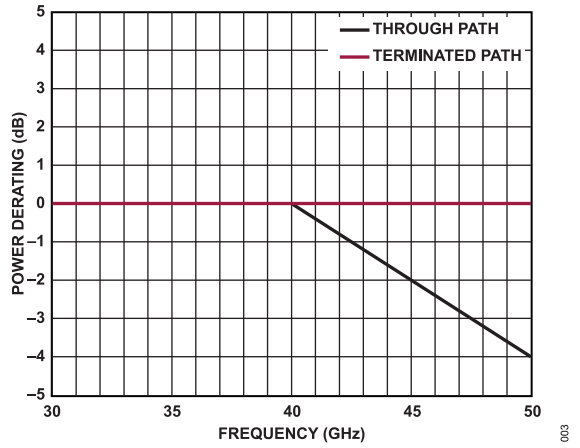


*Figure 3. Power Derating vs. Frequency, High Frequency Detail, $T_{CASE}$ = 85°C*

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device**. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

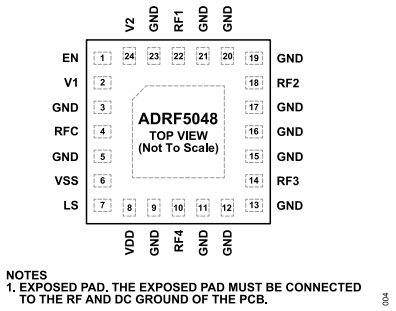


*Figure 4. Pin Configuration*

*Table 5. Pin Function Descriptions*

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | EN | Enable Input. See Table 6 for the truth table and Figure 7 for the control interface schematic. |
| 2 | V1 | Control Input 1. See Table 6 for the truth table and Figure 6 for the control interface schematic. |
| 3, 5, 9, 11 to 13, 15 to 17, 19 to 21, 23 | GND | Ground. |
| 4 | RFC | RF Common Port. The RFC pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Table 6 for the truth table and Figure 5 for the interface schematic. |
| 6 | VSS | Negative Supply Voltage. |
| 7 | LS | Logic Select. See Table 6 for the truth table and Figure 7 for the control interface schematic. |
| 8 | VDD | Positive Supply Voltage. |
| 10 | RF4 | RF Throw Port 4. The RF4 pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Table 6 for the truth table and Figure 5 for the interface schematic. |
| 14 | RF3 | RF Throw Port 3. The RF3 pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Table 6 for the truth table and Figure 5 for the interface schematic. |
| 18 | RF2 | RF Throw Port 2. The RF2 pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Table 6 for the truth table and Figure 5 for the interface schematic. |
| 22 | RF1 | RF Throw Port 1. The RF1 pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Table 6 for the truth table and Figure 5 for the interface schematic. |
| 24 | V2 | Control Input 2. See Table 6 for the truth table and Figure 6 for the control interface schematic. |
| | EPAD | Exposed Pad. The exposed pad must be connected to the RF and DC ground of the PCB. |

## INTERFACE SCHEMATICS

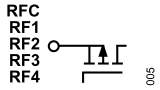


*Figure 5. RFx Interface Schematic*

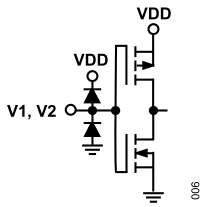


*Figure 6. V1 and V2 Control Interface Schematic*

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

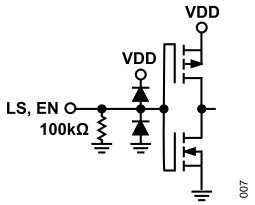


*Figure 7. LS and EN Control Interface Schematic*

## TYPICAL PERFORMANCE CHARACTERISTICS

### INSERTION LOSS, RETURN LOSS, AND ISOLATION

VDD = 3.3 V, VSS = −3.3 V, EN = 0 V, V1 = 0 V or 3.3 V, V2 = 0 V or 3.3 V, LS = 0 V or 3.3 V, and $T_{CASE}$ = 25°C on a 50 Ω system, unless otherwise noted.

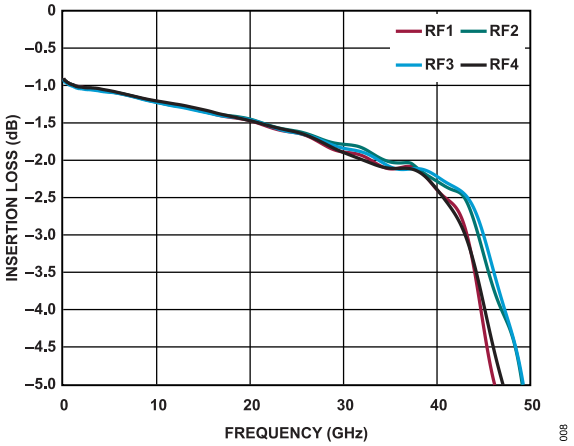


*Figure 8. Insertion Loss for RFC to RFx Selected vs. Frequency*

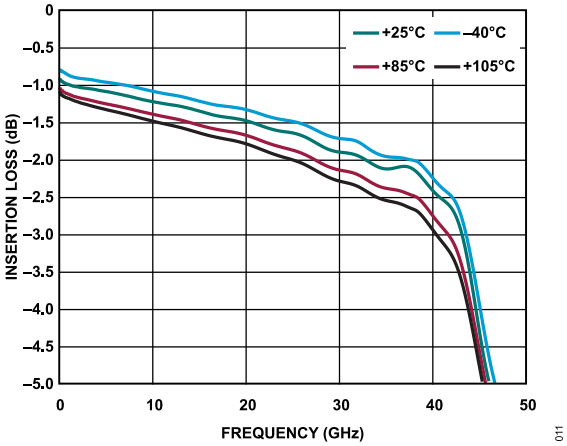


*Figure 11. Insertion Loss for RFC to RF1 vs. Frequency over Temperature*

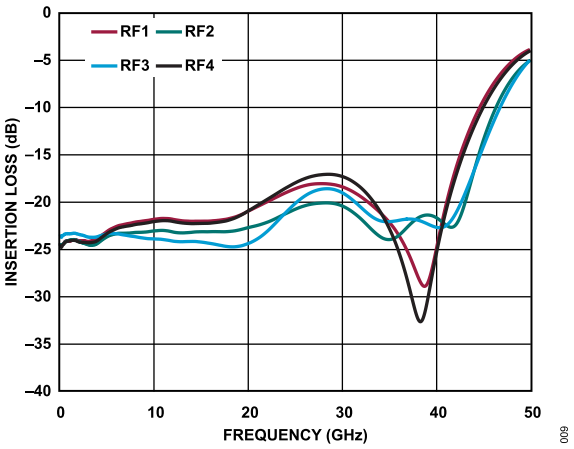


*Figure 9. Insertion Loss for RFC when RFx Selected vs. Frequency*

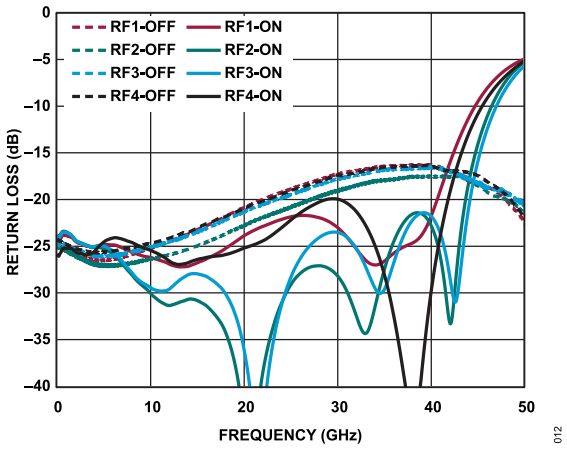


*Figure 12. Return Loss for RFx Unselected and Selected*

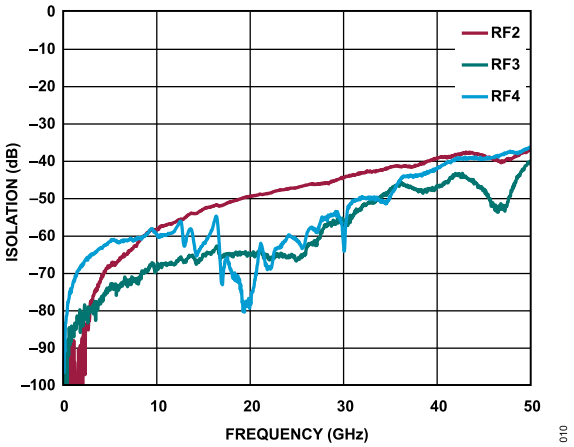


*Figure 10. RFC to RF2, RF3, and RF4 Isolation vs. Frequency, RF1 Selected*

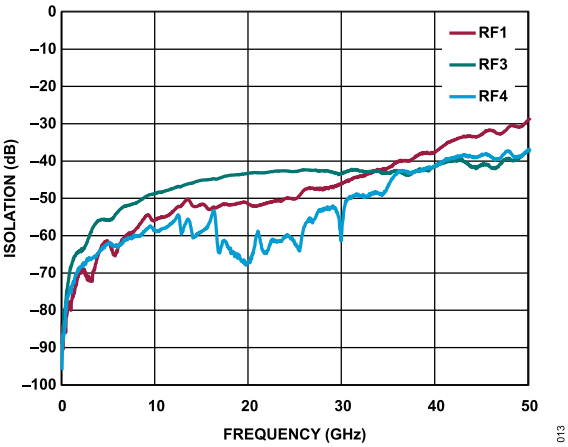


*Figure 13. RFC to RF1, RF3, and RF4 Isolation vs. Frequency, RF2 Selected*

## TYPICAL PERFORMANCE CHARACTERISTICS

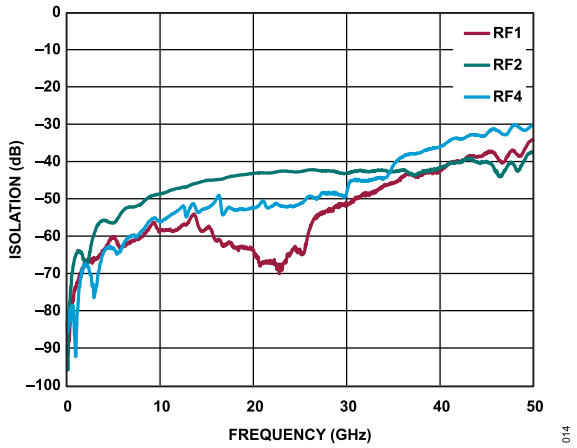


*Figure 14. RFC to RF1, RF2, and RF4 Isolation vs. Frequency, RF3 Selected*

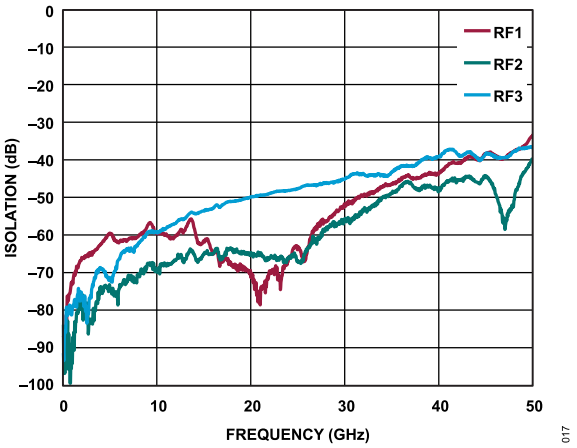


*Figure 17. RFC to RF1, RF2, and RF3 Isolation vs. Frequency, RF4 Selected*

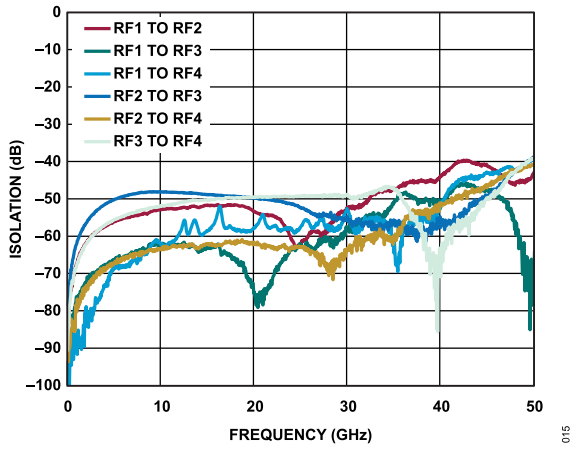


*Figure 15. Channel to Channel Isolation vs. Frequency, RFC to RF1 Path Selected*

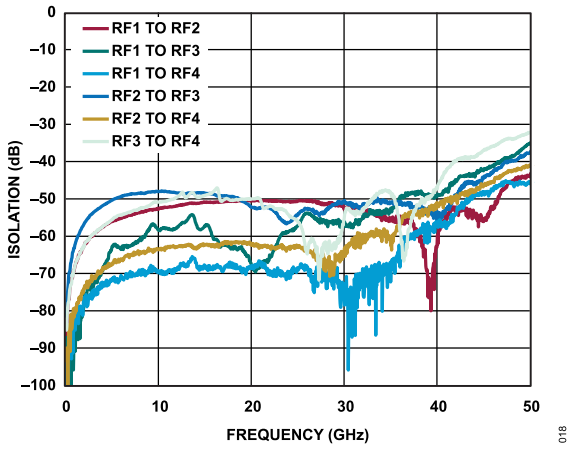


*Figure 18. Channel to Channel Isolation vs. Frequency, RFC to RF2 Path Selected*

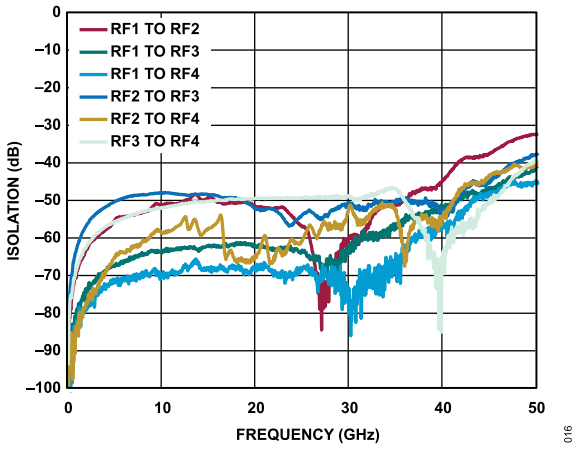


*Figure 16. Channel to Channel Isolation vs. Frequency, RFC to RF3 Path Selected*

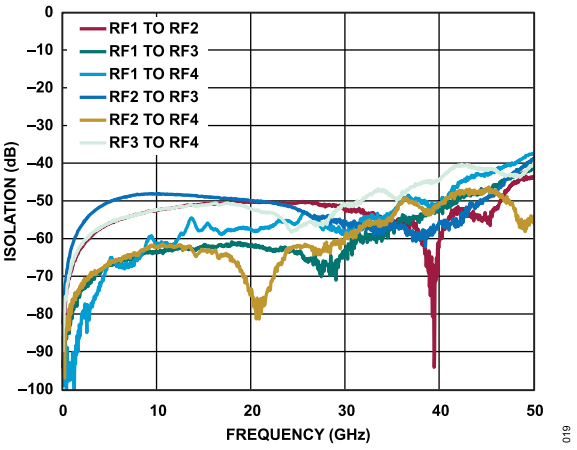


*Figure 19. Channel to Channel Isolation vs. Frequency, RFC to RF4 Path Selected*

## TYPICAL PERFORMANCE CHARACTERISTICS

### INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

VDD = 3.3 V, VSS = −3.3 V, EN = 0 V, V1 = 0 V or 3.3 V, V2 = 0 V or 3.3 V, LS = 0 V or 3.3 V, and $T_{CASE}$ = 25°C on a 50 Ω system, unless otherwise noted.

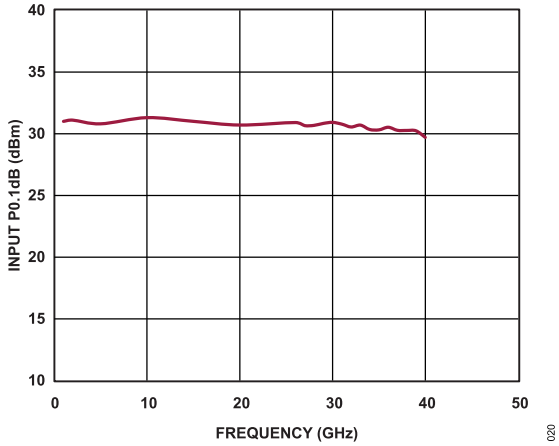


*Figure 20. Input P0.1dB vs. Frequency*

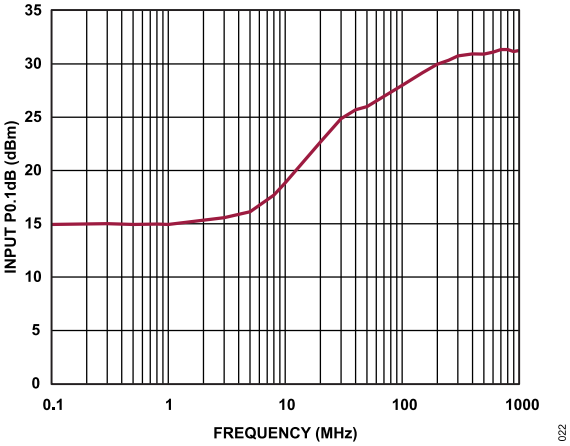


*Figure 22. Input P0.1dB vs. Frequency, Low Frequency Detail*

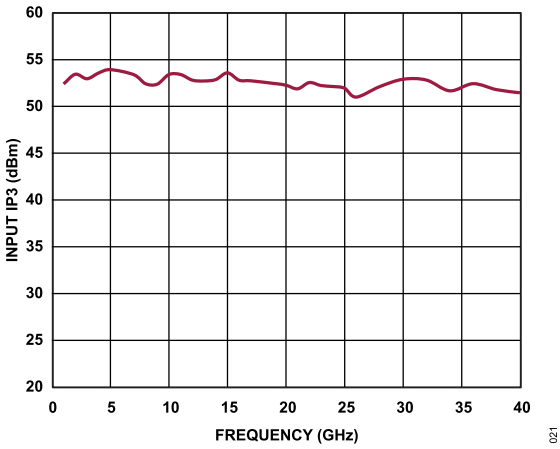


*Figure 21. Input IP3 vs. Frequency*

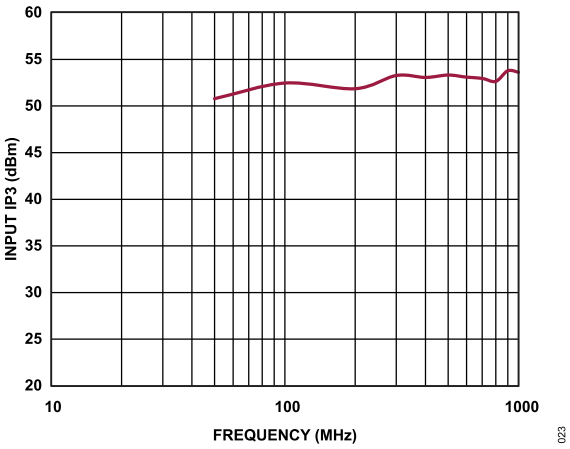


*Figure 23. Input IP3 vs. Frequency, Low Frequency Detail*

## THEORY OF OPERATION

The ADRF5048 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to minimize RF coupling.

All of the RF ports (RFC, RF1 to RF4) are DC-coupled to 0 V, and no DC blocking is required at the RFx ports when the RF line potential is equal to 0 V. The RF ports are internally matched to 50 Ω. Therefore, external matching networks are not required.

The ADRF5048 integrates a driver to perform logic functions internally and to provide the user with the advantage of a simplified CMOS-/LVTTL-compatible control interface. The driver features four digital control input pins (EN, LS, V1, and V2) that control the state of the RF paths (see Table 6).

The LS pin allows the user to define the control input logic sequence for the RF path selections. The logic level applied to the V1 and V2 pins determines which RF port is in the insertion loss state while the other three paths are in the isolation state.

When the EN pin is logic high, all four RF paths are in an isolation state regardless of the logic state of LS, V1, and V2. The RF ports are terminated to internal 50 Ω resistors, and RFC becomes reflective.

The insertion loss path conducts the RF signal between the selected RF throw port and the RF common port. The switch design is bidirectional with equal power handling capabilities. The RF input signal can be applied to the RFC port or the selected RF throw port. The isolation paths provide high loss between the insertion loss path and the unselected RF throw ports that are terminated to internal 50 Ω resistors.

The ideal power-up sequence is as follows:

1. Connect GND.
2. Power up VDD and VSS. Power up VSS after VDD to avoid current transients on VDD during ramp-up.
3. Apply the digital control inputs: EN, LS, V1, and V2. Applying digital control inputs before the VDD supply can inadvertently forward bias and damage the internal ESD protection structures. A series 1 kΩ resistor can be used to limit the current flowing into the digital control input pins in such cases. If the digital control input pins are not driven to a valid logic state (that is, the controller output is in high impedance state) after VDD is powered up, it is recommended to use pull-up and power-down resistors.
4. Apply an RF input signal.

The ideal power-down sequence is the reverse order of the power-up sequence.

*Table 6. Control Voltage Truth Table*

| Digital Control Inputs | | | | RFx Paths | | | |
|---|---|---|---|---|---|---|---|
| **EN** | **LS** | **V1** | **V2** | **RF1 to RFC** | **RF2 to RFC** | **RF3 to RFC** | **RF4 to RFC** |
| Low | Low | Low | Low | Insertion loss (on) | Isolation (off) | Isolation (off) | Isolation (off) |
| Low | Low | High | Low | Isolation (off) | Insertion loss (on) | Isolation (off) | Isolation (off) |
| Low | Low | Low | High | Isolation (off) | Isolation (off) | Insertion loss (on) | Isolation (off) |
| Low | Low | High | High | Isolation (off) | Isolation (off) | Isolation (off) | Insertion loss (on) |
| Low | High | Low | Low | Isolation (off) | Isolation (off) | Isolation (off) | Insertion loss (on) |
| Low | High | High | Low | Isolation (off) | Isolation (off) | Insertion loss (on) | Isolation (off) |
| Low | High | Low | High | Isolation (off) | Insertion loss (on) | Isolation (off) | Isolation (off) |
| Low | High | High | High | Insertion loss (on) | Isolation (off) | Isolation (off) | Isolation (off) |
| High | Low or high | Low or high | Low or high | Isolation (off) | Isolation (off) | Isolation (off) | Isolation (off) |

## APPLICATIONS INFORMATION

The ADRF5048 has two power supply pins (VDD and VSS) and four control pins (V1, V2, LS, and EN). Figure 24 shows the external components and connections for the supply and control pins. The VDD pin and the VSS pin are decoupled with a 100 pF multilayer ceramic capacitor. The ADRF5048 pinout allows the placement of the decoupling capacitors close to the device. No other external components are needed for bias and operation, except DC blocking capacitors on the RFx pins when the RF lines are biased at a voltage different than 0 V. Refer to Pin Configuration and Function Descriptions section for further details.

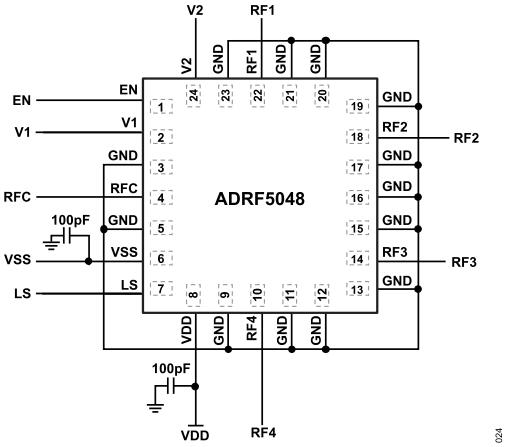


*Figure 24. Recommended Schematic*

## RECOMMENDATIONS FOR PCB DESIGN

The RF ports are matched to 50 Ω internally, and the pinout is designed to mate a coplanar waveguide (CPWG) with 50 Ω characteristic impedance on the PCB. Figure 25 shows the referenced CPWG RF trace design for an RF substrate with 8 mil thick Rogers RO4003 dielectric material. The RF trace with a 14 mil width and a 7 mil clearance is recommended for 2.2 mil finished copper thickness.

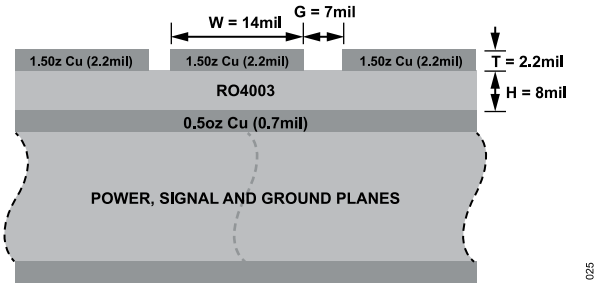


*Figure 25. Example PCB Stackup*

Figure 26 shows the routing of the RF traces, supply, and control signals from the ADRF5048. The ground planes are connected with as many filled through vias as allowed for optimal RF and thermal performance. The primary thermal path for the ADRF5048 is the bottom side.

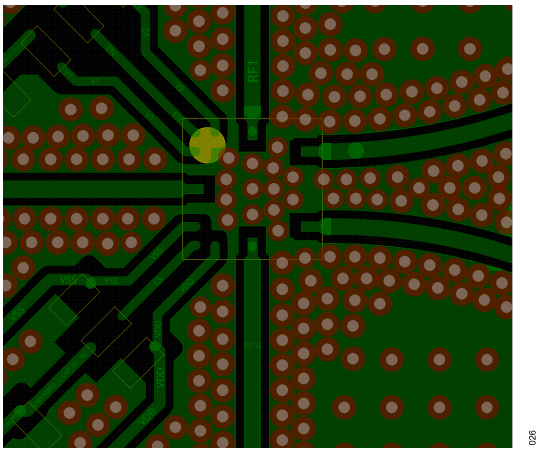


*Figure 26. PCB Routings*

Figure 27 shows the recommended layout from the device RFx pins to the 50 Ω CPWG on the referenced stackup. PCB pads are drawn 1:1 to the device pads. The ground pads are drawn solder mask defined, and the signal pads are drawn as pad defined. The RF trace from the PCB pad is extended with the same width until the package edge and tapered to the RF trace with a 45° angle. The paste mask is also designed to match the pad without any aperture reduction. The paste is divided into multiple openings for the paddle.

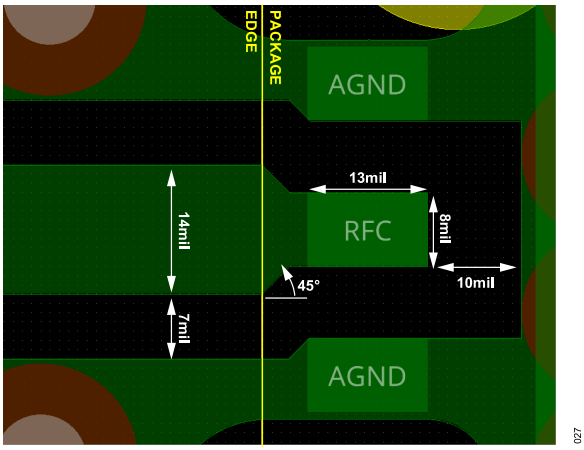


*Figure 27. Recommended RFx Pin Transitions*

For alternate PCB stackups with different dielectric thickness and CPWG design, contact Analog Devices, Inc., Technical Support Request for further recommendations.

## OUTLINE DIMENSIONS

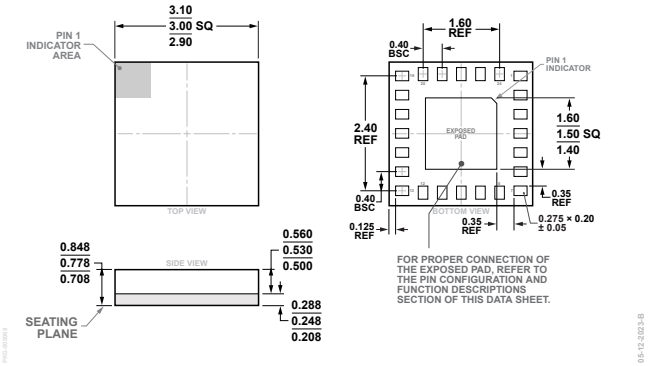


*Figure 28. 24-Terminal Land Grid Array [LGA]*
*(CC-24-14)*
*Dimensions shown in millimeters*

Updated: October 30, 2023

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Packing Quantity | Package Option |
|---|---|---|---|---|
| ADRF5048BCCZN | -40°C to +105°C | 24-Terminal LGA (3mm × 3mm w/ EP) | Reel, 500 | CC-24-14 |
| ADRF5048BCCZN-R7 | -40°C to +105°C | 24-Terminal LGA (3mm × 3mm w/ EP) | Reel, 500 | CC-24-14 |

[1] Z = RoHS Compliant Part.

## EVALUATION BOARDS

| Model[1] | Description |
|---|---|
| ADRF5048-EVALZ | Evaluation Board |

[1] Z = RoHS Compliant Part.