CGHV31500F1

2.7 – 3.1 GHz, 500 W GaN HPA

Description

The CGHV31500F1 is a 500W packaged transistor fully matched to 50 ohms at both input and output ports. Utilizing the high performance, 0.4um GaN on SiC production process, the CGHV31500F1 operates from 2.7 to 3.1 GHz and supports both defense and commercial-related s-band radar applications. The CGHV31500F1 typically achieves 500 W of saturated output power with 11 dB of large signal gain and 60% drain efficiency under long pulse operation.

Packaged in a thermally-enhanced, flange package, the CGHV31500F1 provides superior performance under long pulse operation allowing customers to improve SWaP-C benchmarks in their next-generation systems.

Figure 1. CGHV31500F1

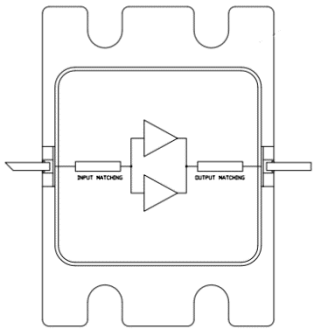


Figure 2. Functional Block Diagram

Features

- Psat: 500 W
- DE: 60 %
- LSG: 11 dB
- S21: 13 dB
- S11: -5 dB
- S22: -6 dB
- Long pulse operation

Note: Features are typical performance under 25°C, pulsed operation. Please reference performance charts for additional information.

Applications

- S-band Radar

RoHS compliant

Absolute Maximum Ratings

Parameter	Symbol	Units	Value	Conditions
Drain to Source Voltage	V_{DSS}	V	150	25 °C
Drain Voltage	V_D	V	50	25 °C
Gate Voltage	V_G	V	-10, +2	25 °C
Drain Current	I_D	A	24	25 °C
Gate Current	I_G	mA	80	25 °C
Input Power	P_{in}	dBm	48	25 °C
Storage Temperature	T_{stg}	°C	-55, +150	
Mounting Temperature	T_J	°C	320	30 seconds
Junction Temperature	T_J	°C	225	MTTF > 1E6 Hours
Output Mismatch Stress	VSWR	Ψ	5:1	
Pulse Width/Duty Cycle		us/%	2000/20	

Recommended Operating Conditions

Parameter	Symbol	Units	Typical Value	Conditions
Drain Voltage	Vd	V	50	Pulsed only
Gate Voltage	Vg	V	-2.7	
Drain Current	Idq	mA	500	
Input Power	Pin	dBm	46	
Case Temperature	Tcase	°C	-40 to 55	

RF Specifications

Test conditions unless otherwise noted: Vd=50 V, Idq=0.5A, PW=2000uS, DC=20%, Pin = 46 dBm, T_{base}=25 °C, Frequency: 2.9GHz

Parameter	Units	Frequency	Min	Typical	Max	Conditions
Frequency	GHz		2.7		3.1	
Output Power	dBm	2.7		57		
		2.9		58		
		3.1		57		
Power-added Efficiency	%	2.7		65		
		2.9		60		
		3.1		58		
LSG	dB	2.7		11		
		2.9		11		
		3.1		10		
Small-Signal Gain (S21)	dB	2.7		16		Pin = -20 dBm
		2.9		15		
		3.1		13		
Input Return Loss	dB			-5		Pin = -20 dBm
Output Return Loss	dB			-6		Pin = -20 dBm

Test conditions unless otherwise noted: Vd=50 V, Idq=0.5A, **PW=2000uS, DC=20%**, Pin = 46 dBm, T_{base}=25°C, Frequency: 2.9GHz

Figure 3: Pout v. Frequency v. Temperature

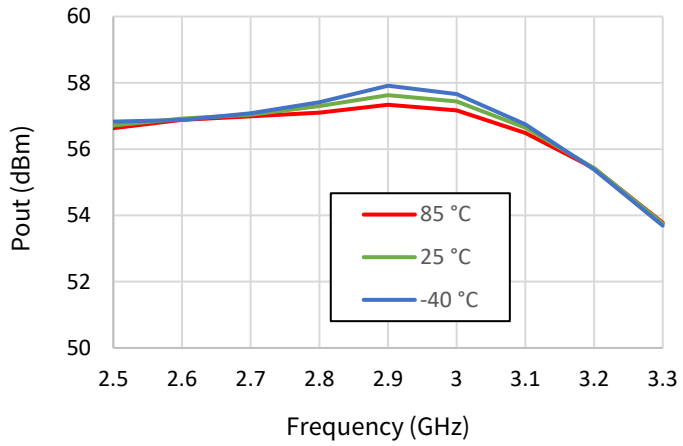


Figure 4: DE v. Frequency v. Temperature

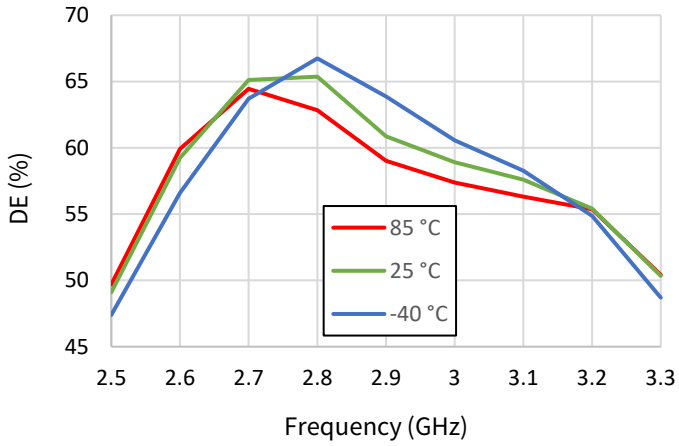


Figure 5: Id v. Frequency v. Temperature

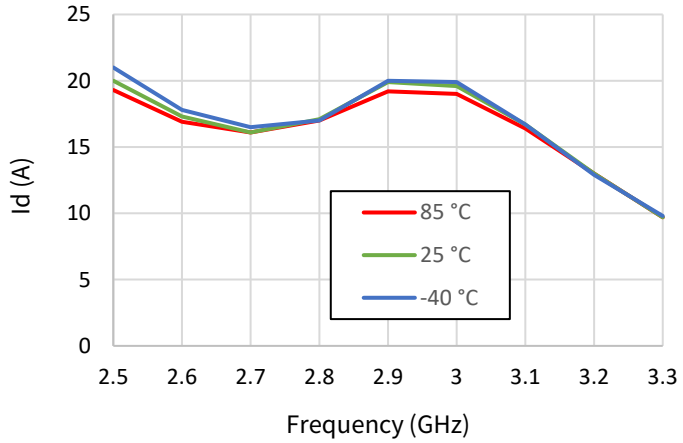


Figure 6: Ig v. Frequency v. Temperature

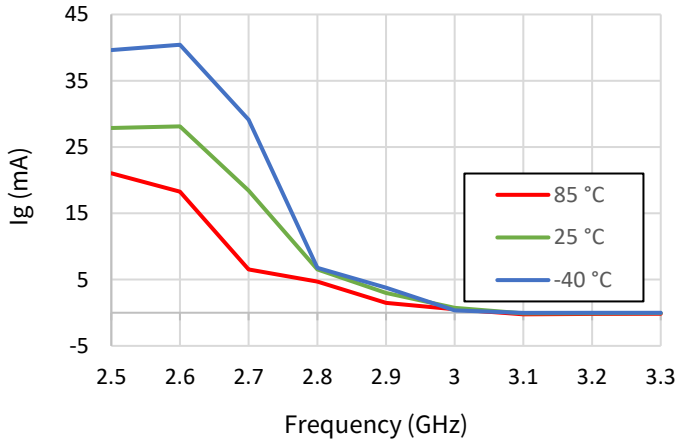
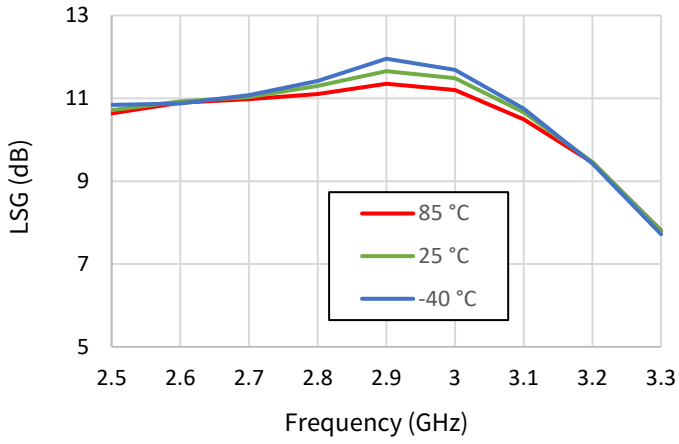


Figure 7: LSG v. Frequency v. Temperature



Test conditions unless otherwise noted: Vd=50 V, Idq=0.5A, PW=2000uS, DC=20%, Pin = 46 dBm, T_{base}=25 °C, Frequency: 2.9GHz

Figure 8: Pout v. Frequency v. Vd

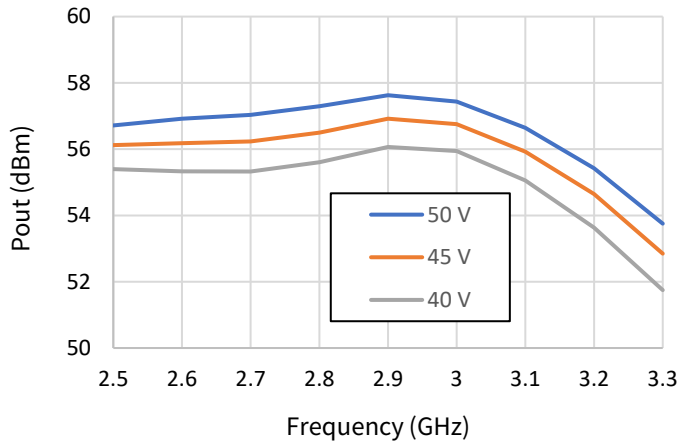


Figure 9: DE v. Frequency v. Vd

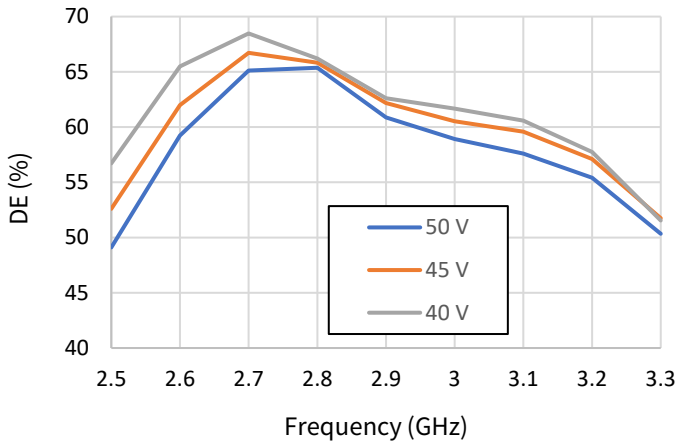


Figure 10: Id v. Frequency v. Vd

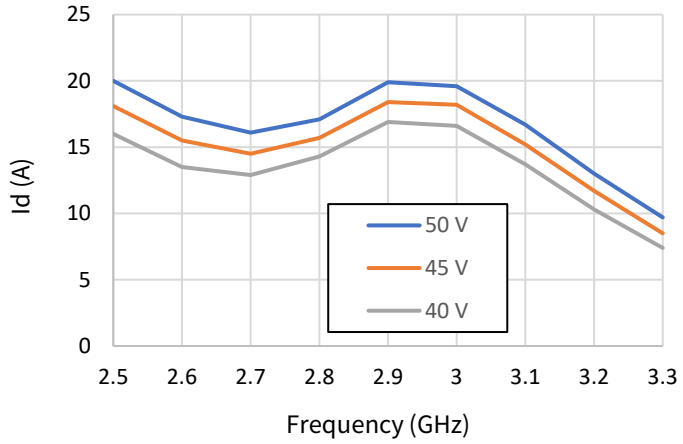


Figure 11: Ig v. Frequency v. Vd

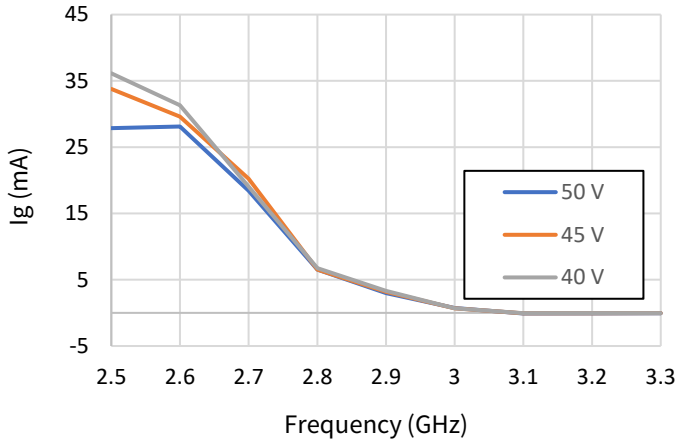
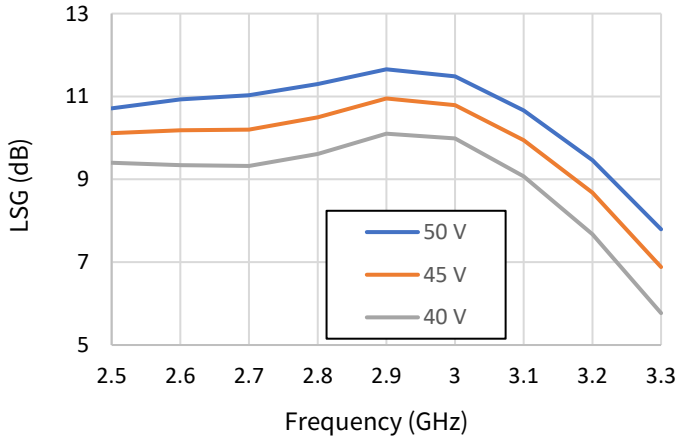


Figure 12: LSG v. Frequency v. Vd



Test conditions unless otherwise noted: Vd=50 V, Idq=0.5A, PW=2000uS, DC=20%, Pin = 46 dBm, T_{base}=25 °C, Frequency: 2.9GHz

Figure 13: Pout v. Frequency v. Idq

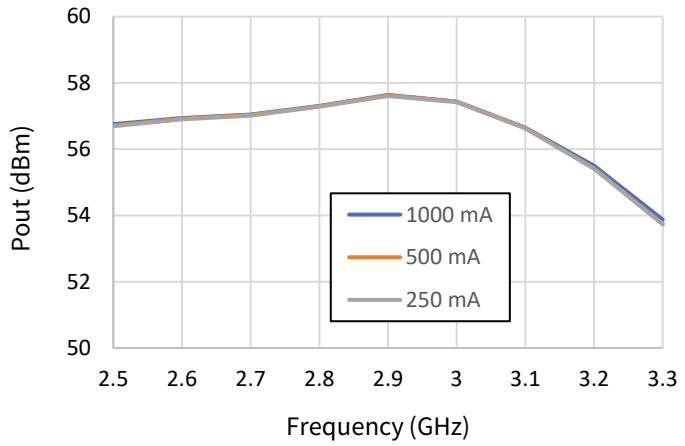


Figure 14: DE v. Frequency v. Idq

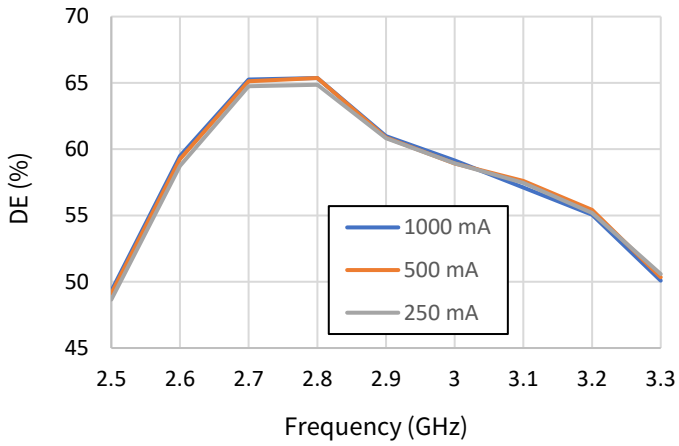


Figure 15: Id v. Frequency v. Idq

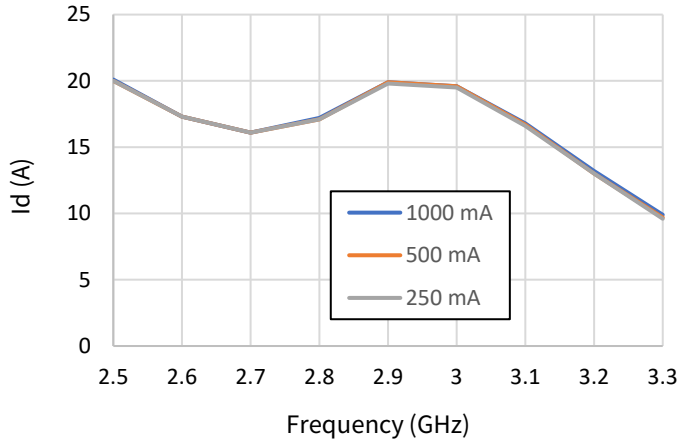


Figure 16: Ig v. Frequency v. Idq

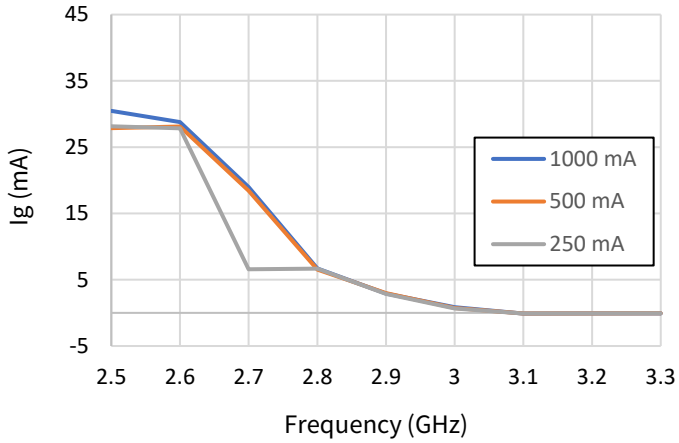
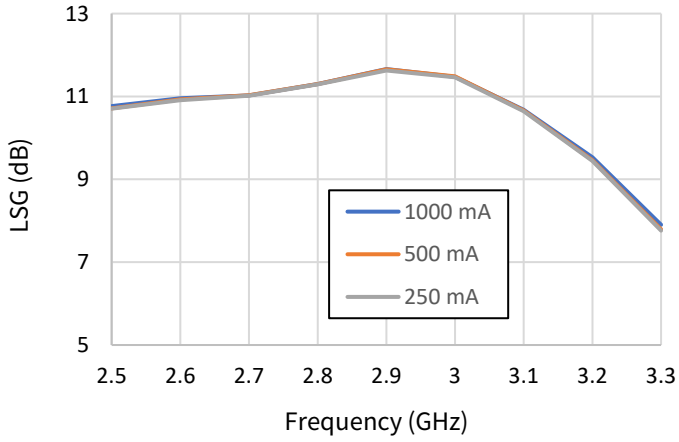


Figure 17: LSG v. Frequency v. Idq



Test conditions unless otherwise noted: Vd=50 V, Idq=0.5A, PW=2000uS, DC=20%, Pin = 46 dBm, T_{base}=25 °C, Frequency: 2.9GHz

Figure 18: Pout v. Pin v. Frequency

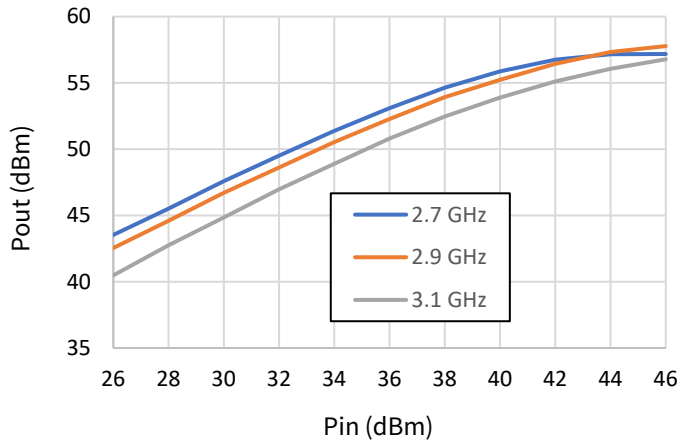


Figure 19: DE v. Pin v. Frequency

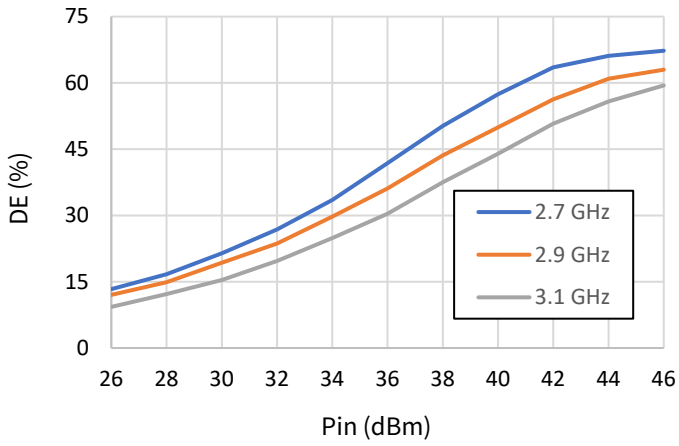


Figure 20: Id v. Pin v. Frequency

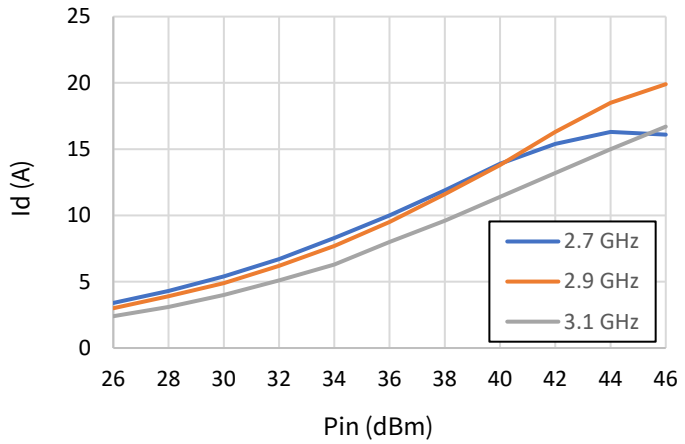


Figure 21: Ig v. Pin v. Frequency

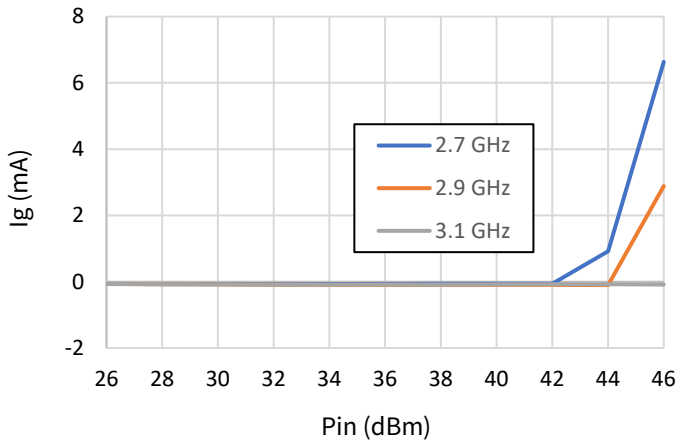
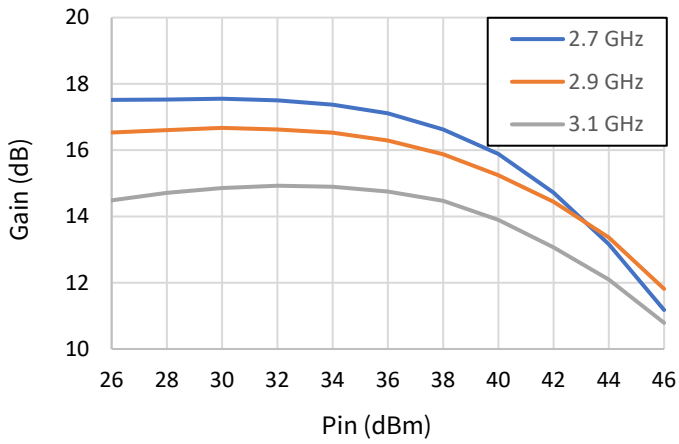


Figure 22: Gain v. Pin v. Frequency



Test conditions unless otherwise noted: Vd=50 V, Idq=0.5A, PW=2000uS, DC=20%, Pin = 46 dBm, T_{base}=25 °C, Frequency: 2.9GHz

Figure 23: Pout v. Pin v. Temperature

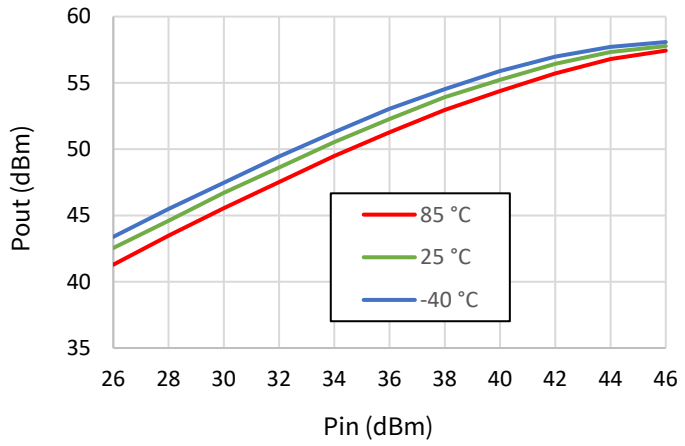


Figure 24: DE v. Pin v. Temperature

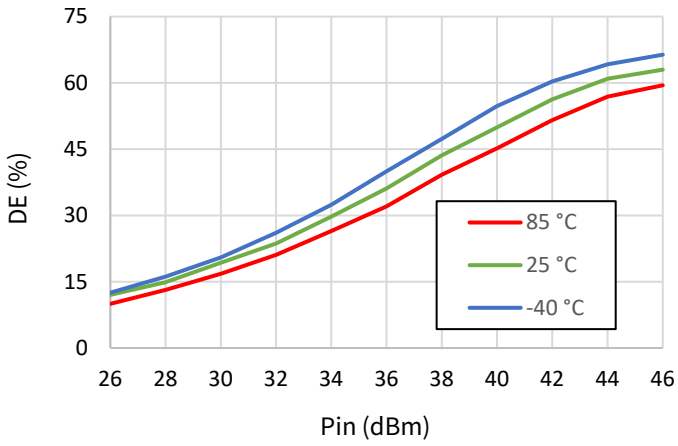


Figure 25: Id v. Pin v. Temperature

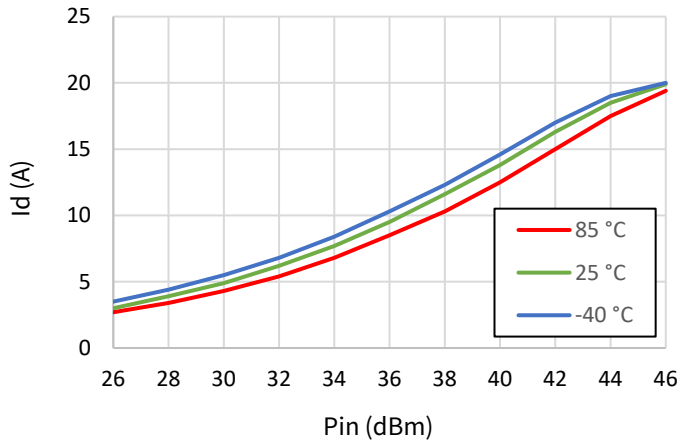


Figure 26: Ig v. Pin v. Temperature

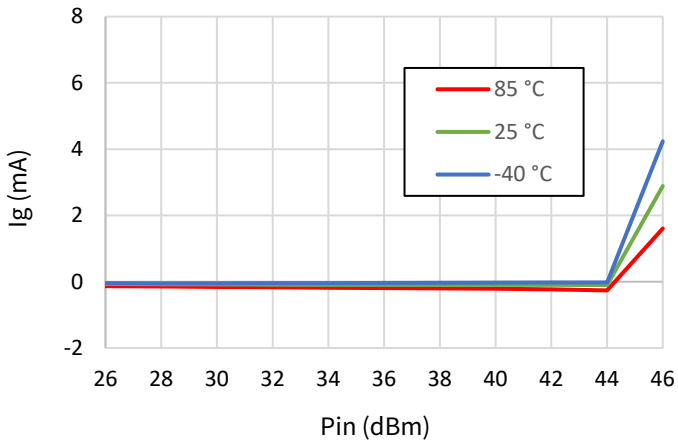
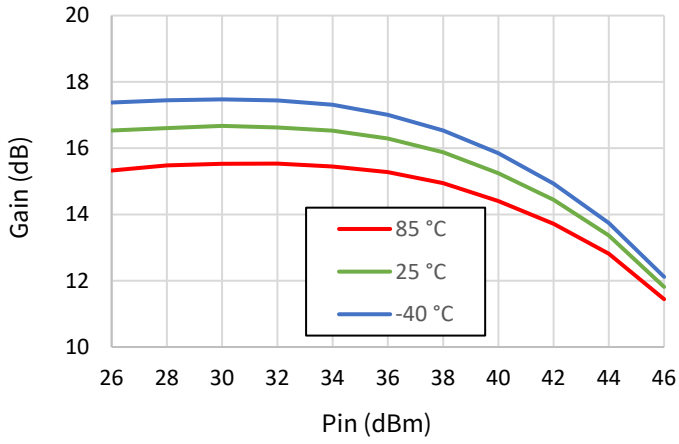


Figure 27: Gain v. Pin v. Temperature



Test conditions unless otherwise noted: Vd=50 V, Idq=0.5A, PW=2000uS, DC=20%, Pin = 46 dBm, T_{base}=25 °C, Frequency: 2.9GHz

Figure 28: Pout v. Pin v. Vd

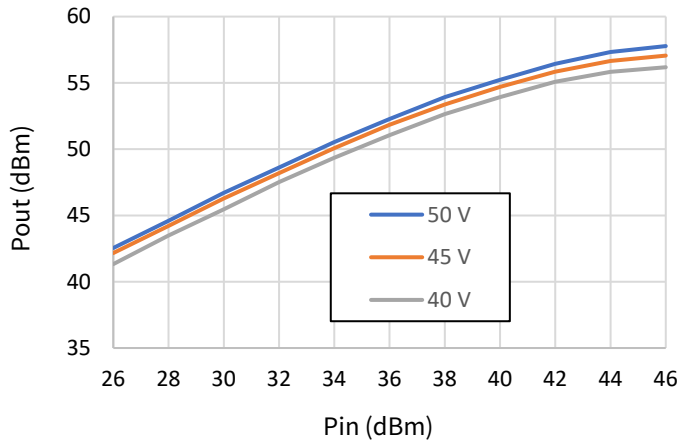


Figure 29: DE v. Pin v. Vd

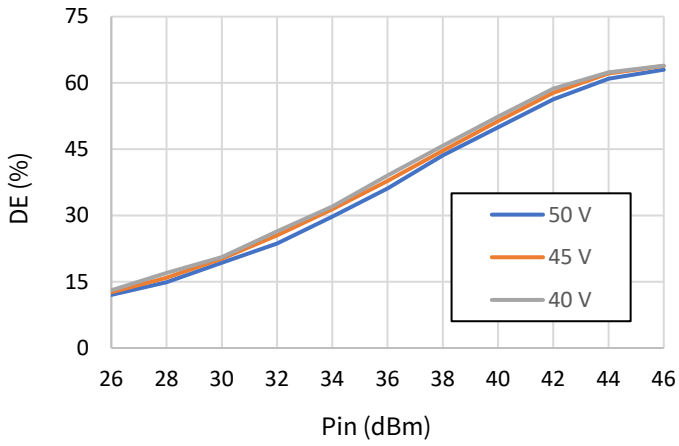


Figure 30: Id v. Pin v. Vd

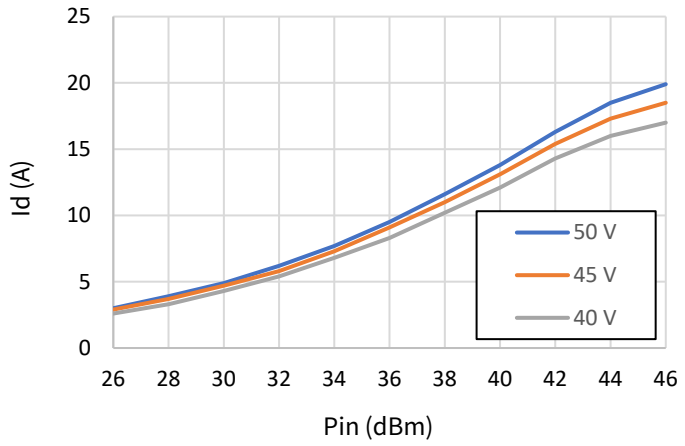


Figure 31: Ig v. Pin v. Vd

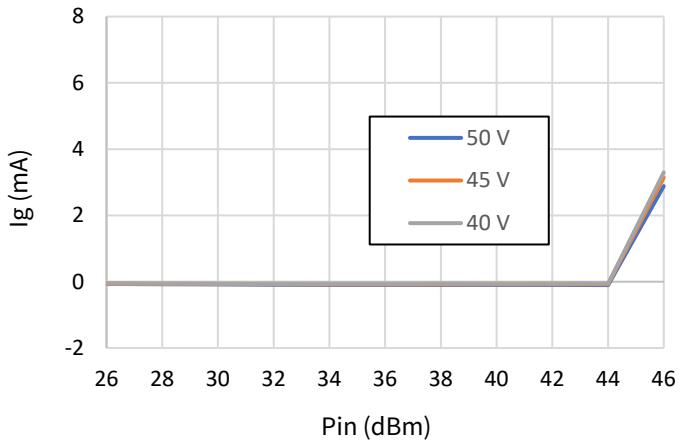
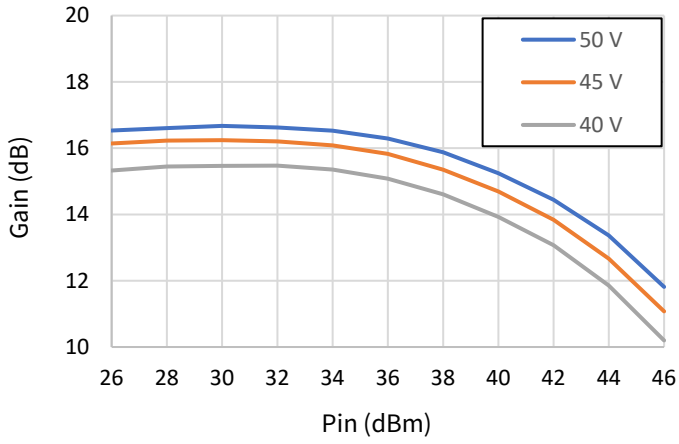


Figure 32: Gain v. Pin v. Vd



Test conditions unless otherwise noted: Vd=50 V, Idq=0.5A, PW=2000uS, DC=20%, Pin = 46 dBm, T_{base}=25 °C, Frequency: 2.9GHz

Figure 33: Pout v. Pin v. Idq

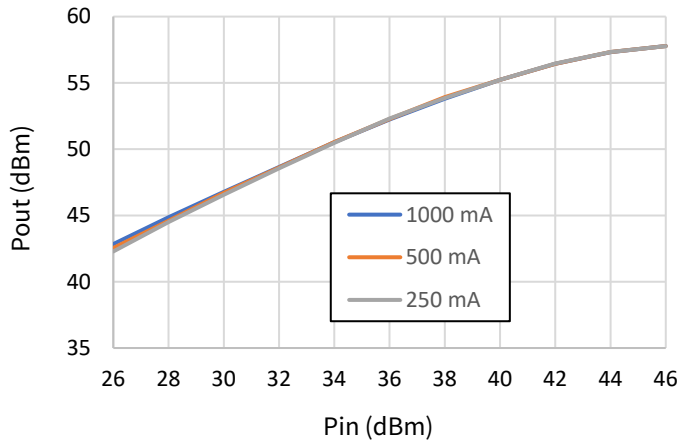


Figure 34: DE v. Pin v. Idq

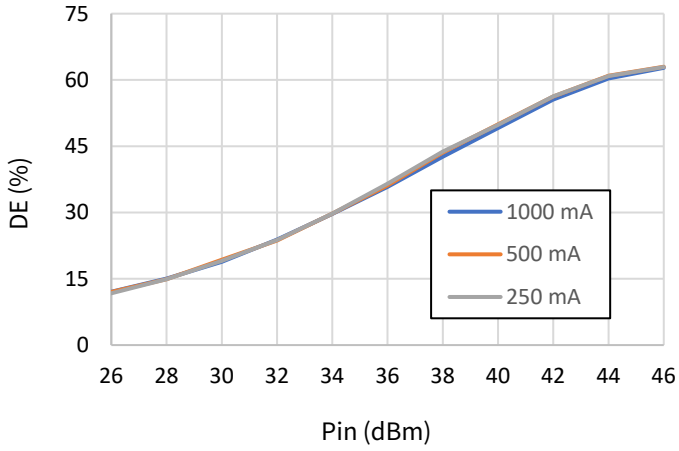


Figure 35: Id v. Pin v. Idq

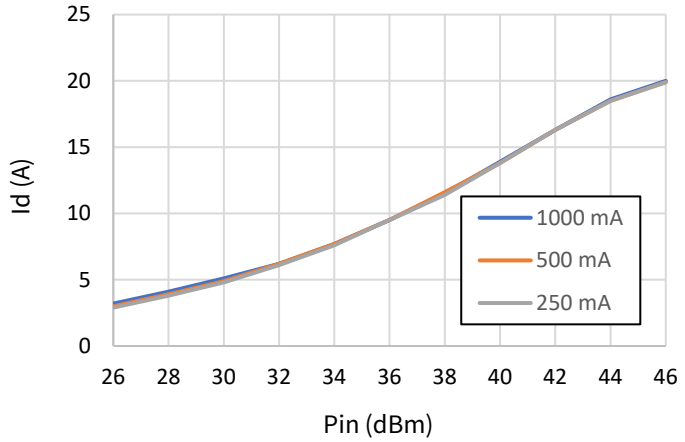


Figure 36: Ig v. Pin v. Idq

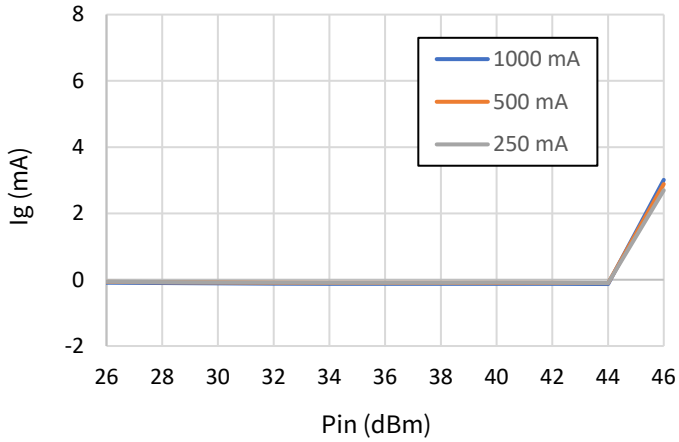
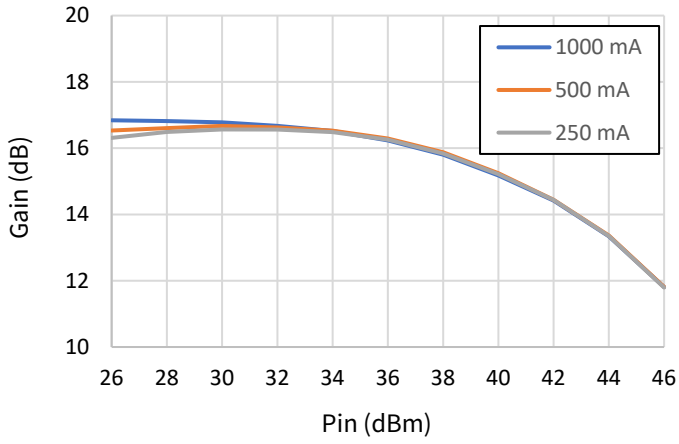


Figure 37: Gain v. Pin v. Idq



Test conditions unless otherwise noted: Vd=50V, Idq= 500mA, Pin = -20dBm, T_{base}=25 °C

Figure 38: S21 v. Frequency v. Temperature

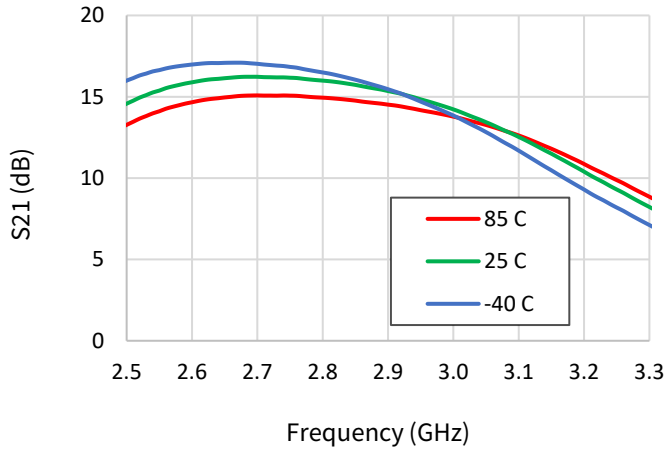


Figure 39: S21 v. Frequency v. Vd

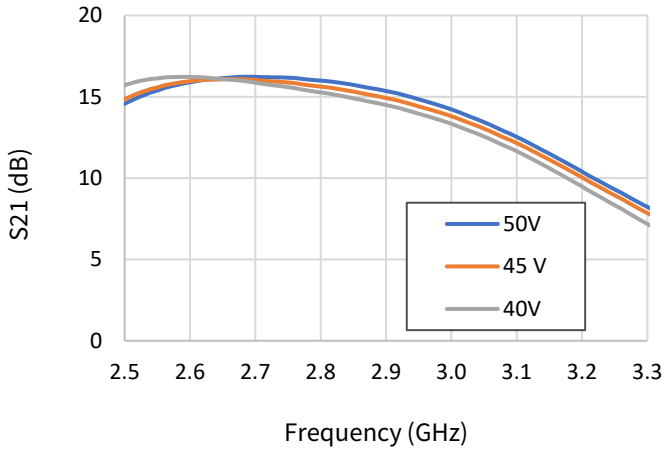


Figure 40: S11 v. Frequency v. Temperature

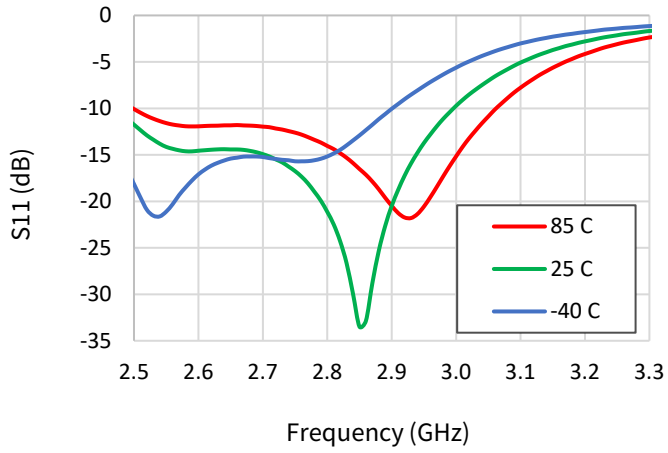


Figure 41: S11 v. Frequency v. Vd

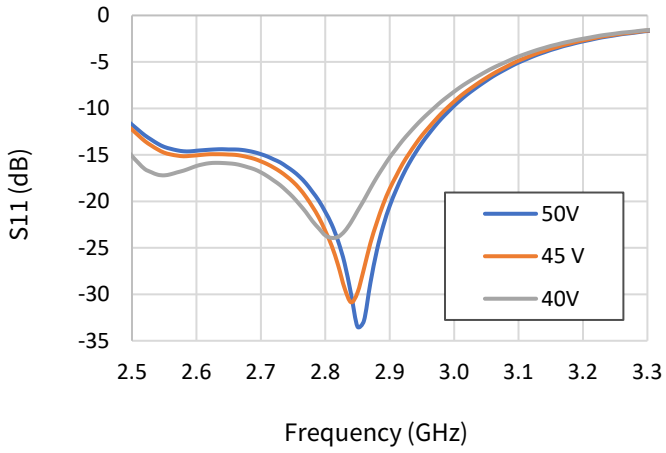


Figure 42: S22 v. Frequency v. Temperature

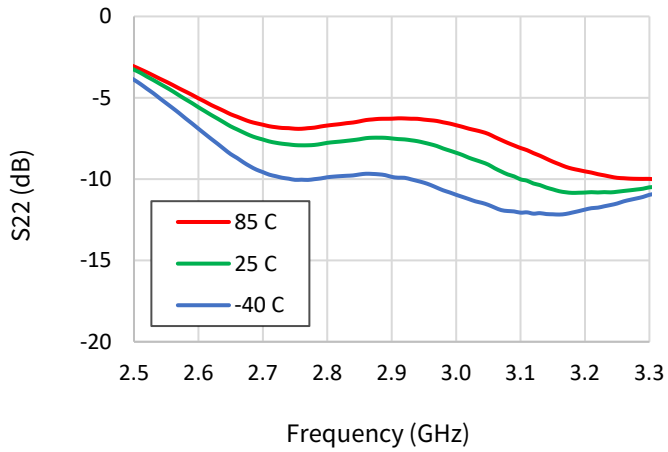
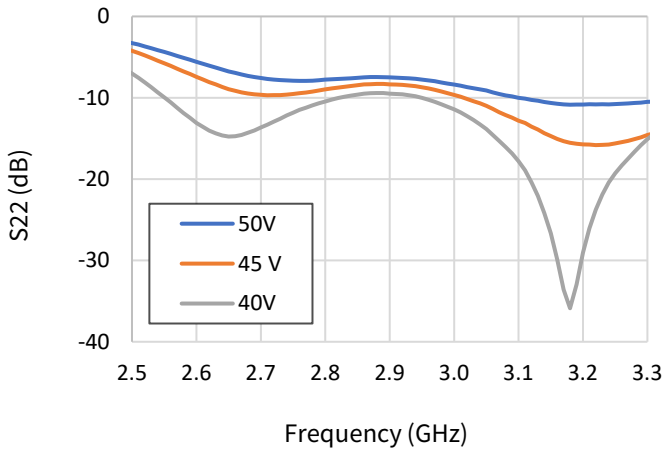


Figure 43: S22 v. Frequency v. Vd



Test conditions unless otherwise noted: Vd=50V, Idq= 500mA, Pin = -20dBm, T_{base}=25 °C

Figure 44: S21 v. Frequency v. Idq

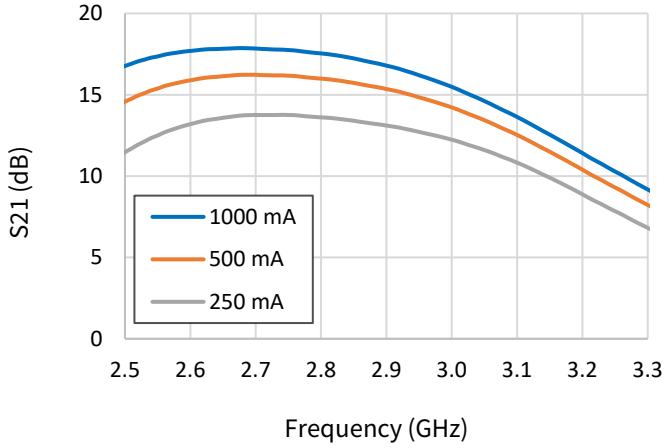


Figure 45: S11 v. Frequency v. Idq

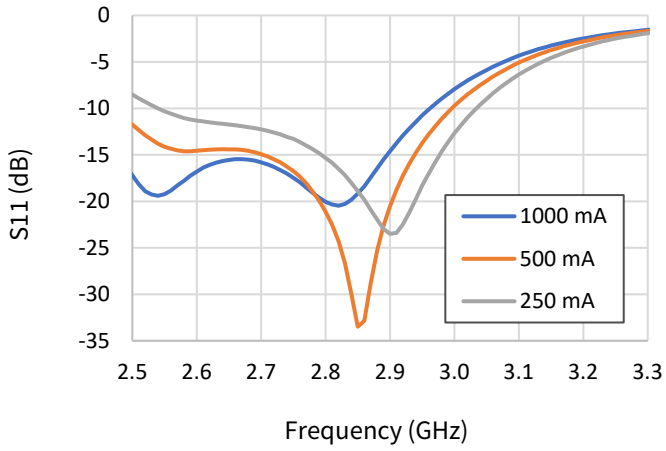
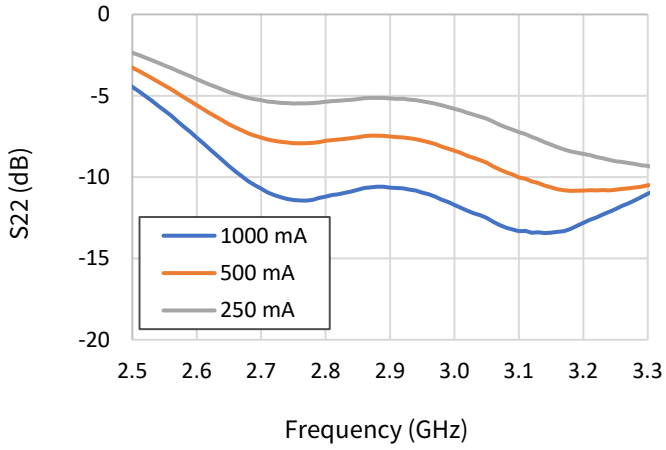


Figure 46: S22 v. Frequency v. Idq



Test conditions unless otherwise noted: Vd=50V, Idq= 500mA, PW=2000uS, DC=20%, Pin = 46dBm, T_{base}=25 °C
Frequency 1= 2.7 GHz, Frequency 2 = 2.9 GHz, Frequency 3 = 3.1 GHz, T_{base}=25 °C

Figure 47: 2f v. Pout v. Temperature, F1

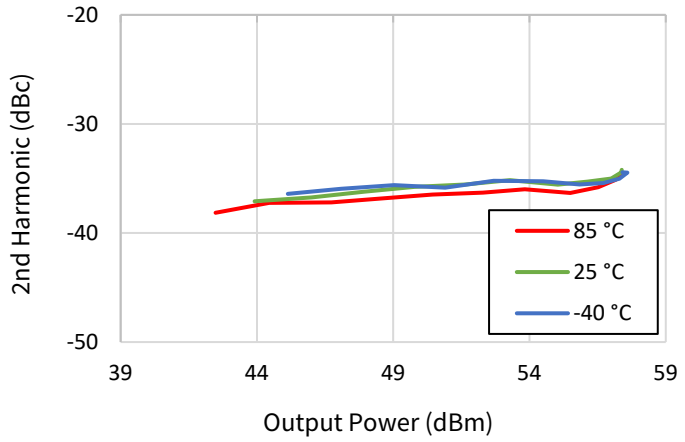


Figure 48: 2f v. Pout v. Vd, F1

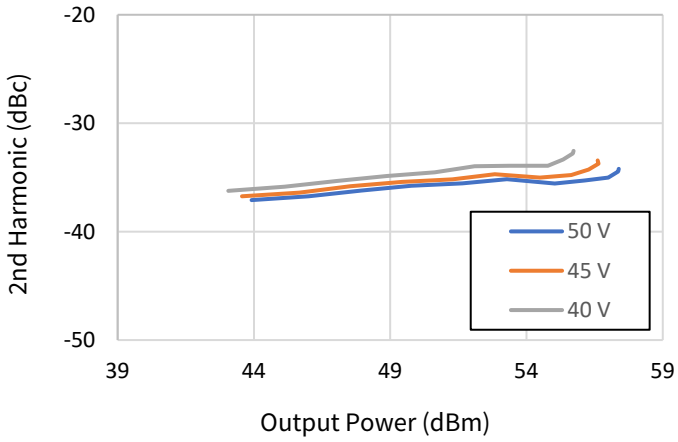


Figure 49: 2f v. Pout v. Temperature, F2

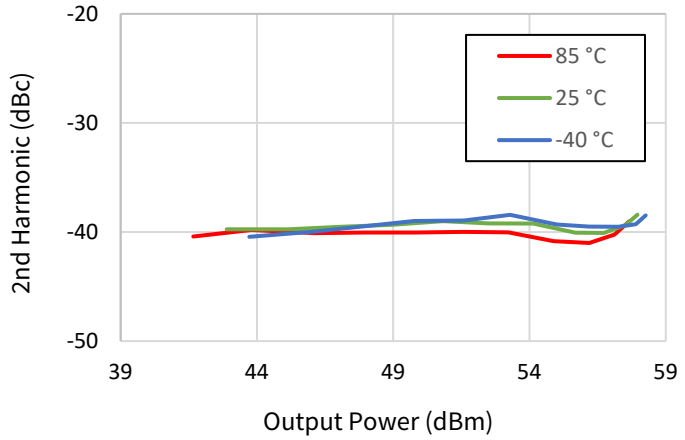


Figure 50: 2f v. Pout v. Vd, F2

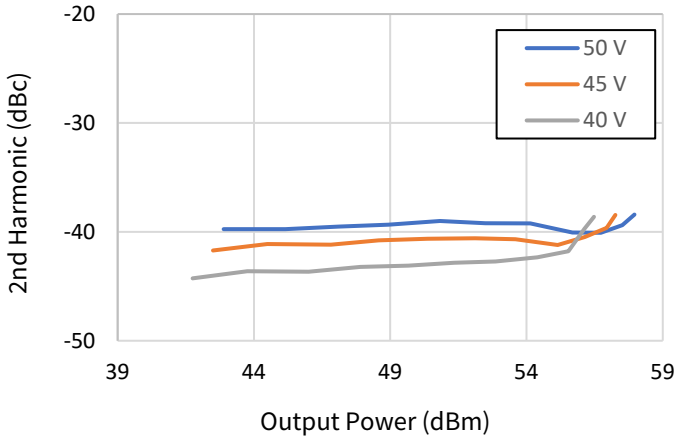


Figure 51: 2f v. Pout v. Temperature, F3

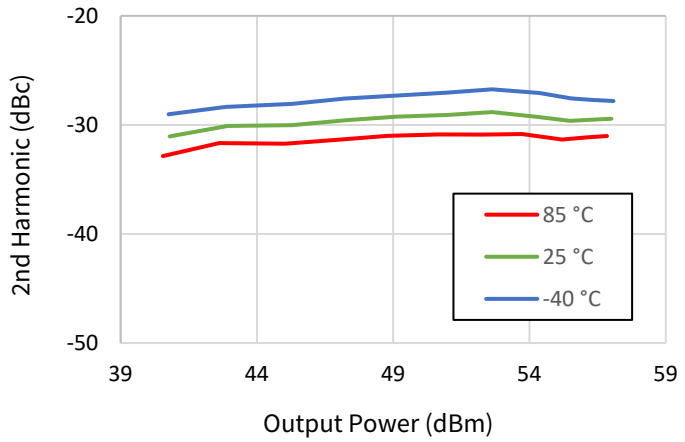
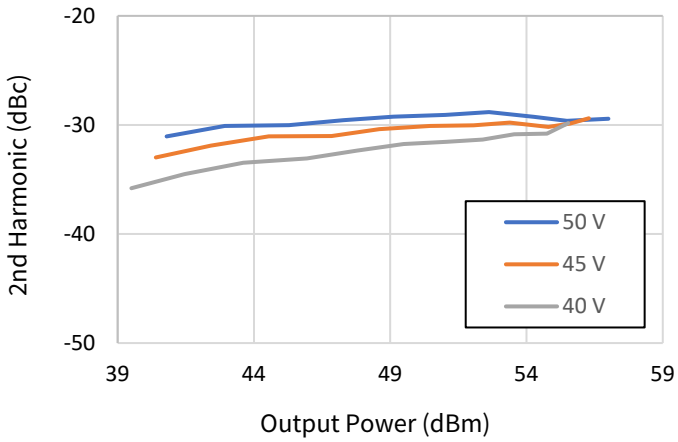


Figure 52: 2f v. Pout v. Vd, F3



Test conditions unless otherwise noted: Vd=50 V, Idq=0.5A, **PW=100uS, DC = 10%,** Pin = 46 dBm, T_{base}=25 °C, Frequency: 2.9GHz

Figure 53: Pout v. Frequency v. Temperature

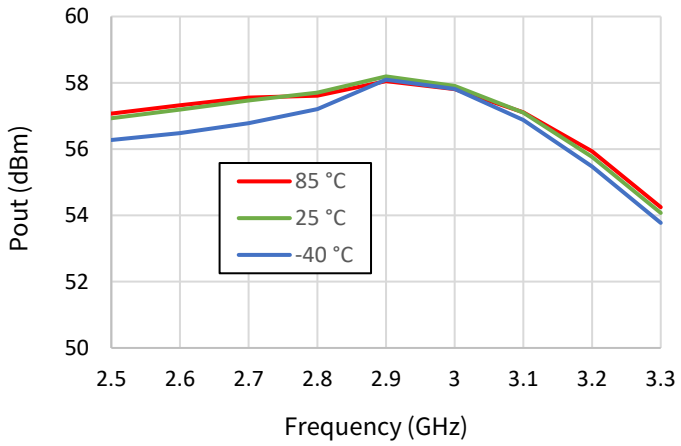


Figure 54: DE v. Frequency v. Temperature

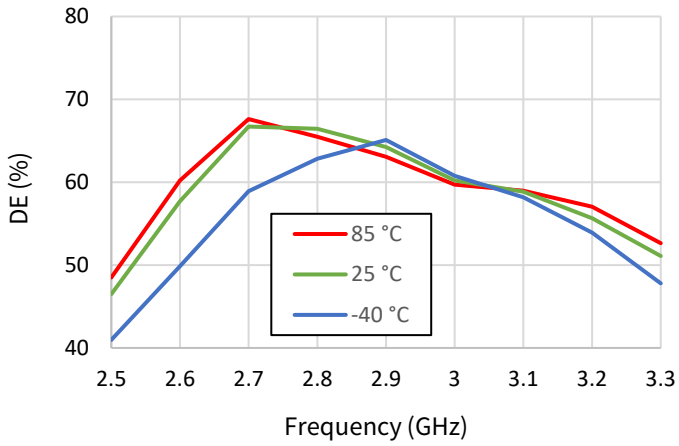


Figure 55: Id v. Frequency v. Temperature

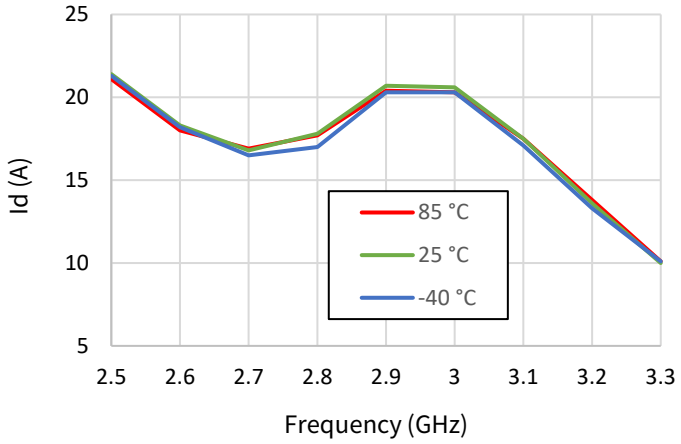


Figure 56: Ig v. Frequency v. Temperature

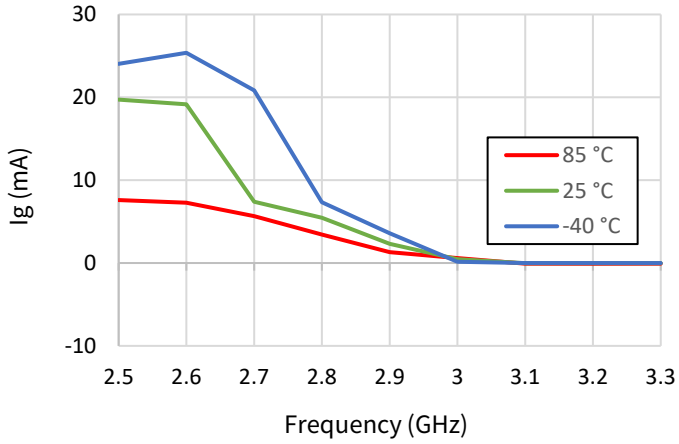
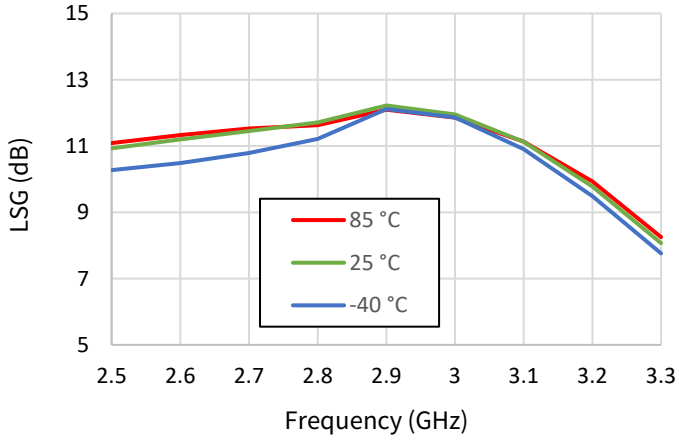


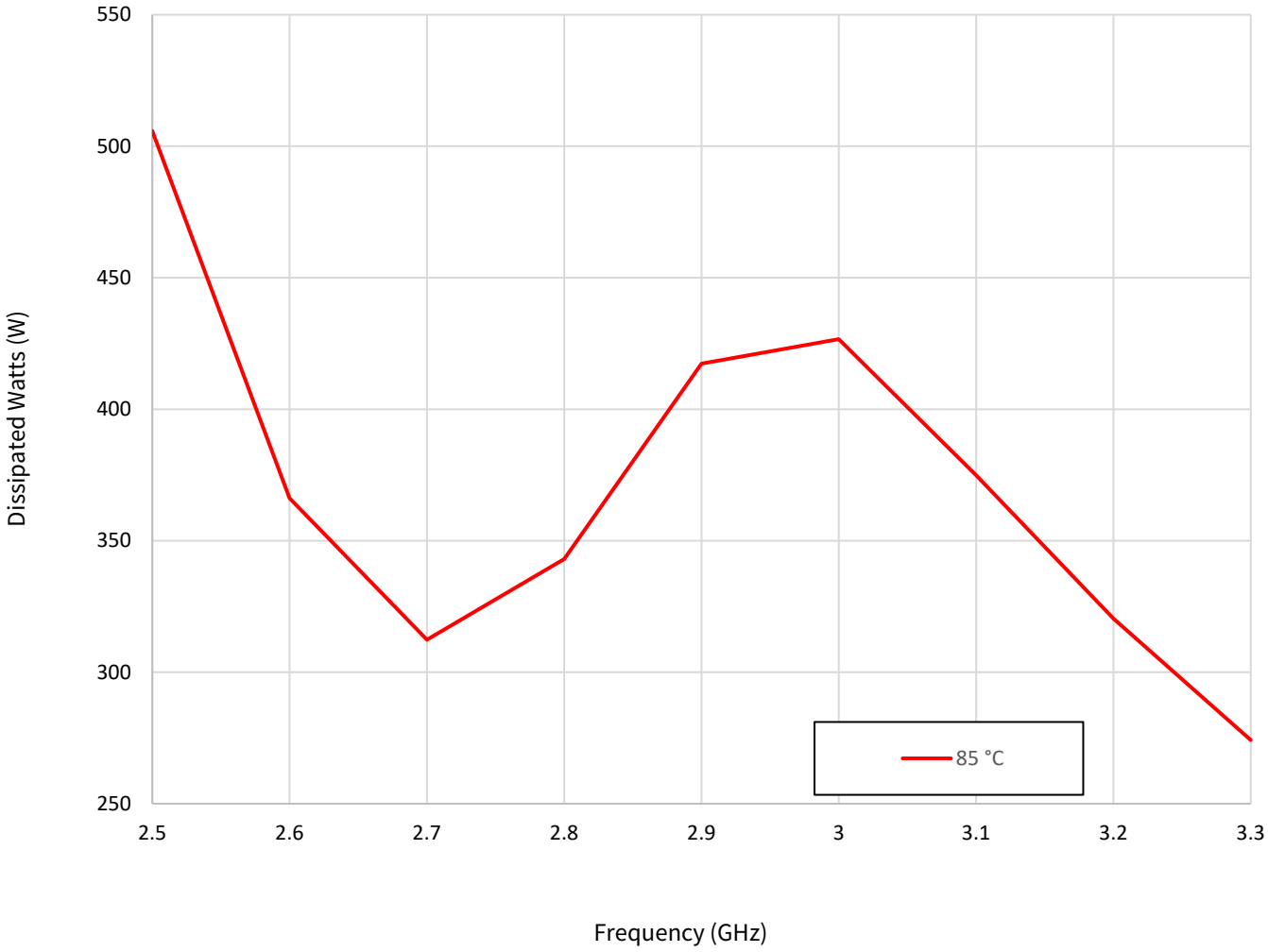
Figure 57: LSG v. Frequency v. Temperature



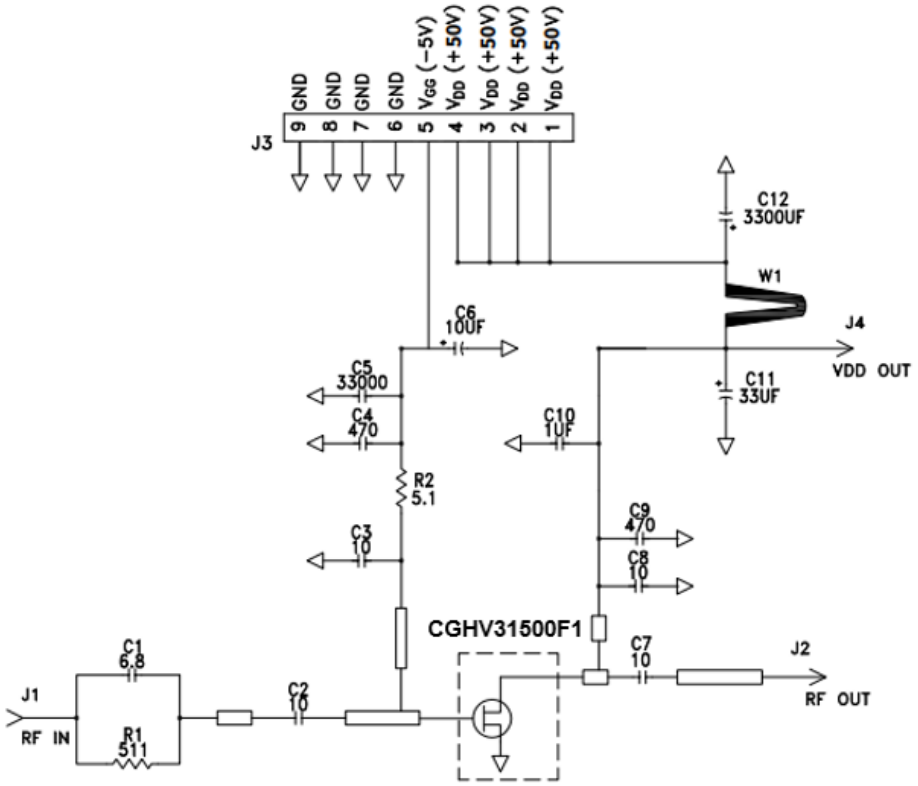
Thermal Characteristics

Parameter	Symbol	Value	Operating Conditions
Operating Junction Temperature	T_J	251.92	Freq = 2.9 GHz, V_d = 50 V, I_{dq} = 500 mA, I_{drive} = 19.4 A, P_{in} = 46 dBm, P_{out} = 57.43 dBm, P_{diss} = 417.3 W, T_{case} = 85 C, PW = 2000uS, DC = 20%
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.4	

Power Dissipation v. Frequency (Tcase = 85°C)



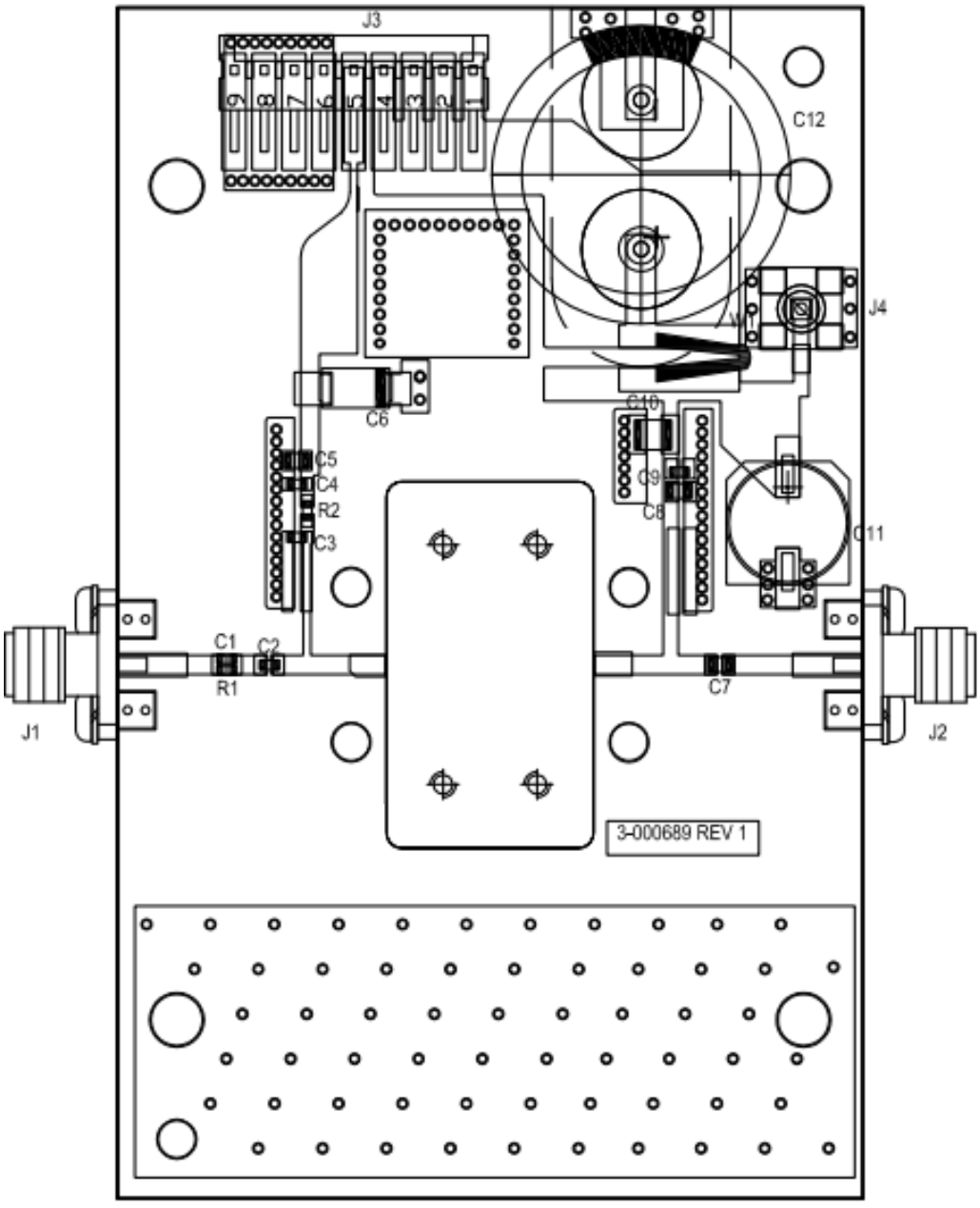
CGHV31500F1-AMP Evaluation Board Schematic Drawing



CGHV31500F1-AMP Evaluation Board Bill of Materials

Reference Designator	Description	Qty
R1	RES, 511, OHM, +/- 1%, 1/16W, 0603	1
R2	RES, 5.1, OHM, +/- 1%, 1/16W, 0603	1
C1	CAP, 6.8pF, +/-0.25%, 250V, 0603	1
C2, C7, C8	CAP, 10.0pF, +/-1%, 250V, 0805	3
C3	CAP, 10.0pF, +/-5%, 250V, 0603	1
C4, C9	CAP, 470pF, 5%, 100V, 0603, X	2
C5	CAP, 33000 pF, 0805, 100V, X7R	1
C6	CAP, 10uF 16V TANTALUM	1
C10	CAP, 1.0uF, 100V, 10%, X7R, 1210	1
C11	CAP, 33uF, 20%, G CASE	1
C12	CAP, 3300uF, +/-20%, 100V, ELECTROLYTIC	1
J1, J2	CONN, SMA, PANEL MOUNT JACK, FL	2
J3	HEADER, RT>PLZ, 0.1CEN LK 9POS	1
J4	CONNECTOR; SMB, Straight, JACK, SMD	1
W1	CABLE, 18 AWG, 4.2	1
	PCB, RO4350, 2.5 X 4.0 X 0.030	1
Q1	CGHV31500F1	1

CGHV31500F1-AMP Evaluation Board Assembly Drawing



Bias On Sequence

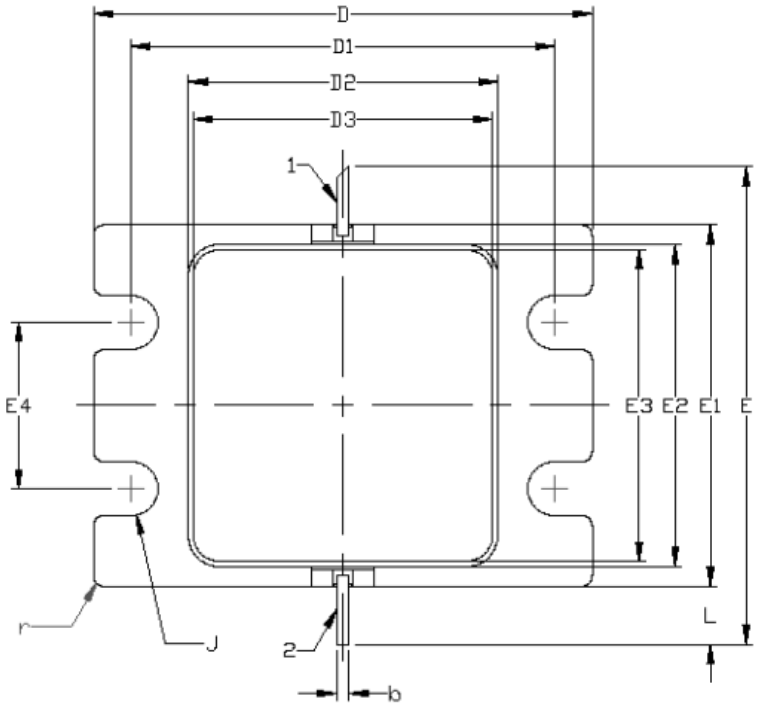
1. Ensure RF is turned-off
2. Apply pinch-off voltage of -5 V to the gate (Vg)
3. Apply nominal drain voltage (Vd)
4. Adjust Vg to obtain desired quiescent drain current (Idq)
5. Apply RF

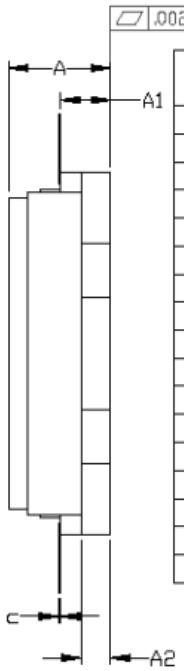
Bias Off Sequence

1. Turn RF off
2. Apply pinch-off to the gate (Vg=-5V)
3. Turn off drain voltage (Vd)
4. Turn off gate voltage (Vg)

Product Dimensions

NOTES: (UNLESS OTHERWISE SPECIFIED)
1. INTERPRET DRAWING IN ACCORDANCE WITH ANSI Y14.5M-2009
2. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF .020 BEYOND EDGE OF LID
3. LID MAY BE MISALIGNED TO THE BODY OF PACKAGE BY A MAXIMUM OF .008 IN ANY DIRECTION
4. ALL PLATED SURFACES ARE GOLD OVER NICKEL





DIM	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.185	0.201	4.70	5.11	
A1	0.088	0.100	2.24	2.54	2x
A2	0.049	0.061	1.24	1.55	
b	0.022	0.026	0.56	0.66	2x
c	0.003	0.006	0.08	0.15	
D	0.935	0.955	23.75	24.26	
D1	0.797	0.809	20.24	20.55	2x
D2	0.581	0.593	14.76	15.06	
D3	0.565	0.571	14.35	14.50	
E	0.906		23.01		REF
E1	0.679	0.691	17.25	17.55	
E2	0.604	0.616	15.34	15.65	
E3	0.588	0.594	14.93	15.09	
E4	0.309	0.321	7.85	8.15	2x
J	ø0.097	ø0.107	ø2.46	ø2.72	4x
L	0.090	0.130	2.29	3.30	2x
r	0.02 TYP		0.51 TYP		12x

Pin	Description
1	GATE/RFIN
2	DRAIN/RFOUT
3	SOURCE/FLANGE

Electrostatic Discharge (ESD) Classification

Parameter	Symbol	Class	Classification Level	Test Methodology
Human Body Model	HBM	TBD	ANSI/ESDA/JEDEC JS-001 Table 3	JEDEC JESD22 A114-D
Charge Device Model	CDM	TBD	ANSI/ESDA/JEDEC JS-002 Table 3	JEDEC JESD22 C101-C

Product Ordering Information

Part Number	Description	MOQ Increment	Image
CGHV31500F1	2.7 – 3.1 GHz, 500W GaN HPA		
CGHV31500F1-AMP	Evaluation Board w/ PA	1 Each	

Notes & Disclaimer

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