Keywords: telecom,hot-swap,16ms dropout,150V transient,MAX5921,ATCA,transient immune, dropout immune,80 Watt,holdup

REFERENCE DESIGN 4163 INCLUDES: √Tested Circuit √Schematic √BOM √Description √Test Data √Layout

Telecom Hot-Swap Reference Design Is Immune to Overvoltage and Brownout Input Transients

Mar 26, 2008

Abstract: This 80W telecom hot-swap reference design is immune to 150V input-voltage transients and 16ms power dropouts. Additional features include -32V to -72V operation, two-diode OR-ing input, and an inrush current that is ≤ 1.5 times the full-load current. Included are a detailed schematic, representative PCB layout, bill of materials, waveforms detailing actual performance at startup, -150V input transient, and full-load holdup at power loss.

Introduction

Telecom systems typically must provide full-power operation from either of two voltage sources that may range between -36V and -72V. Protection must additionally be provided against lightning-induced, higher-voltage pulses and occasional power brownout conditions where the input voltage may drop to 0V for several milliseconds. A plug-in line card may include a high-voltage to low-voltage DC-DC converter preceded by a hot-swap circuit. This circuit limits inrush current to little more than full-load current when the line card is hot-plugged into a live backplane. The hot-swap circuit must provide a power-good (active-low PGOOD) signal to activate the following DC-DC converter after on-card filter capacitors have reached full charge. A hot-swap circuit meeting all requirements is detailed in this document. Most requirements are similar to those of an AdvancedTCA® (ATCA®) first-level hot-swap circuit.

Typical Telecom System Requirements

1. Input Voltage: -43V to -72V Operation
2. Two-Diode OR-ing at Input
3. -32V to -36V Turn-Off (at the Power Source Before the Diode)
4. 80W (max) Input Power, C_{LOAD} = 680µF
5. Withstand -150V, 1ms Overvoltage Pulse[1]
6. Ride-Through, 0V, 16ms Brownout Beginning at -43V Input Voltage; Active-Low PGOOD Must Remain Asserted Throughout this Period
7. Inrush Current ≤ 1.5x Full-Load Current at 43V Startup Voltage

Reference Design Features and Considerations

1. The undervoltage-lockout (UVLO) increasing voltage is set to ~43V. The overvoltage-lockout (OVLO) increasing voltage is set to ≥ 72V.
2. Two 100V Schottky diodes installed at the input allow OR-ing between two discrete sources.
3. The UVLO decreasing voltage is set to ~32V. The design must satisfy Telecom System Requirement 6 while maintaining normal operation with active-low PGOOD active down to the UVLO decreasing voltage.
4. P_{IN} = 80W at V_{IN} = 43V indicates an input current of 1.86A.
5. A 70V TVS diode clamps any input-voltage pulse to a safe level for U1, C3, C4, and Q2. This diode may be placed either directly across the input terminals or across the V_{DD}–V_{EE} pins of the MAX5921 hot-swap

controller and isolated from V_{IN} with a 5Ω series resistor.

6. An energy-storage capacitor (C3) stores sufficient energy to supply an 80W load for 16ms beginning at 43V and ending at 32V. This capacitor charges through a resistor to limit its charging current to a small percentage of the input surge current specified in Telecom System Requirement 7. A Schottky diode bypasses the charge-limiting resistor during discharge.
7. A circuit-breaker minimum-limit trip point is selected to allow the 2.8A, 150% startup surge current at 43V and the 2.5A full-power operation down to 32V.

Telecom Hot-Swap Reference Design

This telecom hot-swap reference design utilizes a MAX5921 hot-swap controller, as shown in the **Figure 1** diagram.

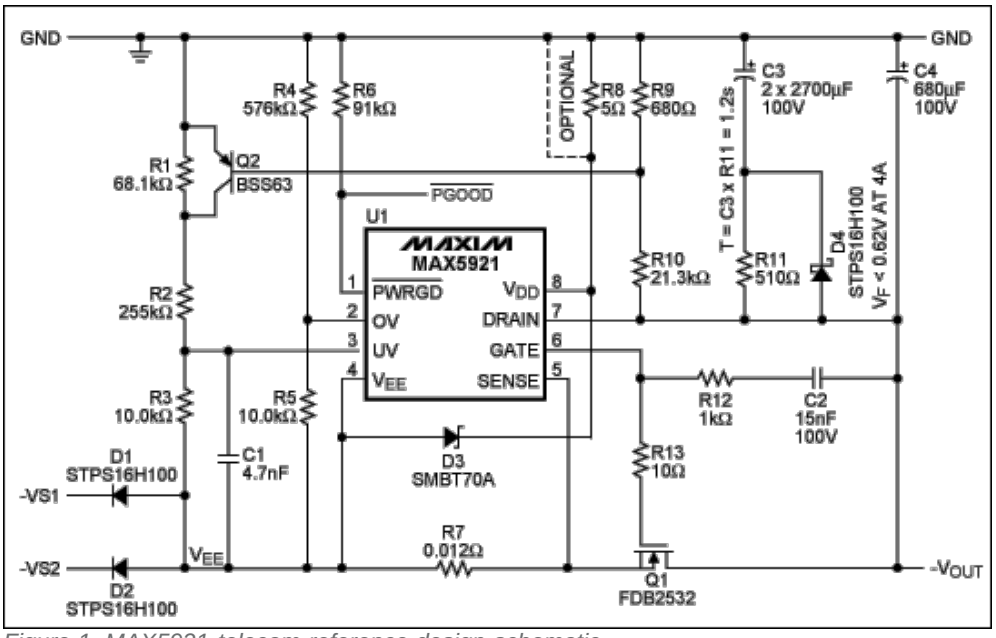

Figure 1. MAX5921 telecom reference design schematic.

Turn-On Performance

The UVLO increasing voltage is set by voltage divider² (R1+R2):R3 as:

$$UVLO\uparrow = V_{UVH}\frac{R1+R2+R3}{R3} + V_{F(D1)} = (1.255 \pm 0.015)V \times \frac{68.1k\Omega + 255k\Omega + 10k\Omega}{10k\Omega} + 0.55V$$
$$= 42.35V \pm 0.5V = 41.85V \text{ to } 42.85V$$

Although the input UVLO increasing turn-on voltage is set by the voltage divider (R1+R2):R3, the input UVLO decreasing turn-off voltage is set by the voltage divider R2:R3. This is because Q2 shorts out R1 when the output voltage appears during startup.

The waveforms in **Figure 2** were created when the input voltage was slowly raised until the UVLO increasing voltage was reached. This occurs at:

$V_{IN} - V_{S1} = V_{IN} - V_{EE} + V_{F(D1)} \approx 42.4V$

The gate voltage rises to midvalue, controlling the output-voltage slew rate at 2.2V/ms to limit the charging current into the output capacitor (C4). The input current ($I_{C4} + I_{C3}$) peaks at 1.75A. When V_{OUT} reaches its final value, the input current decreases to the charging current (I_{C3}).

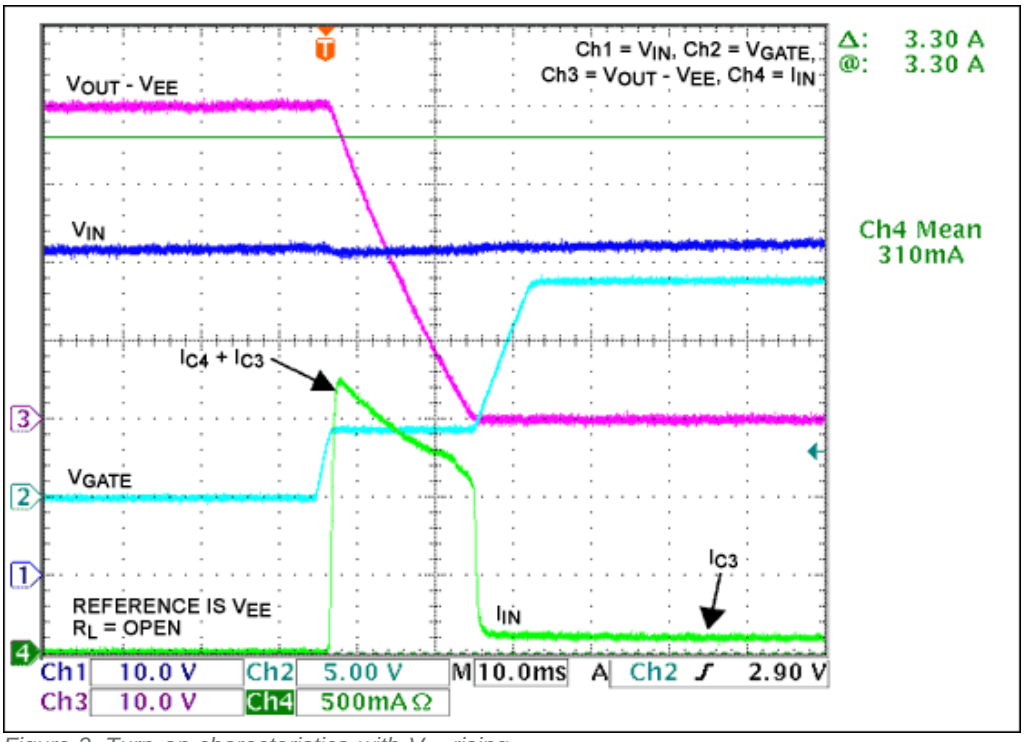

Figure 2. Turn-on characteristics with V_{IN} rising.

Input surge current at startup is controlled by selecting the value of C2.

$$I_{INRUSH} = I_{PU} \frac{C4}{C2} = 45\mu A \frac{680\mu F}{15nF} = 2.04A$$

Thus, the inrush current is limited to ≤ 1.5 times the 1.86A startup current at a 43V input. A smaller value of C2 will increase the inrush current. For example, if C2 = 12nF, then I_{INRUSH} = 2.55A, which is closer to the allowed 2.8A. The input surge current is shown in Figure 2.

Figure 3 is similar to Figure 2, except it shows that active-low PGOOD is asserted 7ms after V_{GATE} reaches its final value and 15ms after V_{OUT} reaches its final value.

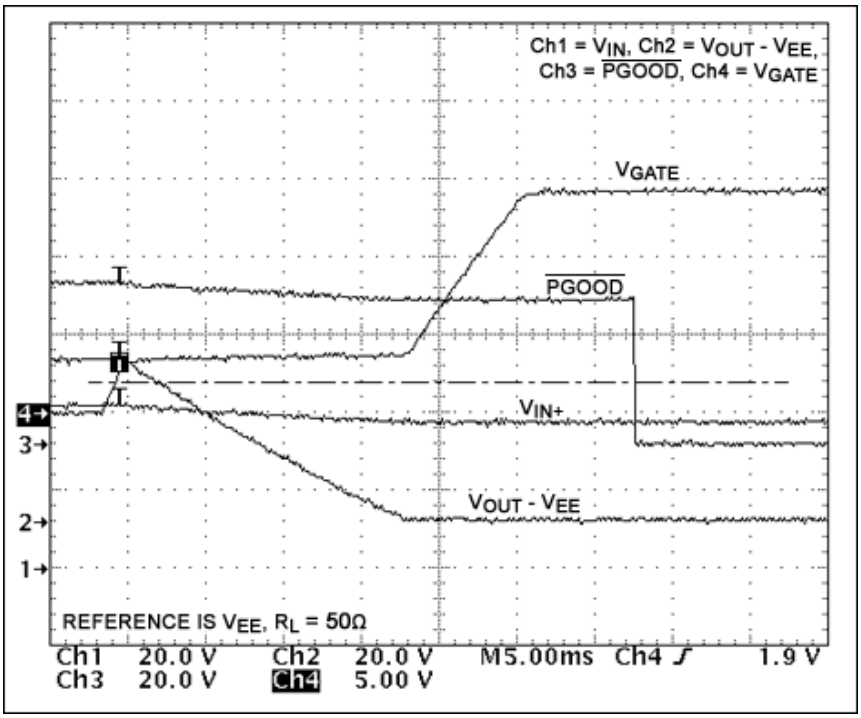

Figure 3. Turn-on characteristics with active-low PGOOD.

When hot-swap nears completion, Q2 shorts out R1, and the UVLO decreasing voltage is set near 32V to meet Telecom System Requirements 3 and 6.

$$UVLO\downarrow = V_{UVL}\frac{R2 + R3}{R3} + V_{F(D1\ or\ Q1)} = (1.225 \pm 0.02)V \times \frac{255k\Omega + 10k\Omega}{10k\Omega} + 0.6V$$
$$= 33.0625V \pm 0.530V = 32.5V\ to\ 33.6V$$

Figure 4 shows the charging of C3 at startup. Charge time is independent of the existence of an output load as C3's initial charging current is only ~100mA peak at V_{IN} = 50V. Charge time is approximately 10s; therefore, the brownout hold-up time is not fully available until 10s after turn-on or following an earlier brownout period.

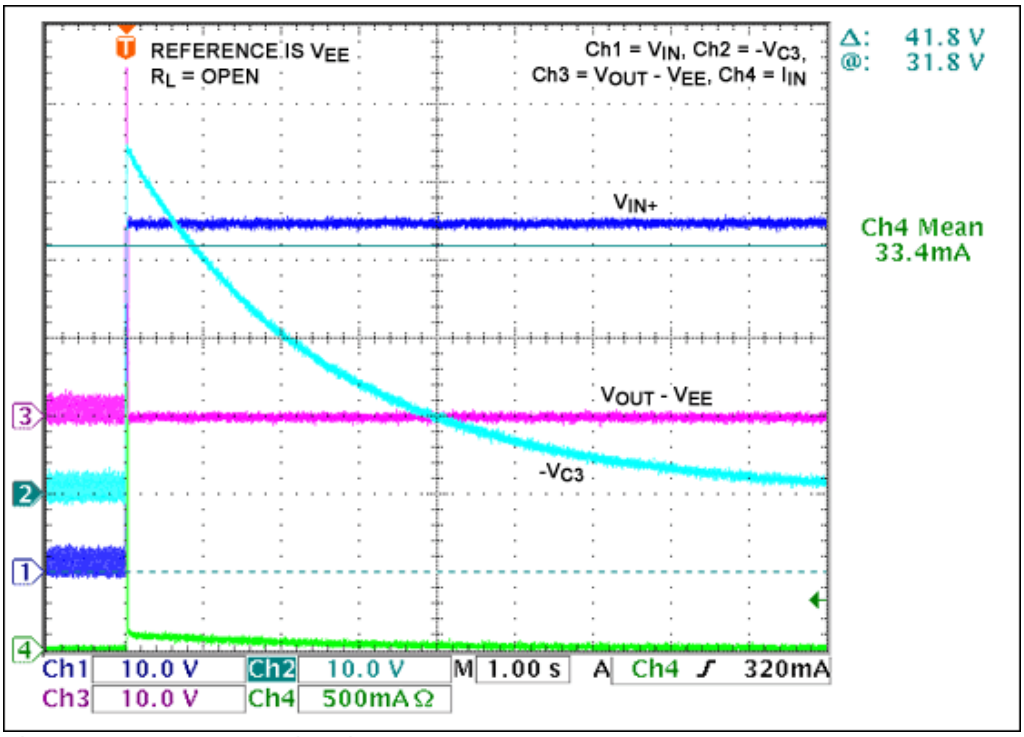

Figure 4. C3 storage capacitor charge at turn-on.

Dropout Immunity

Hold-up time during a brownout period is calculated as follows:

P = 80W and C3 = 5400µF

Dropout may begin at worst-case V_{IN} = 43V, where:

$V_{OUT} = V_{IN} - V_{F(D1)} = 43V - 0.55V = 42.45V$

As soon as the input voltage drops out, V_{OUT} decreases by the drop in diode D4, or by another 0.6V, to 41.85V.

C3 supplies the load during dropout, and active-low PGOOD is valid until:

$UVLO_{MAX} = 33.6V = [V_{CAP} - V_{F(D4)} + V_{F(Q1)}]$ or $V_{CAP} = 34.8V$

$$\text{Energy} = P \times t = \frac{1}{2}CV^2, \text{ and}$$

$$t = \frac{CV^2}{2P} = \frac{C}{2P}(V^2_{MAX} - V^2_{MIN}) = \frac{5400 \times 10^{-6}}{2 \times 80}(41.85^2 - 34.8^2) = 18.24ms$$

Therefore, allowing a 10% tolerance for the capacitor, the calculated hold-up time is 16.4ms.

With no conduction in diodes D1 or D2 during an input-voltage dropout, C3 supplies voltage to the MAX5921 input through the body diode of Q1. Hence, the MAX5921 is operational and supports a valid active-low PGOOD during the brownout period.

An output power of 80W can be maintained by C3 during a brownout input-voltage dropout period (beginning at V_{IN} = 43V and extending to V_{OUT} = 32V) of up to 16ms. C3 is charged through resistor R11 at power-up. The C3 x R11 time constant is chosen as 4860ms to prevent C3 charge current from overwhelming the input surge current

due to the charging of C4 at startup. Therefore, full brownout protection is not provided until ~10s after power-on.

The dropout-immunity waveforms of **Figure 5** show that the initial power is approximately 4.185A × 41.85V ≈ 175W (note that the output voltage drops immediately by the forward voltage of D4 as soon as input power is disconnected).

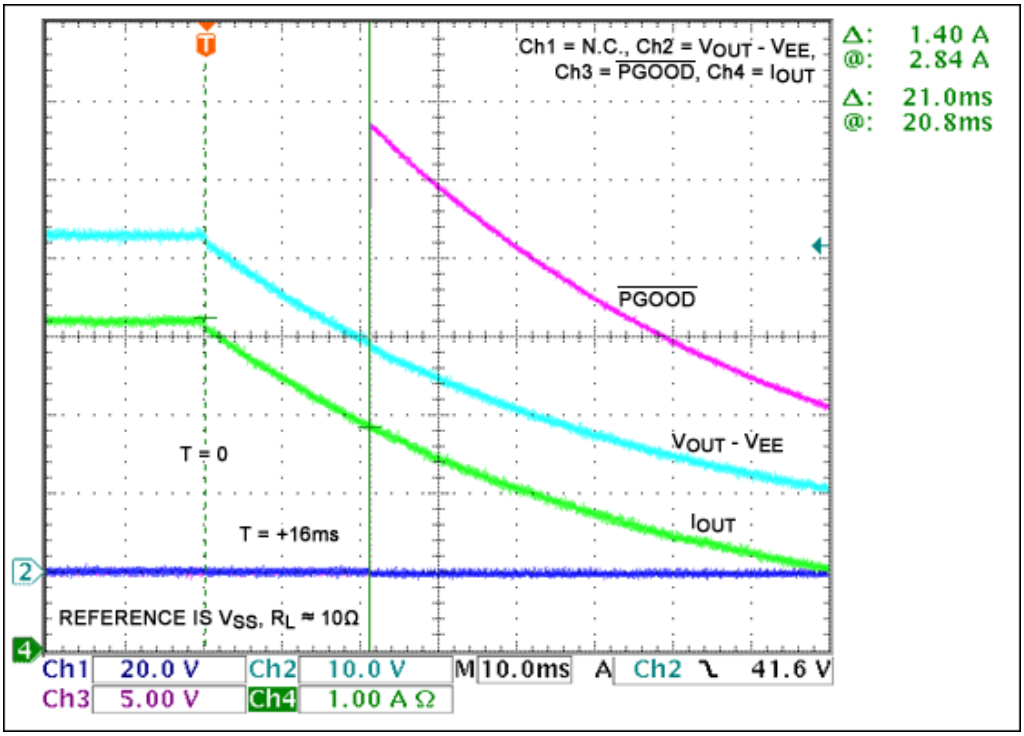

Figure 5. Waveforms at dropout.

Sixteen milliseconds after the dropout begins at 43V, the output has dropped to 31.5V where the power is approximately 3.15A × 3.15V ≈ 99W. Thus, it is seen that there is more than adequate energy storage in C3 to satisfy the dropout-immunity requirement.

Overvoltage Lockout

The OVLO increasing voltage is set by voltage divider R4:R5 as:

$$OVLO\uparrow = V_{UVH}\frac{R4+R5}{R5} + V_{F(D1)} = (1.225 \pm 0.02)V \times \frac{576k\Omega + 10k\Omega}{10k\Omega} + 0.5V$$
$$= 73.54V \pm 1.172V = 72.4V\ (min)\ to\ 74.7V\ (max)$$

Circuit-Breaker Trip Point

The circuit-breaker trip point is selected to assure that trip will not occur at the minimum specified V_{IN} or upon initial surge current. Thus, the minimum trip point is calculated at the larger of 80W/32V = 2.5A or (1.5 × 80W)/43V = 2.8A. As C3 provides all load current during a 16ms brownout period, there is no current through the sense resistor during this period. Resistor R7 sets the trip point as:

$$I_{CL} = \frac{V_{CL}}{R7} = \frac{50mV \pm 10mV}{12m\Omega} = 4.17A \pm 0.833A = 3.34A\ to\ 5.03A$$

Pulsed Overvoltage Immunity

The MAX5921 must be protected from input transients above 100V. Two circuit conditions may be considered.

1. One circuit option incorporates a 5.6Ω series resistor (R8) from $+V_{IN}$ to the V_{DD} pin of the MAX5921, and a TVS diode (D3) between the V_{DD} and V_{EE} pins. In this case, only the MAX5921 is protected, and C3 and C4, as well as Q2, should be rated for > 150V transients.
2. An alternate circuit option connects the TVS diode directly across the V_{IN} terminals following the OR-ing diodes to protect the entire circuit. The selected SMBT70A (D3) limits the transient pulse to ≤ 100V. This is the only TVS diode specified to clamp the pulse voltage at ≤ 100V, while still conducting < 1mA at 75V. Circuitry is input-voltage protected by D3 from the pulse waveform produced by the 0.2-Joule capacitor discharge described in footnote 1.

MAX5921 Protection Only

In the **Figure 6** and **7** graphs, device protection is provided for input transients by D3. Only the MAX5921 is protected when R8 is present. An 0.2-Joule input pulse is provided by the method described in footnote 1.

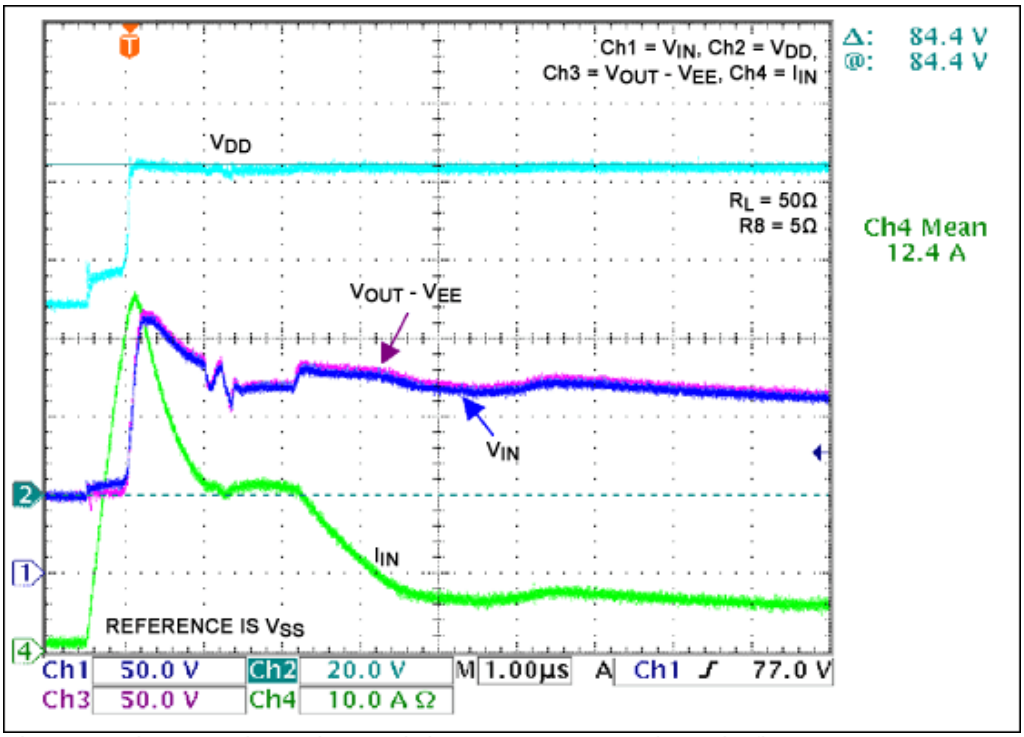

Figure 6. Pulse overvoltage characteristics; MAX5921 protection only; first 9µs.

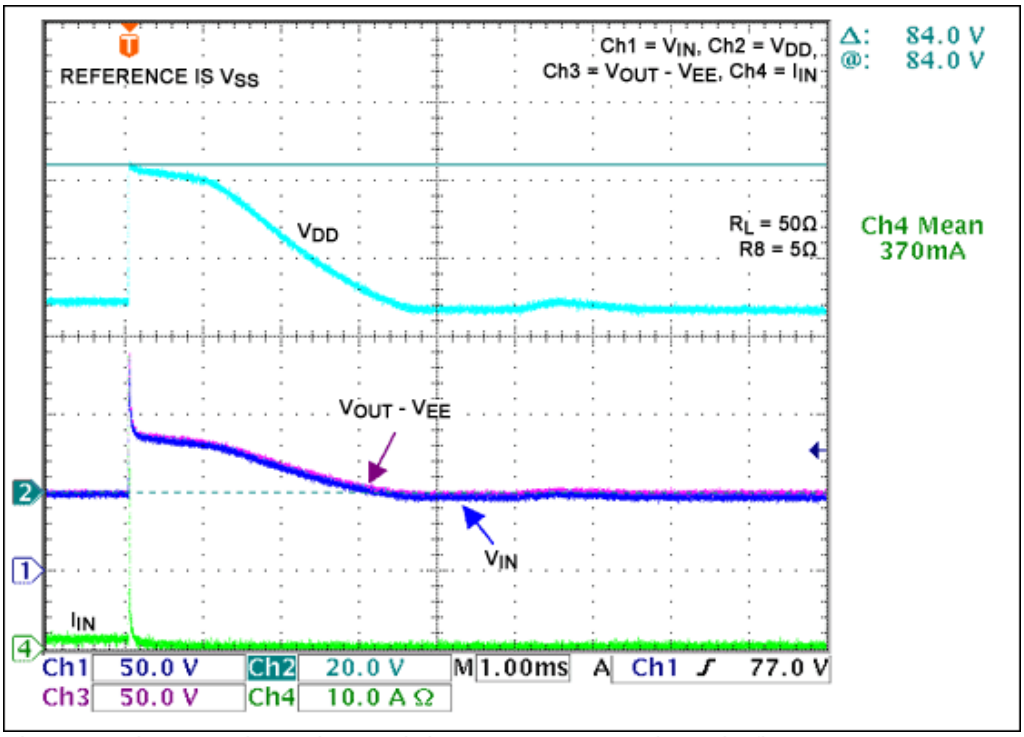

Figure 7. Pulse overvoltage characteristics; MAX5921 protection only; first 9ms.

V_{DD} - V_{SS} is limited at 84.4V. The input current shows a triangular spike with a width of 4µs and a peak of 46A.

V_{IN} rises for 3ms, peaking at 165V or 115V above the initial V_{IN} of 50V. V_{OUT} - V_{EE} follows V_{IN}, also rising 115V above its initial 0V value. Hence, the input pulse is rejected at the output, due to the temporary gate turn-off caused by the MAX5921's input-transient and OVLO circuit-protection mechanisms. C3 supplies the output during the time that the gate is turned off.

Protection of the Entire Circuit

The **Figure 8** and **9** graphs show the results of shorting R8, which provides protection for the MAX5921, Q1, and the circuitry that follows Q1.

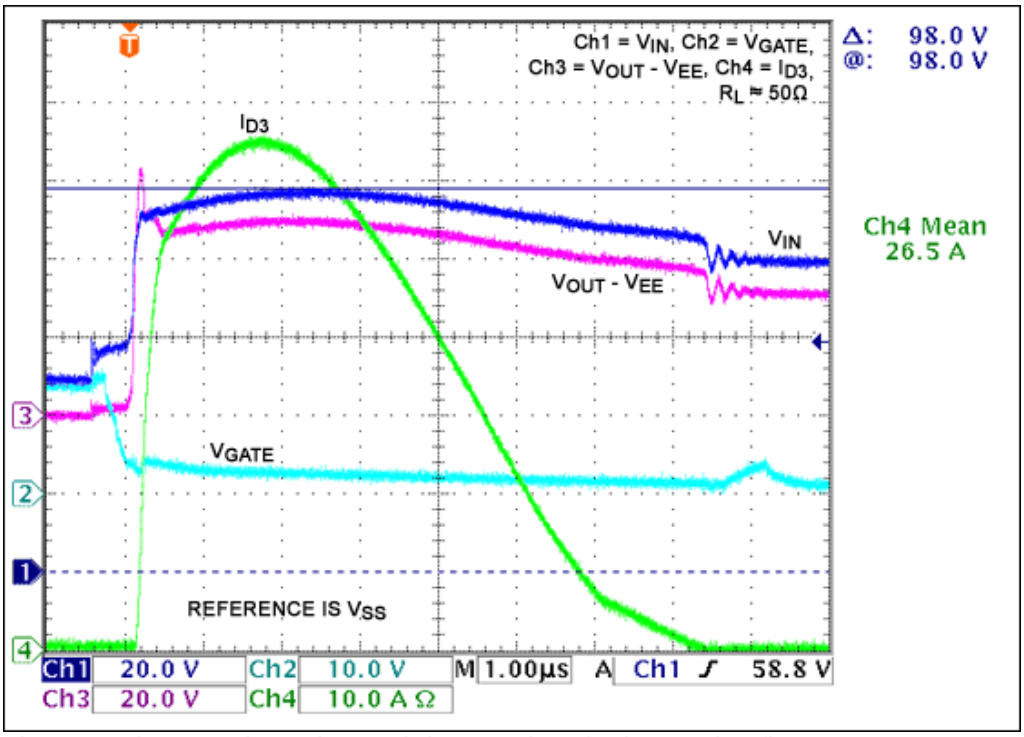

Figure 8. Pulse overvoltage characteristics; complete circuit protection; first 10ms.

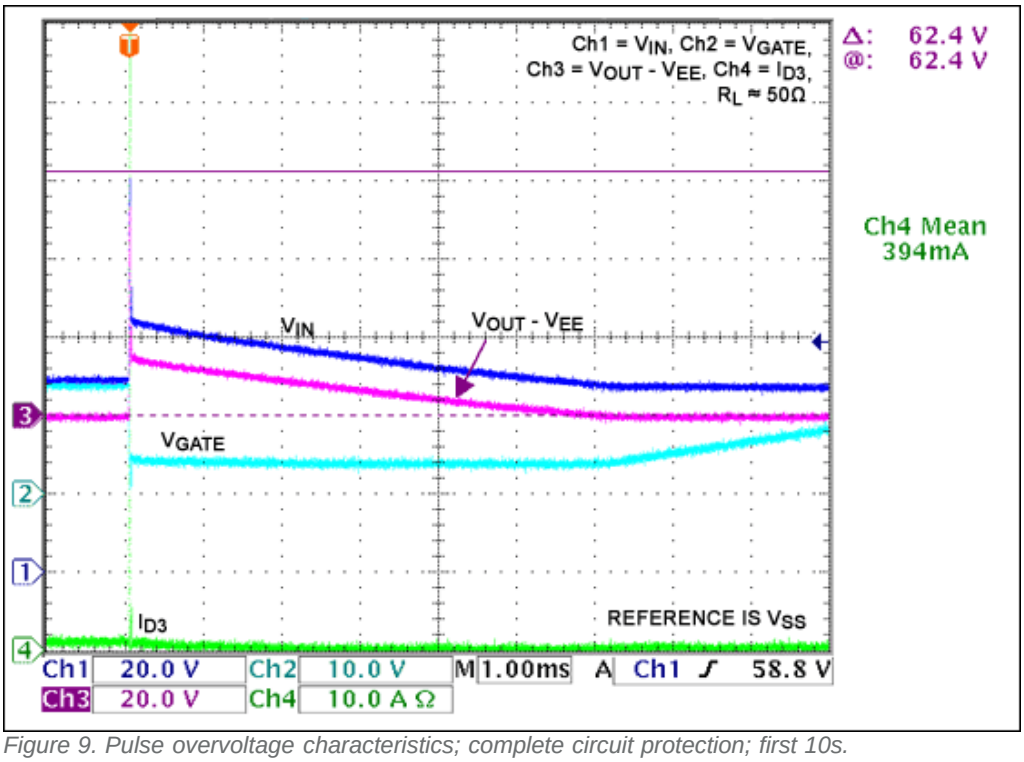

Figure 9. Pulse overvoltage characteristics; complete circuit protection; first 10s.

V_{IN} rises to 98V or 50V over its initial value for approximately 6µs, and returns to ~65V in 30µs before subsiding to its initial value in 6ms. The input-voltage peak is accompanied by a triangular input-current spike with a peak of 66A and a width of 6µs. All of this current flows through D3.

Gate voltage drops to near 0V in 500ns and recovers to normal in ~12ms. This shuts off Q1 to reject the input transient.

V_{OUT} - V_{EE} exhibits an initial 100ns rise of ~60V that quickly subsides to a broader 50V pulse, which lasts for 6µs before returning to its normal level in 6ms. The input pulse is completely rejected at the output, except for the first 400ns, due to gate turn-off. C3 carries the load while V_{GATE} returns to its normal value in 12ms when transient recovery is complete.

Summary

This telecom hot-swap reference design meets all typical Telecom System Requirements. Hold-up time is implemented and effective for ≥ 16ms as required. Pulsed overvoltage protection is provided to protect either only the MAX5921 or the entire circuit. The short across R8 may be removed if the user prefers that D3 protect only the MAX5921. If the short is removed across R8, C3 and C4 should be rated at 160V. The use of the Diodes Inc. TVS diode SMBT70A is key to the overvoltage transient protection—no other TVS diode is ideally suited to this task.

Bill of Materials

Qty.	Designator	Component	Manufacturer and Part Number
1	C1	4.7nF ±10%, 50V ceramic capacitor (0805)	Vishay VJ0805Y472KXACW1BC
1	C2	15nF ±10%, 50V ceramic capacitor (0805)	Vishay VJ0805Y153KXACW1BC
2	C3a, C3b	2700µF ±10%, 100V electrolytic capacitors	Panasonic ECD-S2AP272CA
1	C4	680µF ±10%, 100V electrolytic capacitor	Panasonic ECD-S2AP681BA
3	D1, D2, D4	10A or 16A, 100V Schottky diodes (D2PAK)	Vishay MBRB10H100CT-E3/45, ST Microelectronics STPS16H100CG, or Vishay 16CTQ100SPBF
1	D3	70V TVS diode (SMB)	Diodes Inc. SMBT70A
1	Q1	150V, 16mΩ n-channel MOSFET (D2PAK)	Fairchild FDB2532 or Vishay SUM85N15-19-T1-E3
1	Q2	100V, bipolar PNP transistor (SOT23)	Fairchild BSS63
1	R1	68.1kΩ ±1% thick-film resistor (0603)	Vishay CRCW0603154KFKEA
1	R2	255kΩ ±1% thick-film resistor (0603)	Vishay CRCW0603255KFKEA
2	R3, R5	10.0kΩ ±1% thick-film resistors (0603)	Vishay CRCW060310K0FKEA
1	R4	576kΩ ±1% thick-film resistor (0603)	Vishay CRCW0603576KFKEA
1	R6	91kΩ ±5% thick-film resistor (0805)	Vishay CRCW080591K0JNEA
1	R7	12mΩ thick-film resistor (2512)	Vishay WSL2512R0120FEA
1	R8	5Ω ±1% thick-film resistor (2512)	Vishay CRCW25125R00FKEG
1	R9	680Ω ±1% thick-film resistor (0603)	Vishay CRCW0603680RFKEA
1	R10	21.3kΩ ±1% thick-film resistor (1210)	Vishay CRCW121021K3FKEA
1	R11	510Ω ±1% thick-film resistor (2512)	Vishay CRCW2512510RFKEG
1	R12	1kΩ ±1% thick-film resistor (0603)	Vishay CRCW06031K00FKEA
1	R13	10Ω ±1% thick-film resistor (0603)	Vishay CRCW060310R0FKEA
1	**U1**	**Hot-swap controller IC, -100V**	**Maxim MAX5921AESA**

Test PCB Layout

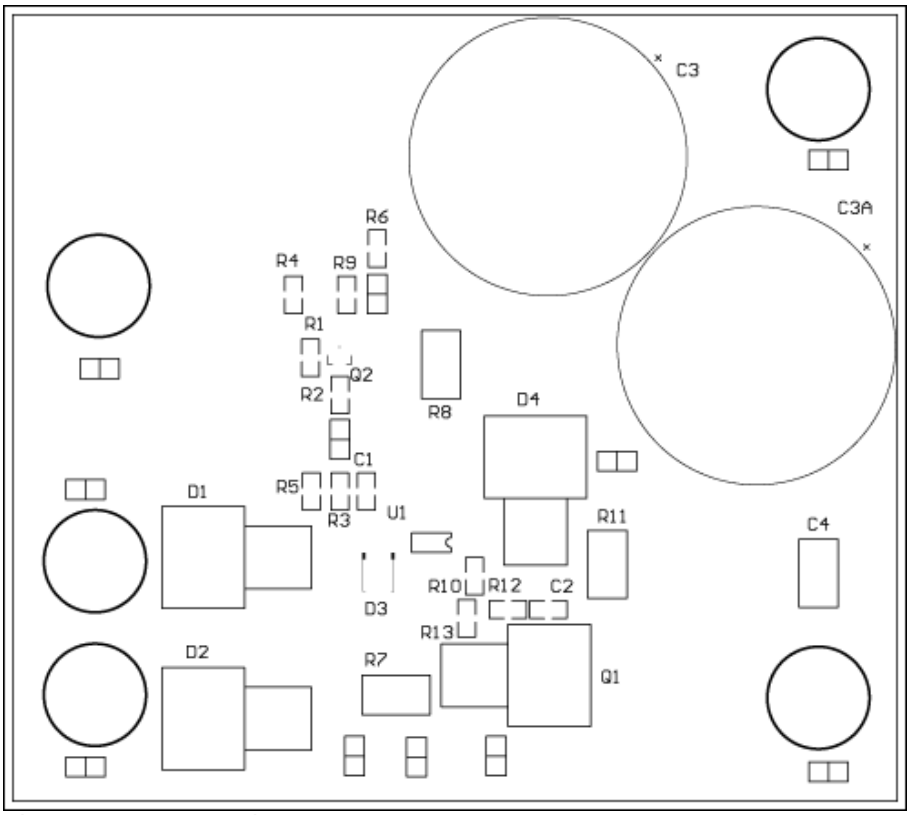

Figure 10. Component layout.

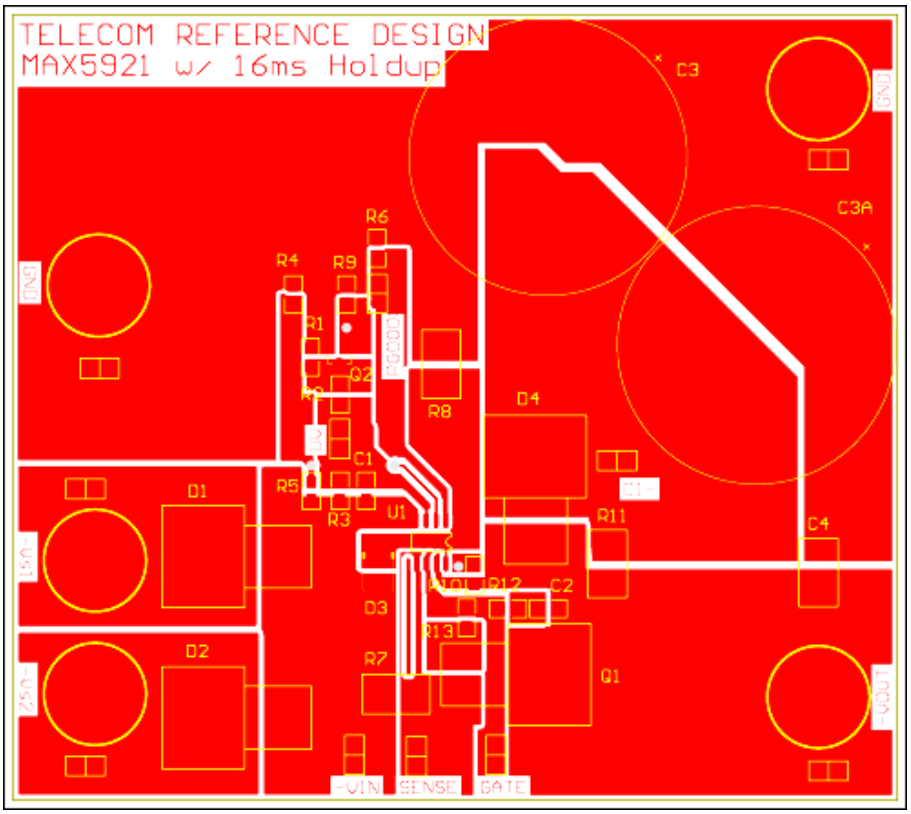

Figure 11. Top layer.

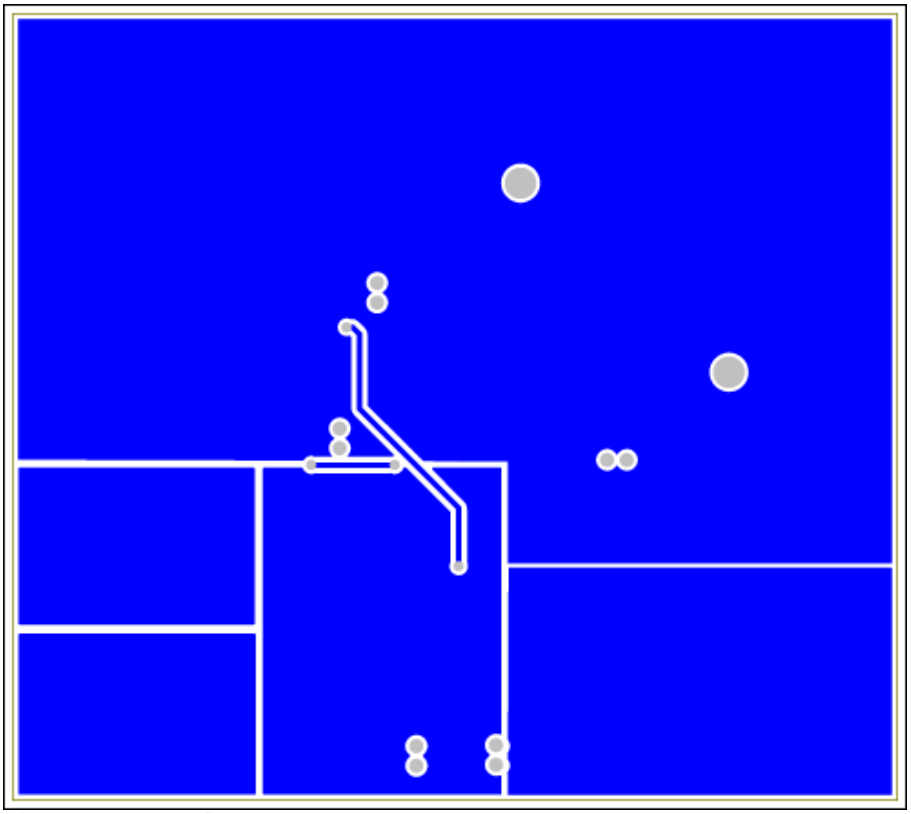

Figure 12. Bottom layer.

References

1. The 0.2-Joule test pulse is formed by discharging an 18µF capacitor (charged to 150V) into the circuit input while the power source is isolated by a 10mH inductor, as directed in Power & Earthing of Transmission Equipment Specification 1555, Telstra Corp Ltd. CAN 051 775 55.
2. Resistor tolerance is not included in UVLO and OVLO calculations. V_{UVH}, V_{UVL}, and V_{OVH} values are from the MAX5921 data sheet.

Related Parts		
MAX5941	IEEE 802.3af-Compliant Power-Over-Ethernet Interface/PWM Controller for Power Devices	Free Samples

More Information
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