

Integrated Load Switch

FDC6325L

General Description

This device is particularly suited for compact power management in portable electronic equipment where 2.5 V to 8 V input and 1.8 A output current capability are needed. This load switch integrates a small N-Channel power MOSFET (Q1) which drives a large P-Channel power MOSFET (Q2) in one tiny SUPERSOT™-6 package.

Features

- $V_{DROD} = 0.2 \text{ V}$ @ $V_{IN} = 5 \text{ V}$, $I_L = 1.5 \text{ A}$, $R_{(ON)} = 0.13 \Omega$
 $V_{DROD} = 0.2 \text{ V}$ @ $V_{IN} = 3.3 \text{ V}$, $I_L = 1.2 \text{ A}$, $R_{(ON)} = 0.16 \Omega$
 $V_{DROD} = 0.2 \text{ V}$ @ $V_{IN} = 2.5 \text{ V}$, $I_L = 1 \text{ A}$, $R_{(ON)} = 0.18 \Omega$
- SUPERSOT™-6 Package Design Using Copper Lead Frame for Superior Thermal and Electrical Capabilities
- This is a Pb-Free Device

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

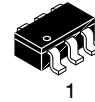
Symbol	Parameter	Ratings	Unit
V_{IN}	Input Voltage Range	2.8 – 8	V
$V_{ON/OFF}$	On/Off Voltage Range	1.5 – 8	V
I_L	Load Current	Continuous (Note 1)	1.8
		Pulsed (Notes 1 & 3)	5
P_D	Maximum Power Dissipation (Note 2)	0.7	W
T_J, T_{STG}	Operating and Storage Temperature Range	–55 to 150	$^\circ\text{C}$
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100 pF / 1500 Ω)	6	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. $V_{IN} = 8 \text{ V}$, $V_{ON/OFF} = 8 \text{ V}$, $T_A = 25^\circ\text{C}$
2. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

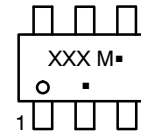
THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 2)	180	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 2)	60	$^\circ\text{C/W}$



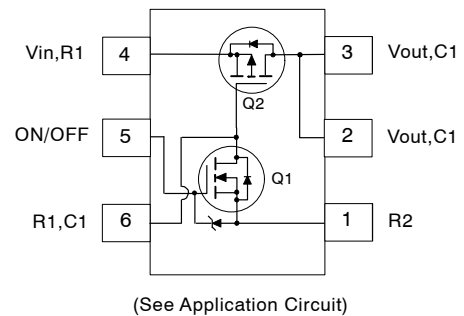
TSOT23 6-Lead
CASE 419BL

MARKING DIAGRAM

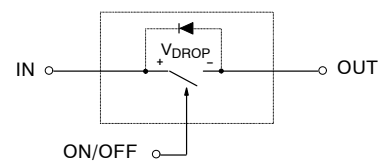


XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

PINOUT



EQUIVALENT CIRCUIT



ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDC6325L

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

I _{FL}	Forward Leakage Current	V _{IN} = 8 V, V _{ON/OFF} = 0 V			1	μA
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ON CHARACTERISTICS (Note 3)

V _{DROP}	Conduction Voltage Drop	V _{IN} = 5 V, V _{ON/OFF} = 3.3 V, I _L = 1.5 A		0.15	0.2	V
		V _{IN} = 3.3 V, V _{ON/OFF} = 3.3 V, I _L = 1.2 A		0.145	0.2	
		V _{IN} = 2.5 V, V _{ON/OFF} = 3.3 V, I _L = 1 A		0.13	0.2	
R _(ON)	Q ₂ – Static On-Resistance	V _{GS} = -5 V, I _D = -1.8 A		0.115	0.13	Ω
		V _{GS} = -3.3 V, I _D = -1.6 A		0.13	0.16	
		V _{GS} = -2.5 V, I _D = -1.5 A		0.155	0.18	
I _L	Load Current	V _{DROP} = 0.13 V, V _{IN} = 5 V, V _{ON/OFF} = 3.3 V	1			A
		V _{DROP} = 0.16 V, V _{IN} = 3.3 V, V _{ON/OFF} = 3.3 V	1			
		V _{DROP} = 0.2 V, V _{IN} = 2.5 V, V _{ON/OFF} = 3.3 V	1			

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty cycle ≤ 2.0 %.

ORDERING INFORMATION

Device	Device Marking	Package Type	Shipping [†]
FDC6325L	.325	TSOT-23-6 (Pb-free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

FDC6325L Load Switch Application

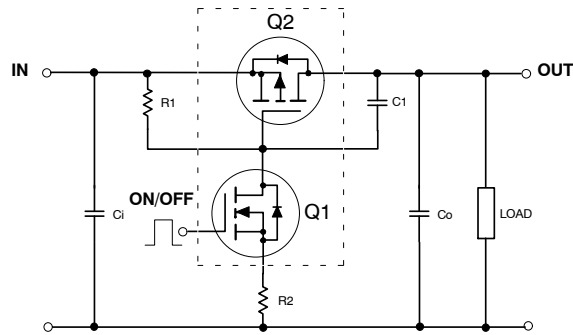


Figure 1. Application Circuit

External Component Recommendation

For C₀ ≤ 1 μF applications:

First select R₂, 100 – 1 kW, for Slew Rate control.

C₁ ≤ 1000 pF can be added in addition to R₂ for further In-rush current control.

Then select R₁ such that R₁/R₂ ratio maintains between 10 – 100. R₁ is required to turn Q₂ off. For SPICE simulation, users can download a “FDC6325L.MOD” Spice model from **onsemi** Web Site at www.onsemi.com

TYPICAL ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

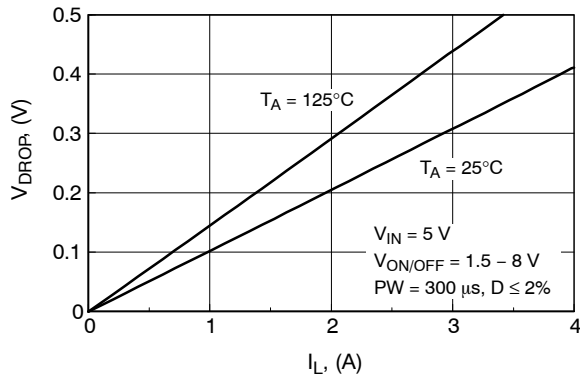


Figure 1. Conduction Voltage Drop Variation with Load Current

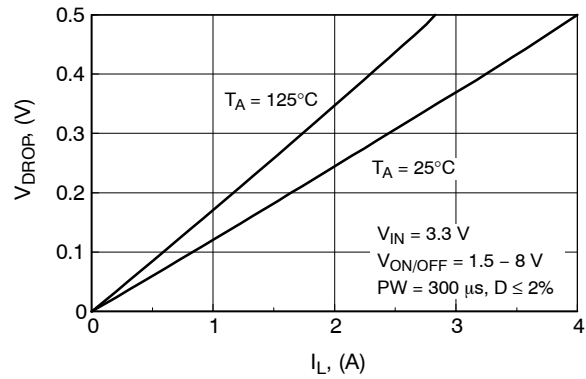


Figure 2. Conduction Voltage Drop Variation with Load Current

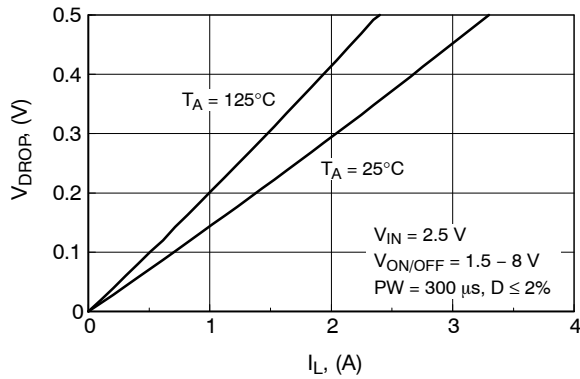


Figure 3. Conduction Voltage Drop Variation with Load Current

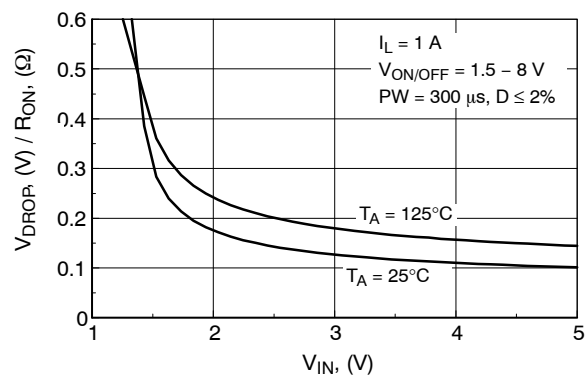


Figure 4. On-Resistance Variation with Input Voltage

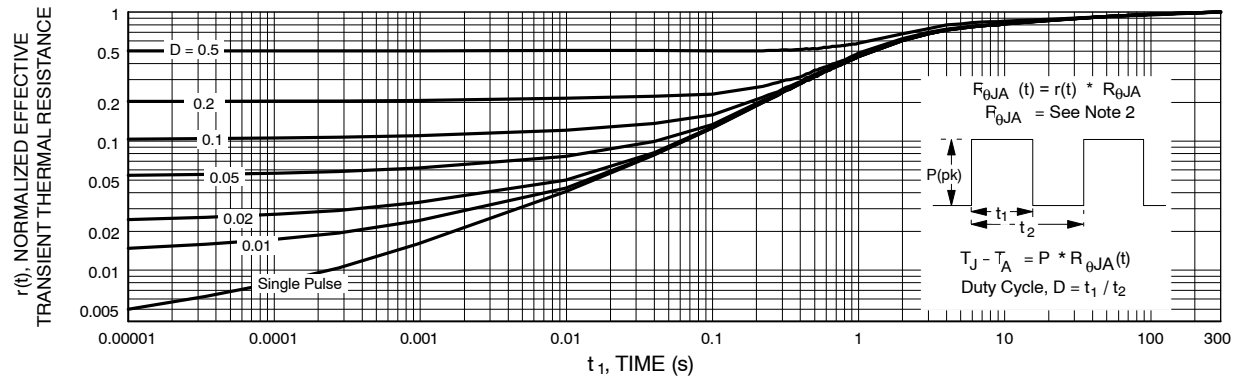


Figure 5. Transient Thermal Response Curve

Note: Thermal characterization performed using the conditions described in Note 2.

Transient thermal response will change depending on the circuit board design.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

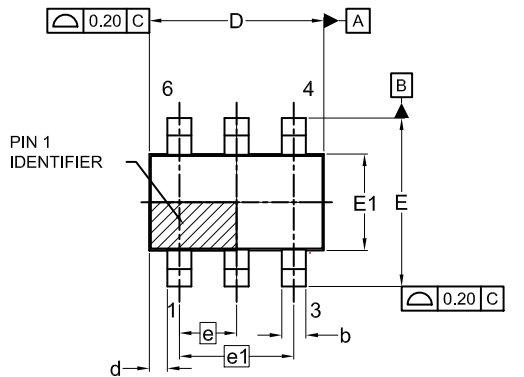
ON Semiconductor®



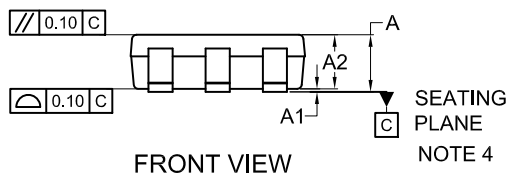
SCALE 2:1

TSOT23 6-Lead CASE 419BL ISSUE A

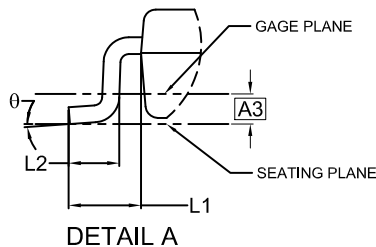
DATE 31 AUG 2020



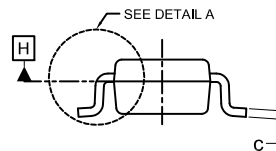
TOP VIEW



FRONT VIEW

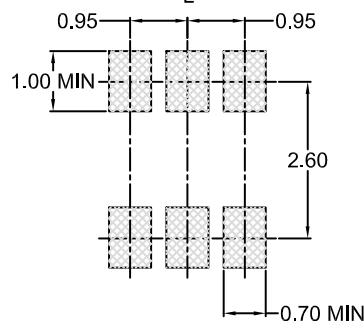


DETAIL A



SIDE VIEW

SYMM



LAND PATTERN RECOMMENDATION

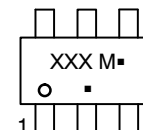
*FOR ADDITIONAL INFORMATION ON OUR
Pb-FREE STRATEGY AND SOLDERING DETAILS,
PLEASE DOWNLOAD THE ON SEMICONDUCTOR
SOLDERING AND MOUNTING TECHNIQUES
REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3	0.25 BSC		
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d	0.30 REF		
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.95 BSC		
e1	1.90 BSC		
L1	0.60 REF		
L2	0.20	0.40	0.60
Θ	0°	—	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code

M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	TSOT23 6-Lead	PAGE 1 OF 1

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