ALPHA & OMEGA SEMICONDUCTOR

AOZ1382DI-01

ECPower™ Type-C PD Ideal Diode Sink/ Source Combo 2-in-1 Protection Switch

General Description

AOZ1382DI-01 integrates two back-to-back power switches and control circuitry into one single package to provide all the functionality and protection needed for sourcing and sinking current through a USB Type-C port with PD capability.

The sink function features Ideal Diode True Reverse Current Blocking (IDTRCB). It supports power ORing configurations and can sink current from the Type-C port through a back-to-back MOSFET with only 20 mΩ ON resistance from VBUS to VCHG pin. The VBUS operating range is from 3.4 V to 23 V under sink mode with absolute maximum rating of 28V on both VBUS and VCHG pins. There is Under-Voltage Lock Out (UVLO) and Over-Voltage Lock Out (OVLO) on VBUS. The sink switch has an active low enable input to support dead battery operation and its soft-start is adjustable through an external capacitor through the SS pin.

The source function provides power to the VBUS from V5V through a separate back-to-back MOSFET with 39 mΩ ON resistance. The input operating range at V5V pin is from 3.4 V to 5.5 V. The sourcing switch is also protected by UVLO and OVLO. There is internal soft-start to control inrush current. The current limit can be adjusted from 500 mA to 3.5A with an external resistor. The source function has short circuit protection that shuts off the switch quickly to prevent input droop and system brown out. The sourcing switch also features a FON pin for fast turn-on capability to support the Fast Role Swap (FRS) function

AOZ1382DI-01 has True Reverse Current Blocking (TRCB) function in the source modes and Ideal Diode True Reverse Current Blocking (IDTRCB) in the sink mode. The back-to-back MOSFET automatically prevents reverse current when the output voltage exceeds the input voltage. The device is also protected by thermal shutdown. There are two FLTB flags, FLTB_SNK for sink mode and FLTB_SRC for source mode, which are open drain outputs and each will be pulled low independently for fault condition. AOZ1382DI is available in a 3mm x 5.2mm DFN-20L package and can operate from -40 °C to +85 °C temperature range.

Features

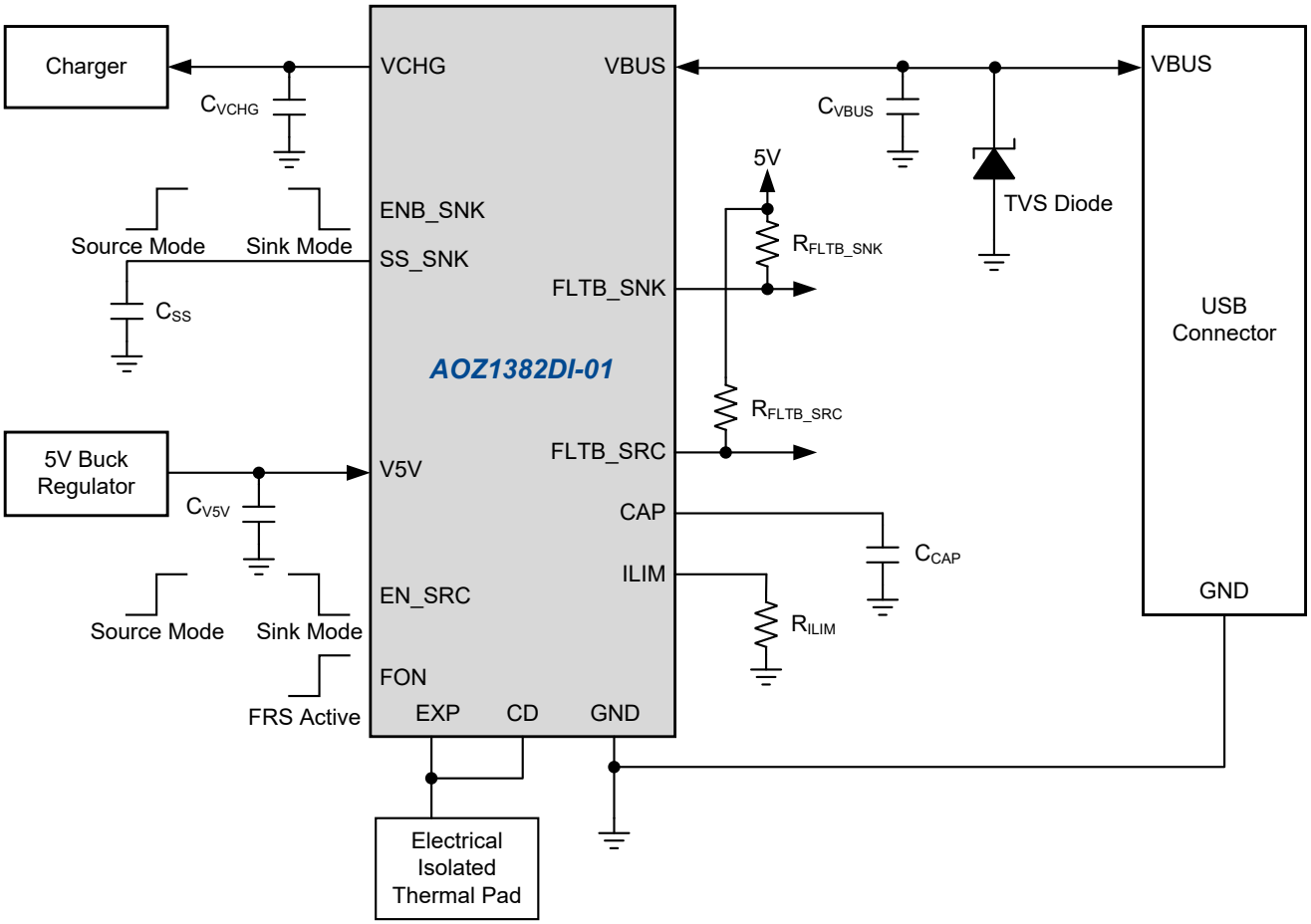
- Support Type-C PD sink and source mode
- 10 A Sink Continuous Current
- 20 A Sink Pulsed Current (10 ms @ 2% Duty Cycle)
- Thermal shutdown protection
- IEC 62368-1: 2014 Certification No US-36226-M2-UL
- ± 2.5 kV HBM rating
- ± 1 kV CDM rating
- IEC 61000-4-2 ± 8 kV on VBUS
- IEC 61000-4-5 40 V on VBUS (no cap)
- **Sink Switch Features**:
  - Ideal Diode True Reverse Current Blocking (IDTRCB)
  - 20 mΩ ON resistance
  - 3.4 V to 23 V operating voltage
  - VBUS and VCHG rated 28 V
  - Under Voltage Lock Out (UVLO)
  - Programmable soft-start
  - Enable active low for dead battery operation
- **Source Switch Features:**
  - 39 mΩ ON resistance
  - FRS (Fast Role Swap) support
  - 3.4 V to 5.5 V operating voltage
  - True Reverse Current Blocking (TRCB)
  - Programmable current limit (OCP)
  - Internal soft-start
  - Enable active high
- 3mm x 5.2mm DFN-20L package

Applications

- Thunderbolt/USB Type-C PD ports
- Portable devices
- Notebooks
- Ultrabooks
- Docking Stations / Dongles
- Power ORing Applications

Green Product

Typical Application



Ordering Information

Part Number	Fault Recovery	Junction Temperature Range	Package	Environmental
AOZ1382DI-01	Auto-Recovery	-40 °C to +125 °C	DFN3x5.2-20L	RoHS

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

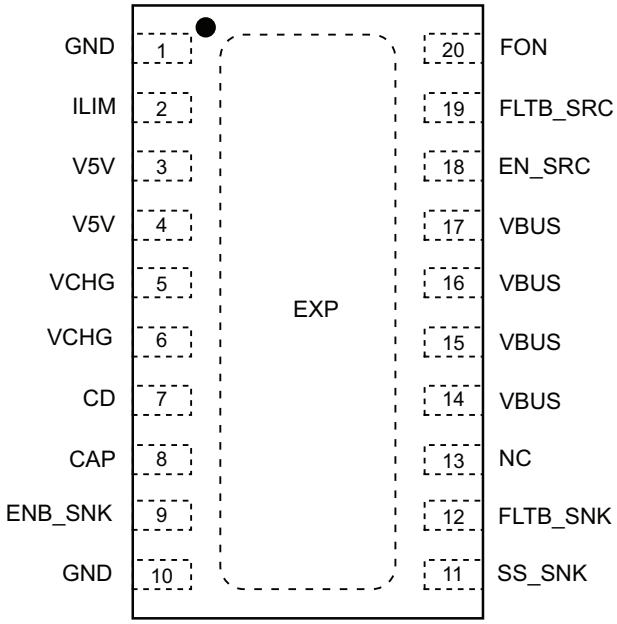


Figure 1. DFN3x5.2-20L
(Top Transparent View)

Pin Description

Pin Number	Pin Name	Pin Function
1, 10	GND	Ground connection.
2	ILIM	Current limit setting for Source mode. Connect a resistor to this pin to set the threshold of current limit.
3, 4	V5V	Source mode power input from 5 V power bus.
5,6	VCHG	Sink mode power output to battery charger.
7	CD	Common drain sense pin. This pin must be connected to the EXP and electrically isolated. No external load is allowed on this pin.
8	CAP	Connect a 1 nF Capacitor to GND. No external load is allowed on this pin.
9	ENB_SNK	Enable for Sink mode. Active low.
11	SS_SNK	Soft start slew rate control for Sink mode.
12	FLTB_SNK	Open drain fault indicator for Sink mode. Connect a pull up resistor from this pin to 5 V supply
13	NC	No connect.
14, 15, 16, 17	VBUS	Common power bus for VCHG and V5V. It is connected to VCHG for Sink mode or V5 V for Source mode.
18	EN_SRC	Enable for Source function. Active high.
19	FLTB_SRC	Open drain fault indicator for Source mode. Connect a pull up resistor from this pin to 5 V supply.
20	FON	Fast Role Swap (FRS) function control for Source mode.
EXP	EXP	Exposed Thermal Pad. It is the common drain node of the internal back-back sink switches and it must be electrically isolated. Solder to a metal surface directly underneath EXP and connect to floating Cu thermal pads on multiple PCB layers through VIAs. For best thermal performance make the floating Cu pads as large as possible and connect to EXP with multiple VIAs.

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
VBUS, VCHG, CD to GND	-0.3 V to 28 V
V5V to GND	-0.3 V to 6 V
Control Inputs ENB_SNK, EN_SRC, SS_SNK, ILIM, FON to GND	-0.3 V to 6 V
Outputs FLTB_SNK, FLTB_SRC to GND	-0.3 V to 6 V
CAP to VIN	-0.3 V to 6 V
Junction Temperature (T_J)	+150 °C
Storage Temperature (T_S)	-65 °C to +150 °C
ESD Rating HBM/CDM All Pins	±2.5 kV / ±1 kV
IEC 61000-4-2 on VBUS (Air and Contact)	±8 kV

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
VBUS, VCHG, CD to GND	3.4 V to 23 V
V5V to GND	0 V to 5.5 V
Control Inputs ENB_SNK, EN_SRC, SS_SNK, ILIM, FON to GND	0 V to 5.5 V
Outputs FLTB_SNK, FLTB_SRC to GND	0 V to 5.5 V
CAP to VIN	-3.0 V to 5.5 V
Sink Switch DC Current (I_{SW_SNK})	0 A to 10 A
Peak Sink Switch Current (I_{SW_PK}) for 10 ms @ 2% Duty Cycle	20 A
Source Switch DC Current (I_{SW_SRC})	0 A to 3.5 A
Junction Temperature (T_J)	-40 °C to +125 °C
Package Thermal Resistance Evaluation Board DFN3x5.5-17L (Θ_{JA})	36 °C/W

Electrical Characteristics for Sink Mode Switch

T_A = 25 °C, VBUS = 20 V, FON = 0 V, ENB_SNK = 0 V, EN_SRC = 0 V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Sink Mode General Characteristics						
V_{BUS}	Input Supply Voltage		3.4		23	V
V_{UVLO_SNK}	Under-voltage Lockout Threshold	VBUS rising	3.0		3.35	V
$V_{UVLO\_SNK\_HYS}$	Under-voltage Lockout Hysteresis	VBUS rising		0.25		V
$I_{VBUS\_ON\_SNK}$	Input Quiescent Current	V_{BUS} = 20 V, I_{VCHG} = 0 A		550		µA
$I_{VBUS\_OFF\_SNK}$	Input Quiescent Current	V_{BUS} = 20 V, I_{VCHG} = 0 A, ENB_SNK = 5V		32		µA
I_{VCHG_OFF}	Input Shutdown Current	V_{CHG} = 20 V, V_{BUS} = 0 V, ENB_SNK = 5V		32		µA
R_{ON_SNK}	Output Leakage Current	I_{VBUS} = 1 A[(1)]		20		mΩ
Sink Mode Enable and Fault Logic						
$V_{ENB\_SNK\_H}$	Enable Input High Voltage	ENB_SNK rising	1.4			V
$V_{ENB\_SNK\_L}$	Enable Input Low Voltage	ENB_SNK falling			0.6	V
I_{ENB_SNK}	Enable Input Bias Current	ENB_SNK = 1.8 V			10	µA
V_{FLTB_SNK}	Fault Pull-down Voltage	I_{SINK} = 3 mA			0.3	V

Electrical Characteristics for Sink Mode Switch *(Continued)*

T_A = 25 °C, VBUS = 20 V, FON = 0 V, ENB_SNK = 0 V, EN_SRC = 0 V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Sink Mode Over-Voltage Protection						
V_{OVLO_SNK}	Overvoltage Lockout Threshold	VBUS rising	23.1	24	25	V
$V_{OVLO\_SNK\_HYS}$	Overvoltage Lockout Hysteresis	VBUS falling		300		mV
$t_{OVLO\_DEB\_SNK}$	Over-Voltage Protection Debounce Time	From VBUS ≥ V_{OVLO_SNK} to switch turns off		512		µs
Sink Mode Ideal Diode True Reverse Current Blocking (IDTRCB)						
V_{IDTRCB_SNK}	IDTRCB Regulation Voltage	VBUS – VCHG		35		mV
V_{TRCB_SNK}	Fast TRCB Threshold	VCHG – VBUS		100		mV
Dynamic Characteristics						
$t_{DLY\_ON\_SNK}$	Turn-On Delay Time	ENB_SNK to VCHG at 10 % of VBUS C_{CHG} = 10 µF, C_{SS} = 5.6 nF		8		ms
t_{ON_SNK}	Turn-On Rise Time	VCHG rising from 10% to 90% of VBUS C_{CHG} = 10 µF, C_{SS} = 5.6 nF		1.9		ms
t_{OFF_SNK}	Turn-Off Fall Time	From ENB_SNK falling edge to I_{VBUS} = 0 A		32		µs
t_{REC_SNK}	Auto Restart Time after Fault			64		ms
Thermal Shutdown for Sink Mode						
T_{TSD_SNK}	Thermal shutdown Threshold	Temperature rising		140		°C
$T_{TSD\_SNK\_HYS}$	Thermal Shutdown Hysteresis	Temperature falling		30		°C

Electrical Characteristics for Source Mode Switch

T_A = 25 °C, VBUS = 20 V, FON = 0 V, ENB_SNK = 5 V, EN_SRC = 5 V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Source Mode General Characteristics						
V_{V5V}	Input Supply Voltage		3.4		5.5	V
V_{UVLO_SRC}	Under-Voltage Lockout Threshold	V5V rising	3	3.25	3.35	V
$V_{UVLO\_SRC\_HYS}$	Under-Voltage Lockout Hysteresis	V5V falling		200		mV
$I_{V5V\_ON\_SRC}$	Input Quiescent Current	V5V = 5 V, I_{VBUS} = 0 A		125		µA
$I_{V5V\_OFF\_SRC}$	Input Shutdown Current	V5V = 5 V, EN_SRC = 0 V		6		µA
R_{ON_SRC}	Switch On Resistance	V5V = 5 V, I_{VBUS} = 0 A		39		mΩ
Source Mode Enable, Fast On, and Fault Logic						
$V_{EN\_SRC\_H}$	Enable Input Logic High Threshold	EN_SRC rising	1.4			V
$V_{EN\_SRC\_L}$	Enable Input Logic Low Threshold	EN_SRC falling			0.4	V
I_{EN_SRC}	Enable Input Bias Current	EN_SRC = 1.8 V		1	1.5	µA
V_{FON_H}	Fast-On Input Logic High Threshold	FON rising	1.4			V
V_{FON_L}	Fast-On Input Logic Low Threshold	FON falling			0.4	V
I_{FON}	Fast-On Input Bias Current	FON = 1.8 V		1.5	4	µA
V_{FLTB_SRC}	Fault Pull-down Voltage	I_{SINK} = 3 mA			0.3	V
Source Mode Over-Voltage Protection						
V_{OVLO_SRC}	Over-voltage Lockout Threshold	V5V rising	5.7	5.9	6	V
$V_{OVLO\_SRC\_HYS}$	Over-voltage Lockout Hysteresis	V5V falling		250		mV
$t_{DELAY\_OVLO\_SRC}$	OVP Turn-Off Delay			3.5		µs
Source Mode Over-Current Protection						
I_{LIM}	Current Limit Threshold	VBUS = 5 V, R_{LIM} = 4.02 kΩ	3.15	3.5	3.85	A
		VBUS = 5 V, R_{LIM} = 7.1 kΩ	1.78	2	2.22	
		VBUS = 5 V, R_{LIM} = 14.3 kΩ	0.9	1	1.1	
$t_{OCP\_FLTB\_SRC}$	Over-Current Flag Delay	From I_{VBUS} ≥ I_{LIM} to FLTB_SRC pulled low		10		ms
Source Mode True Reverse-Current Blocking (TRCB)						
$V_{T\_TRCB\_SRC}$	TRCB Protection Trip Point	VBUS - V5V, VBUS rising		25		mV
$V_{R\_TRCB\_SRC}$	TRCB Protection Release Trip Point	V5V - VBUS, VBUS falling		40		mV
$V_{TRCB\_SRC\_HYS}$	TRCB Hysteresis	$V_{T\_TRCB\_SRC}$ + $V_{R\_TRCB\_SRC}$		65		mV
t_{TRCB_SRC}	TRCB Response Time	VBUS - V5V > $V_{T\_TRCB\_SRC}$ + 500 mV		600		ns

Electrical Characteristics for Source Mode Switch *(Continued)*

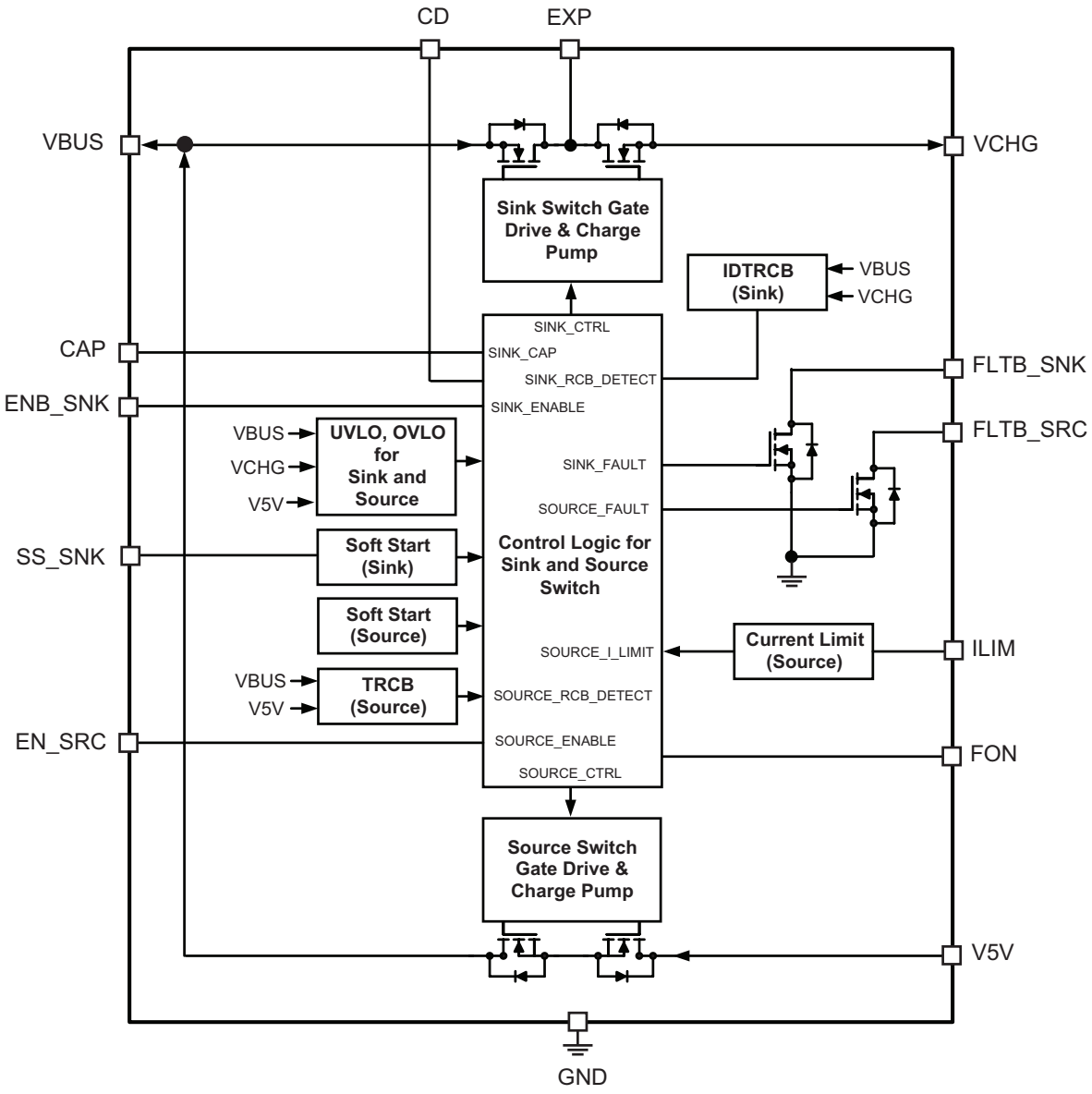
T_A = 25 °C, VBUS = 20 V, FON = 0 V, ENB_SNK = 5 V, EN_SRC = 5 V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Source Mode Dynamic Characteristics						
$t_{DLY\_ON\_SRC}$	Turn-On Delay Time (From EN_SRC = VEN_SRC_H to VBUS = 0.5 V)	R_{VBUS} = 100 Ω, C_{VBUS} = 1 µF		2.1		ms
t_{ON_SRC}	Turn-On Time (VBUS from 0.5 V to 4.5 V)	R_{VBUS} = 100 Ω, C_{VBUS} = 1 µF		2.7		ms
t_{FON}	Fast Turn-On Time (From EN_SRC = VEN_SRC_H to VBUS = 4.75 V)	FON = 5 V, R_{VBUS} = 100 Ω, C_{VBUS} = 1 µF		50	100	µs
t_{S_FON}	Fast Turn-On Setup Time	FON = 5 V before EN_SRC, = $V_{EN\_SRC\_H}$	100			µs
t_{H_FON}	Fast Turn-On Hold Time	FON = 5 V after EN_SRC, = $V_{EN\_SRC\_H}$	40			µs
t_{REC_SRC}	Auto Restart Time after Fault			24		ms
Thermal Shutdown for Source Mode						
T_{TSD_SRC}	Thermal Shutdown Threshold	Temperature rising		140		°C
$T_{TSD\_SRC\_HYS}$	Thermal Shutdown Hysteresis	Temperature falling		30		

Note:

1. RON is tested at 1A in test mode to bypass ideal diode regulation

Functional Block Diagram



Timing Diagrams

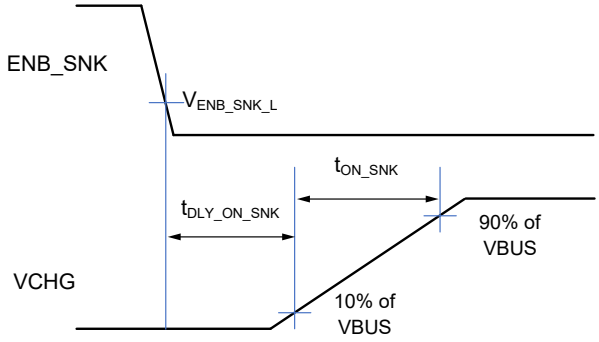


Figure 2. Turn-on Delay and Turn-on Time in Sink Mode

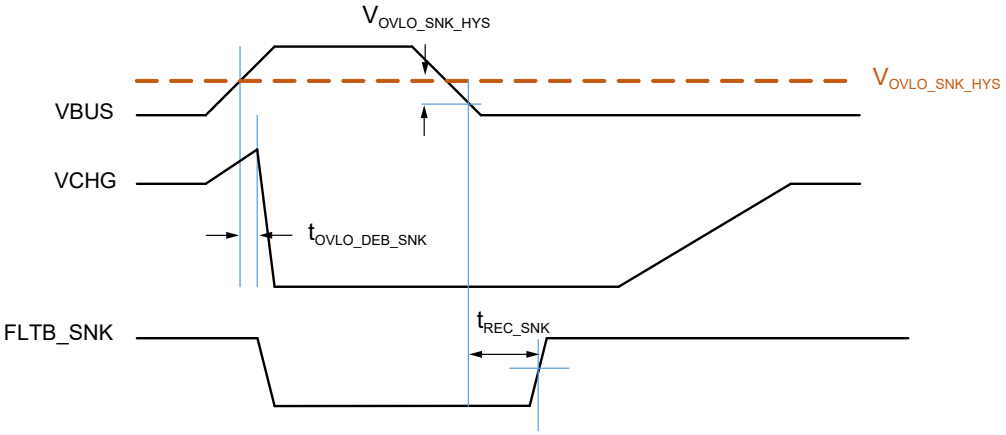


Figure 3. Over-Voltage Protection (OVP) Operation in Sink Mode

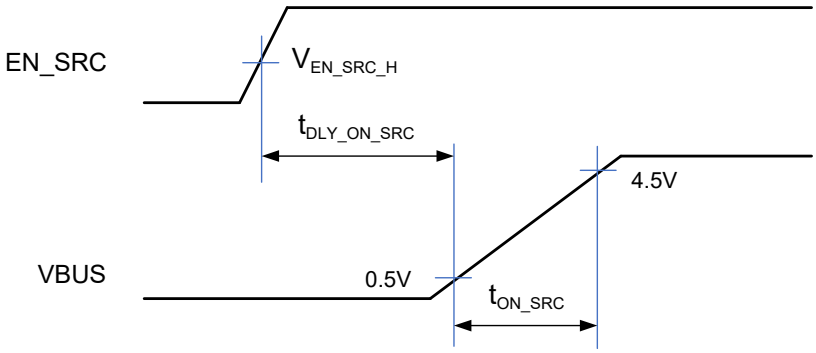


Figure 4. Turn-on Delay and Turn-on Time in Source Mode

Timing Diagrams *(Continued)*

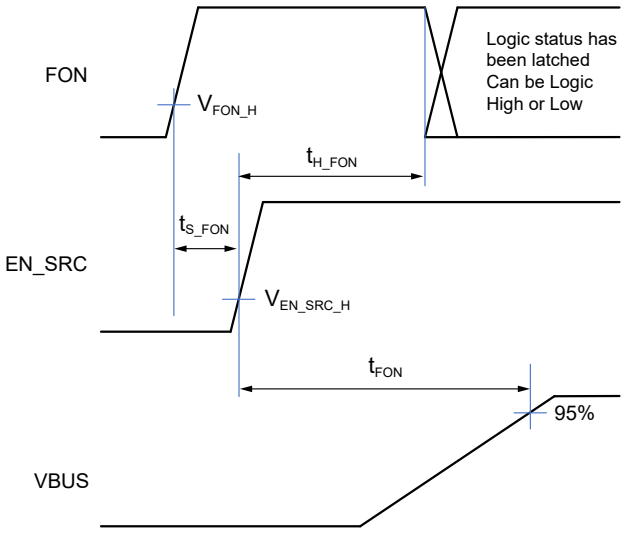


Figure 5. Turn-on Time with Fast Role Swap (FRS) in Source Mode

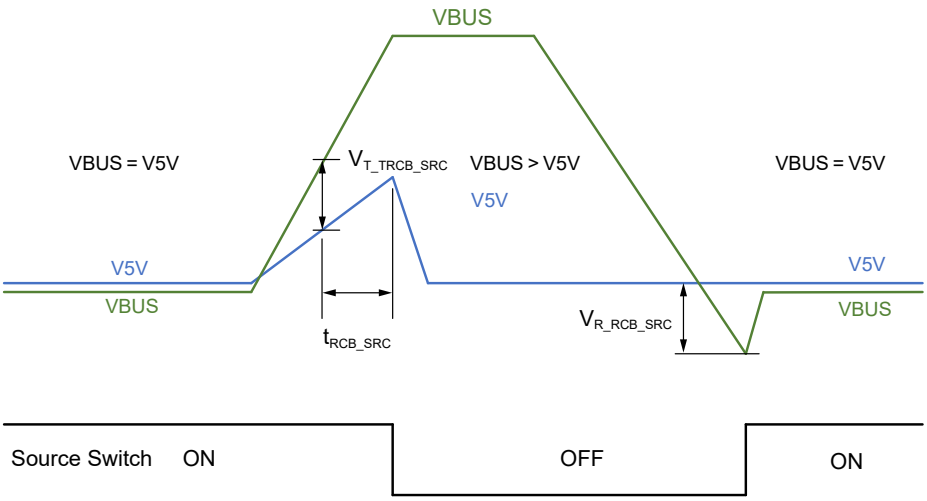


Figure 6. True Reverse Current Blocking (RCB) Operation in Source Mode

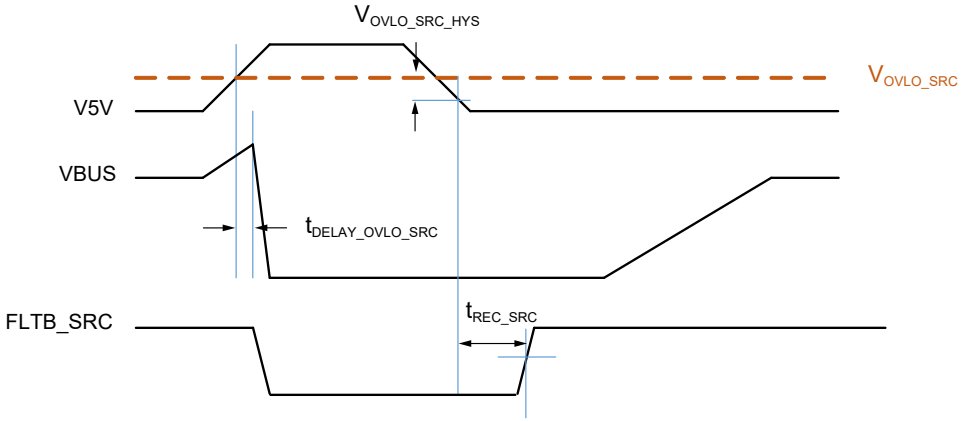
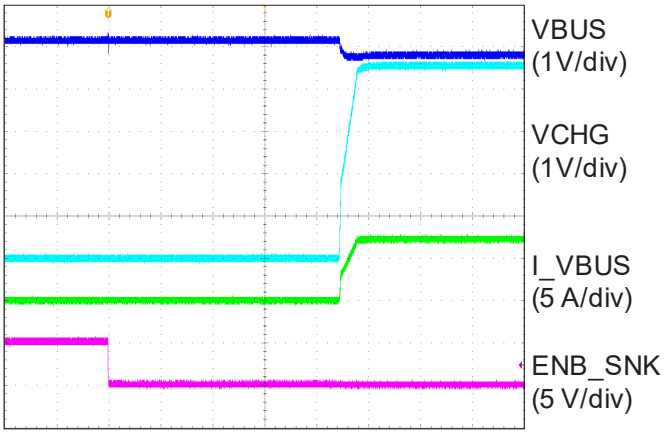


Figure 7. Over-Voltage Protection (OVP) Operation in Source Mode

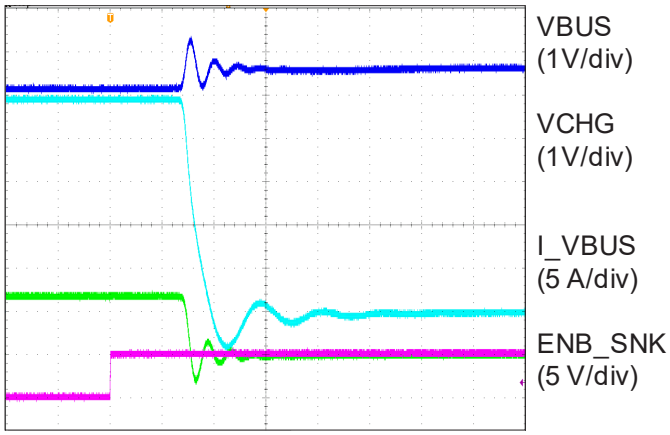
Typical Characteristics for Sink Mode

T_A = 25°C, VBUS = 20V, ENB_SNK = EN_SRC = 0V, C_{VBUS} = 10µF, C_{VCHG} = 10µF, C_{SS} = 5.6nF, C_{CAP} = 1nF, unless otherwise specified.

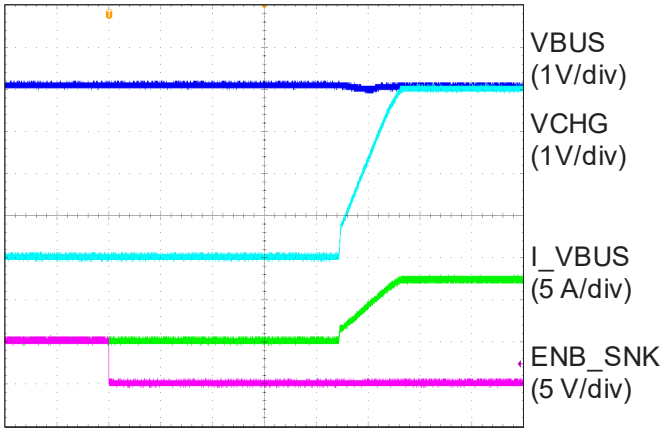
Soft-Start Ramp
(V_{BUS}=5V, I_{LOAD}=8A)



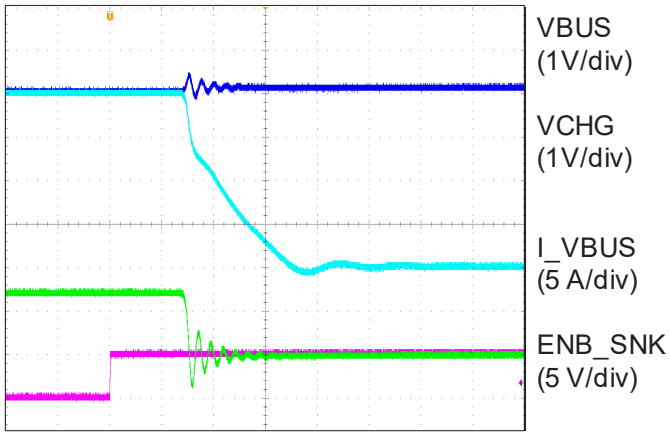
Shutdown
(V_{BUS}=5V, I_{LOAD}=8A)



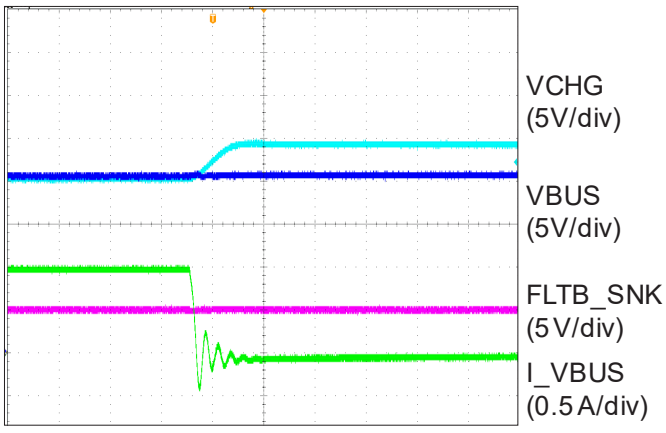
Soft-Start Ramp
(V_{BUS}=20V, I_{LOAD}=8A)



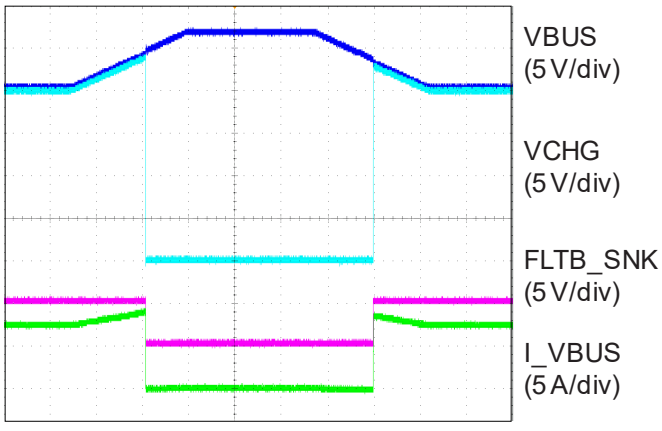
Shutdown
(V_{BUS}=20V, I_{LOAD}=8A)



Ideal Diode True Reverse Current Blocking



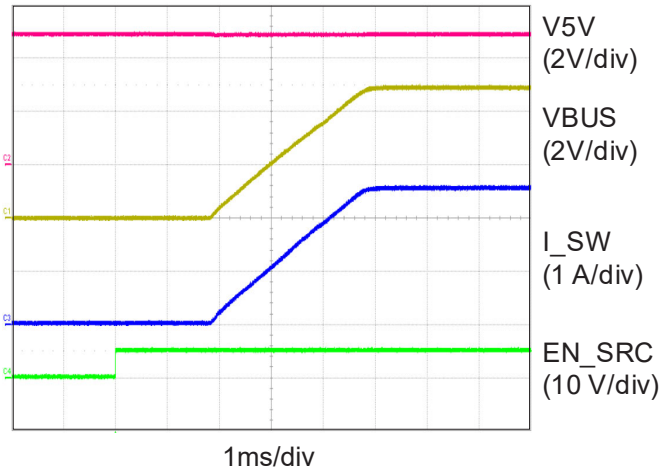
Sink Mode Over-Voltage Protection



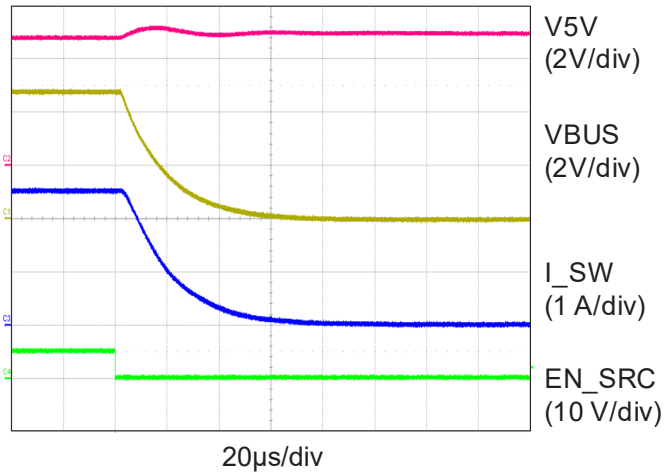
Typical Characteristics for Source Mode

T_A = 25°C, ENB_SNK = EN_SRC = 5V, FON = 0V, C_{VBUS} = 10µF, C_{V5V} = 80µF, R_{LIM} = 4.75kΩ, C_{CAP} = 1nF, Load = 1.9Ω, unless otherwise specified.

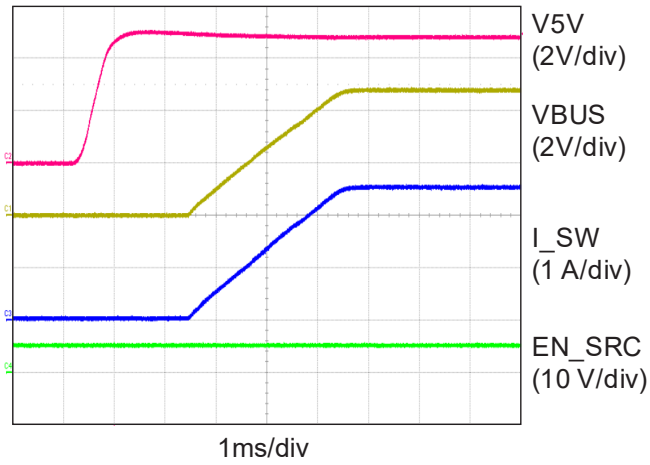
Source Mode Start Up by Enable



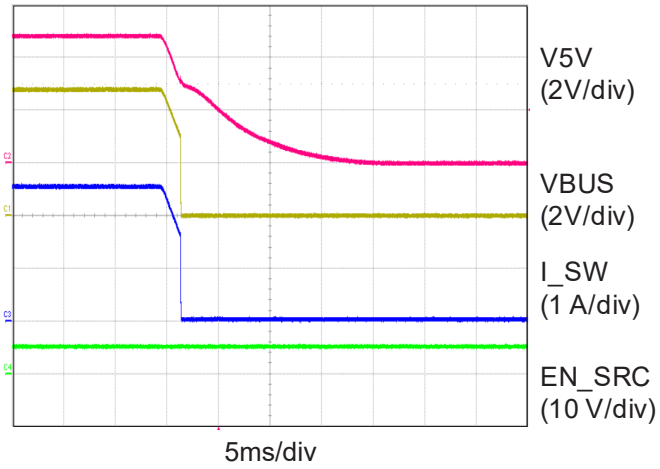
Source Mode Shutdown by Disable



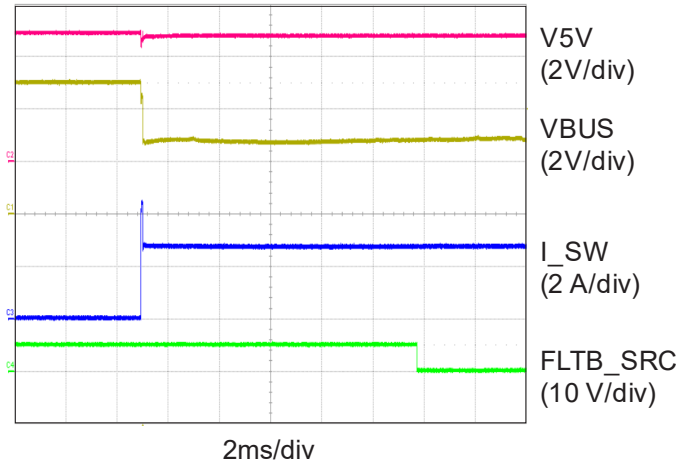
Source Mode Start Up by V5V Ramp



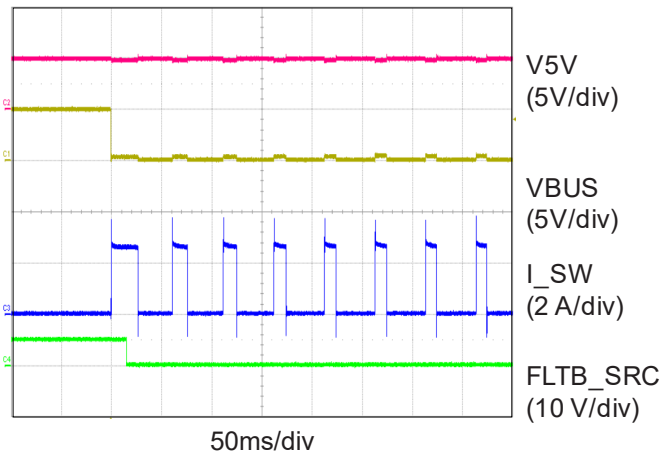
Source Mode Shutdown by V5V Ramp



Source Mode Over Current Protection (Load = 1.2Ω)



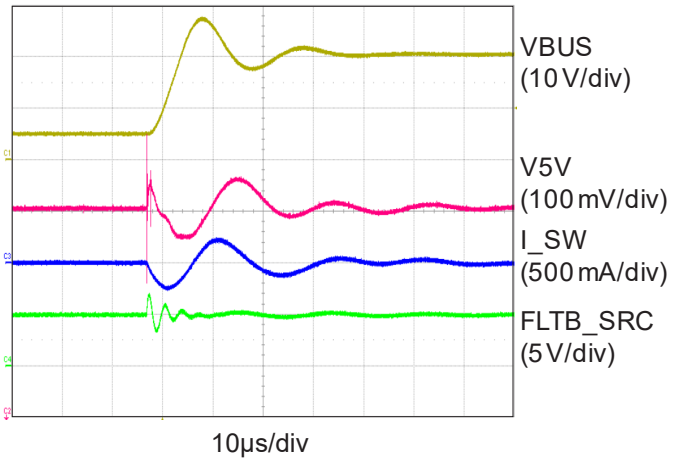
Source Mode Short Circuit Protection, Thermal Shutdown and Auto Restart



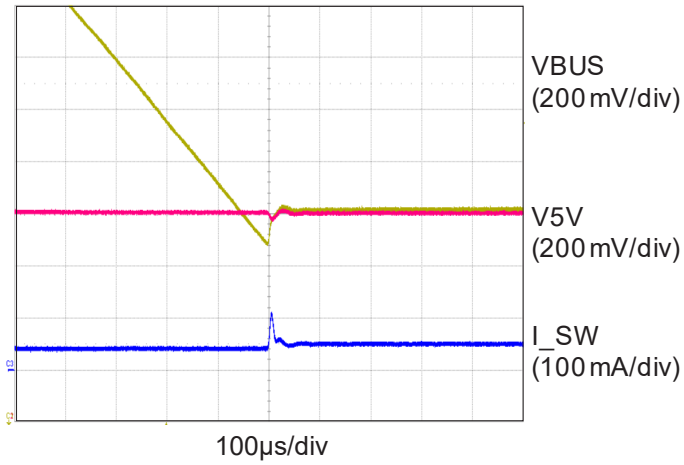
Typical Characteristics for Source Mode *(Continued)*

T_A = 25 °C, ENB_SNK = EN_SRC = 5 V, FON = 0V, C_{VBUS} = 10 µF, C_{V5V} = 80 µF, R_{LIM} = 4.75 kΩ, C_{CAP} = 1 nF, Load = 1.9Ω, unless otherwise specified.

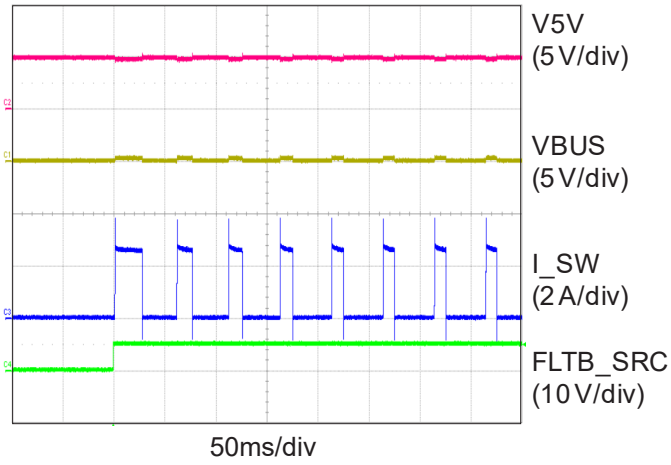
Source Mode Reverse Current Blocking



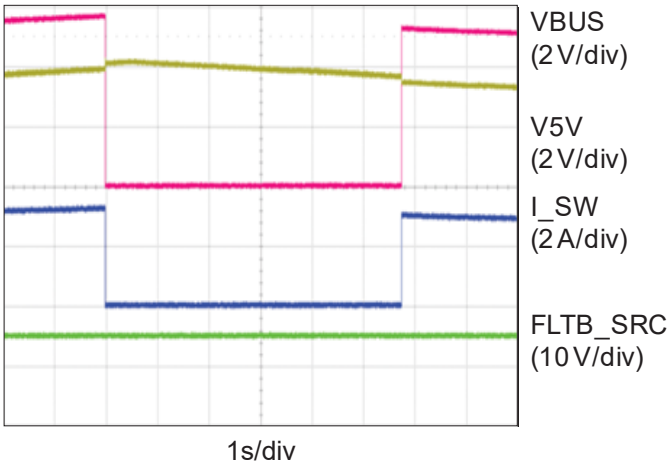
Source Mode Recovery from Reverse Current Blocking Release



Source Mode Start Up to Short Condition



Source Mode Over Voltage Protection



Functional Description

AOZ1382DI-01 can operate in both sink and source mode as selected by ENB_SNK and EN_SRC. Only one mode can be active at any time. The sinking mode acts as a load for the USB Type-C connector. It passes current from the connector (VBUS) to the output supply (VCHG). The sourcing mode acts as a power supply for the connector. It passes current from (V5V) to the connector (VBUS).

Sink Mode

The sinking mode power switch consists of a back-to-back connected N-channel MOSFET. It is capable of operating from 3.4 V to 23 V and rated up to 10 A of DC current and 20 A of pulsed current (10 ms @ 2% duty cycle). It features adjustable soft-start, over-voltage, under-voltage, and over temperature protections.

When the switch is enabled, the overall resistance between VBUS (input voltage) and VCHG (output voltage) is 20 mΩ, minimizing power lose and thermal dissipation. The back-to-back configuration of MOSFET completely isolates VBUS from VCHG when turned off or when VCHG > VBUS, preventing leakage current back to VBUS pin of the connector.

The AOZ1382DI-01 is a high-side protection switch with programmable soft-start, over-voltage, and over-temperature protections. The Ideal diode TRCB allows multi-port solution for system power flexibility.

Power Delivery Capability

During start-up, the voltage at VCHG linearly ramps up to the VBUS voltage over a period of time set by the soft-start time. This ramp time is referred to as the soft-start time and is typically in milliseconds. Figure 8 illustrates the soft-start condition and power dissipation.

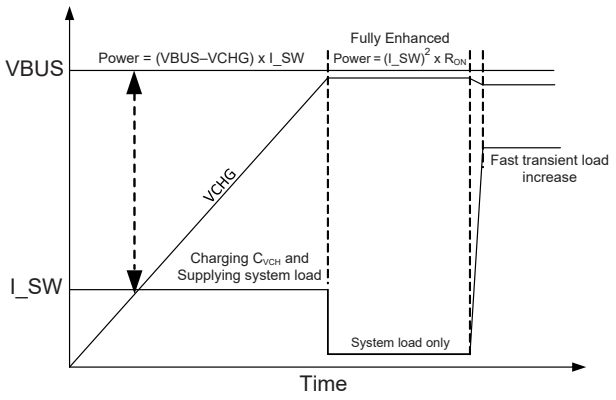


Figure 8. Soft-Start Power Dissipation

During this soft-start time, there will be a large voltage across the power switch. Also, there will be current I_SW through the switch to charge the output capacitance. In addition, there may be load current to the downstream system as well. This total current is calculated as:

$$I_{SW} = C_{VCHG}\left(\frac{dVCHG}{dt}\right) + I_{SYS}$$

In the soft-start condition, the switch is operating in the linear mode, and power dissipation is high. The ability to handle this power is largely a function of the power MOSFET linear mode SOA and good package thermal performance θ_{JC} (Junction-to-Case) as the soft-start ramp time is in milliseconds. θ_{JA} (Junction-to-Ambient), which is more a function of PCB thermal performance, doesn't play a role.

With a high-reliability MOSFET as the power switch and superior packaging technology, the AOZ1382DI-01 is capable of dissipating this power. The power dissipated is:

$$Power\ Dissipation = I\_SW \times (VBUS - VCHG)$$

To calculate the average power dissipation during the soft-start period: ½ of the input voltage should be used as the output voltage will ramp towards the input voltage, as shown in Figure 8.

For example, if the output capacitance COUT is 10 µF, the input voltage VBUS is 20 V, the soft-start time is 2 ms, and there is an additional 1 A of system current (I_SYS), then the average power being dissipated by the part is:

$$I_{SW} = 10\ \mu F\left(\frac{20\ V}{2\ ms}\right) + 1\ A = 1.1\ A$$

$$Average\ Power\ Dissipation = 1.1\ A \times \frac{20\ V}{2}$$

$$= 11\ W$$

Referring to the SOA curve in Figure 9, the maximum power allowed for 2ms is 120W (6A x 20V or 12A x 10V). The AOZ1382DI-01 power switch is robust enough to drive a large output capacitance with load in reasonable soft-start time.

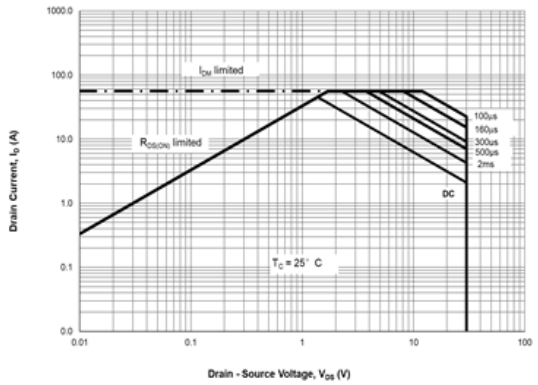


Figure 9. Safe Operating Area (SOA) Curves for Power Switch

After soft-start is completed, the power switch is fully on, and it is at its lowest resistance. The power switch acts as a resistor. Under this condition, the power dissipation is much lower than the soft-start period. However, as this is a continuous current, a low on-resistance is required to minimize power dissipation. Attention must be paid to board layout so that losses dissipated in the sinking switch are dissipated to the PCB and hence the ambient.

With a low on-resistance of 20mΩ, the AOZ1382DI-01 provides the most efficient power delivery without much resistive power dissipation.

While Type C power delivery is limited to 20V @ 5A or a 100W, many high-end laptops require peak currents far in excess of the 5A. While the thermal design current (TDC) for a CPU may be low, peak current (ICCmax in the case of Intel and EDP in the case of AMD) of many systems is often 2 x thermal design current. These events are typical of short duration (< 2ms) and low duty cycle, but they are important for system performance as a CPU/GPU capable of operating at several GHz can boost its compute power in those 2ms peak current events. The AOZ1382DI-01 can handle such short, high current, transient pulses without any reliability degradation, thus enhancing the performance of high-end systems when plugged into the Type C adaptor. The shorter the pulse and the lower the duty cycle, the higher the pulse current that the part can sustain. The part has enough time to dissipate the heat generated from the pulse current with longer off-time, as shown in Figure 10. For example, AOZ1382DI-01 can maintain 20A for 10ms with a duty cycle of 2%.

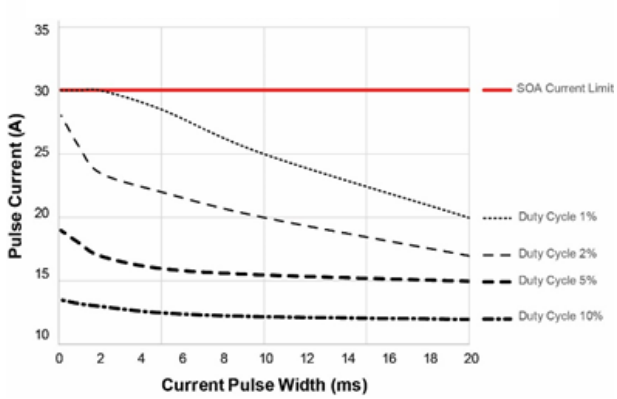


Figure 10. AOZ1382DI-01 Sinking Switch Pulsed Current vs. Duration for a Given Duty Cycle

Enable (ENB_SNK)

The active low ENB_SNK pin is the ON/OFF control for the power switch. The device is enabled when the EN pin is low and not in UVLO state. The EN pin must be driven to a logic high (OFF) ($V_{ENB\_SNK\_H}$) or logic low (ON) ($V_{ENB\_SNK\_L}$) state to guarantee operation. AOZ1382DI-01 draws about 32µA supply current when it is disabled.

Input Under-Voltage Lockout (UVLO)

The internal control circuit is powered from VBUS. The under-voltage lockout (UVLO) circuit monitors the voltage at the input pin (VBUS) and only allows the power switches to turn on when it is higher than 3.35V (V_{UVLO_SNK}).

Over-Voltage Protection (OVP)

The voltages at VBUS pin are constantly monitored once the device is enabled. In case the voltage exceeds the OVLO threshold, over-voltage protection is activated:

1. If the power switch is on, it will be turned off after OVP debounce time ($t_{OVLO\_DEB\_SNK}$) to isolate VCHG from VBUS;
2. OVP will prevent power switch to be turned on if it is in off state;

In either case FLTB_SNK pin is pulled low to report the fault condition. The device will restart once the OVP condition no longer exists.

Ideal Diode True Reverse Current Blocking (IDTRCB)

When the device is ON with no load or under light load conditions, it regulates VCHG to be 35mV below VBUS. As the load current is increasing or decreasing, the device adjusts the gate drive to maintain the 35mV drop from VBUS to VCHG. As the load current continues to increase the device increases the gate drive until the gate is fully turned on

and VBUS to VCHG drop is determined by IR drop through the MOSFET. If for any reason VCHG increases such that VBUS to VCHG drop to less than 0 V, the gate driver forces the switch to turn off. The 35 mV VBUS to VCHG regulation ensures no reverse current flow under any conditions.

When the AOZ1382DI-01 is first enabled or during each auto-restart, power switch will be kept off if VCHG > VBUS.

Thermal Shutdown Protection (TSD)

When the die temperature reaches 140°C (T_{TSD_SNK}), the power switch is turned off. The device will be re-enabled once the temperature drop by the hysteresis threshold ($T_{TSD\_SNK\_HYS}$).

Soft-Start Slew-Rate Control

When ENB_SNK pin is asserted low, the slew rate control applies voltage on the gate of the power switch in a manner such that the output voltage is ramped up linearly until VCHG reaches VBUS voltage level. The output ramps up time (t_{ON_SNK}) is programmable by an external soft-start capacitor (C_{SS}). The following formula provides the estimated 10% to 90% ramp up time.

$$t_{ON\_SNK} = \left(\frac{VBUS}{24}\right) \times \left[\left(\frac{C_{SS}}{0.0023}\right) - 100\right]$$

where C_{SS} is in nF and t_{ON_SNK} is in µs.

System Startup

The device is enabled when ENB_SNK is low and VBUS is higher than UVLO threshold (V_{UVLO_SNK}). The device will check if any fault condition exists. If no fault exists, the power switch is turned on and VCHG is then ramped up after enable delay ($t_{DLY\_ON\_SNK}$), controlled by the soft-start time (t_{ON_SNK}) until VCHG reaches VBUS voltage level. Soft start time can be programmed externally through SS input with a capacitor C_{SS} to control in-rush current.

Fault Protection

The AOZ1382DI-01 offers multiple protection against the following fault conditions: VBUS over-voltage (OVLO), True Reverse Current Blocking (TRCB) when VCHG > VBUS, and over temperature.

When the device is first enabled, the power switch is off and fault conditions are checked if any of these conditions exist:

1. VBUS is higher than the OVP threshold (V_{OVLO_SNK});
2. TRCB when VCHG > VBUS
3. Die temperature is higher than thermal shutdown threshold (T_{TSD_SNK});

The power switch will not be turned on and FLTB_SNK pin will be pulled low to indicate fault status of the device when OVP and/or TSD occur.

After the power switch turns on, the device will continuously monitor these fault conditions.

Auto-restart after TRCB, OVP, TSD Faults

AOZ1382DI-01 power switch is turned off under fault protection. If it is TRCB fault condition and VCHG is out of RCB condition, the device will restart when VBUS > VCHG.

The AOZ1382DI-01 will auto restart after t_{REC_SNK} when Over-Voltage Protection (OVP) and Thermal Shut Down Protection (TSD) fault conditions are removed.

VBUS Capacitor Selection

The input capacitor prevents large voltage transients from appearing at the input, and provides the instantaneous current needed each time the switch turns on to charge output capacitors and to limit input voltage drop. It is also to prevent high-frequency noise on the power line from passing through to the output. The input capacitor should be located as close to the pin as possible. A 10 µF ceramic capacitor is recommended. The USB specification limits the capacitance on VBUS to a maximum of 10 µF. Use this maximum value for noise immunity due to the system and cable plug/unplug transients.

VCHG Capacitor Selection

The VCHG capacitor for sinking path has to supply enough current for a large load that it may encounter during system transient. This bulk capacitor must be large enough to supply fast transient load in order to prevent the output from dropping.

If VCHG capacitor is too large and the output voltage is lower than approximately 300 mV of the input voltage at the end of soft-start-time, short-circuit protection will be triggered to turn-off the power switch.

Power Dissipation Calculation

The following equation can be used to estimate the power dissipation for normal load condition:

$$Power\ Dissipated = R_{ON\_SNK} \times (I_{VBUS})^2$$

Source Mode

The sourcing mode power switch consists of a back-to-back connected N-channel MOSFET. It is capable of operating from 3.4V to 5.5V and rated up to 3.5A. It features adjustable current limit, over-voltage, under-voltage, and over temperature protections.

When the switch is enabled, the overall resistance between V5V and VBUS is 39mΩ, minimizing power lose and thermal dissipation. The back-to-back configuration of MOSFET completely isolates VBUS from V5V when turned off or when VBUS > V5V, preventing leakage current back to VBUS pin of the connector.

Enable (EN_SRC)

The active high EN_SRC is the enable control for the sourcing power path. The device is enabled when EN_SRC input is high and device is not in the UVLO state. The EN_SRC must be driven to a logic low ($V_{EN\_SRC\_L}$) or logic high ($V_{EN\_SRC\_H}$) to guarantee operation. While disabled, the AOZ1382DI-01 only draws about 6µA supply current.

Input Under-Voltage LockOut (UVLO)

The internal circuitry of sourcing path is powered from V5V. The Under-Voltage Lockout (UVLO) circuit monitors the voltage at the V5V pin and only allows the power switch to turn on when V5V is higher than V_{UVLO_SRC}.

Over-Voltage Protection (OVP)

The voltage at the V5V is constantly monitored once the device is enabled. In case the input voltage exceeds the over-voltage lockout threshold (V_{OVLO_SRC}), the power switch is either turned off immediately or kept off, depending on its initial state. The AOZ1382DI-01 can restart when V5V drops $V_{OVLO\_SRC\_HYS}$ below.

Over-Current Protection (OCP)

The sourcing path features adjustable current limit to prevent over-current condition. An external resistor R_{ILIM} connected between ILIM and GND pins sets the over-current protection threshold.

The current limit threshold can be estimated using the equation below:

$$I_{LIM} = \frac{14300}{R_{LIM}} \ (A)$$

For example, for 1A current limit threshold, a 14.3kΩ RLIM resistor should be selected. 1% resistor is recommended for R_{LIM}.

Under current-limiting, FLTB_SRC is pulled low after delay ($t_{OCP\_FLTB\_SRC}$). Severe overload causes excessive power dissipation and die temperature might increase and may trigger thermal shutdown.

Short Circuit Protection (SCP)

A short circuit condition will cause the chip to clamp the current to the programmed limit value. The short circuit condition will cause large power dissipation in the switches which will cause an over temperature condition.

True Reverse Current Blocking (TRCB)

True Reverse Current Blocking (TRCB) prevents undesired current flow from output to input when the power switch is in either on or off state. When the device is enabled, the power switch is quickly turned off if VBUS voltage is higher than V5V voltage. The power switch is turned on again when the VBUS voltage falls below V5V by 40mV.

Soft Start

The AOZ1382DI-01 has internal soft-start circuitry for sourcing mode to limit in-rush current due to a large capacitive load. By default, the turn-on time is 2.7ms.

In case of fast turn-on (FON is logic high) or fast recovery from TRCB, soft-start is disabled to ensure the output rises quickly.

Fast Role Swap (FRS)

The FON input control allows the power switch to turn on quickly. FON should be asserted before the device is enabled. If V5V > VBUS, the power switch turns on quickly by minimizing the turn on delay and disabling the internal soft-start. Over-current protection is disabled during fast turn-on. If VBUS > V5V (VBUS pre-biased), the device is enabled but true reverse blocking protection (TRCB) keeps the power switch off to prevent the V5V from being pulled to the higher VBUS voltage. The power switch is kept off until the TRCB event is removed.

Fast Recovery from TRCB

Once the TRCB event is removed, the power switch turns on again quickly. The recovery time is less than 80µs soft-start is not active during fast recovery.

Thermal Shutdown (TSD)

In the event of over temperature, FLTB_SRC pin will pull low and the switches will open. Once the device temperature drops below the hysteresis and the short circuit still exists, it will try to turn on the switch again but FLTB_SRC will keep low to indicate fault conditions. FLTB_SRC will only be released if both TSD and OCP conditions are not active.

V5V Capacitor Selection

The V5V capacitor for sourcing path prevents large voltage transients from appearing at the input, and provides the instantaneous current needed each time the switch turns on to charge output capacitors and to limit input voltage drop. It is also to prevent high-frequency noise on the power line from passing through to the output. The V5V capacitor should be located as close to the pin as possible. A 20 µF ceramic capacitor is recommended. However, higher capacitor values further reduce the transient voltage drop at the input.

Layout Guidelines

AOZ1382DI-01 is a protection switch designed deliver high current. Layout is critical to remove the heat generated by this current. For the most efficient heat sinking, connect as much copper as possible to the exposed pad. The exposed pad is the common drain of the power switch which must be electrically isolated.

On the top layer expand the exposed pad island as much as possible for optimal thermal performance. The exposed pad copper plane must be electrically isolated. See example in Figure 11.

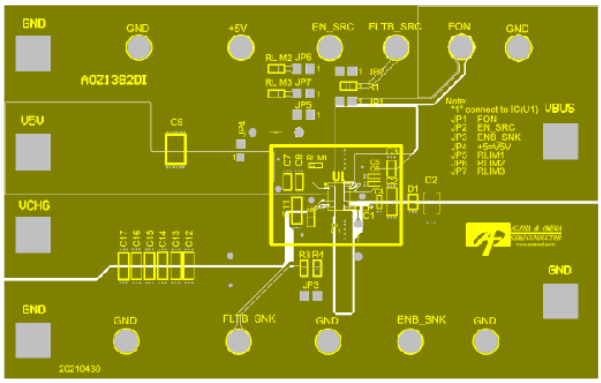


Figure 11. Top layer layout. Maximum number of VIAs from top layer exposed pad to inner layer.

There are two ways to create thermal islands on the inner layers. If the layer is flooded with a plane an isolated pad may be etched out as showed in Figure 12. If there are no flooded planes then an isolated island may be created as showed in Figure 13. The more layers that have these electrically isolated thermal heat sink islands the better the thermal performance will be. Connect all isolated thermal island (top, inner layers and bottom) together with as many VIAs as possible.

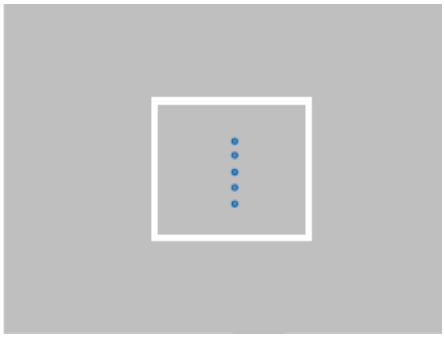


Figure 12. Inner layer layout. Create an isolated island with no flooded plane.

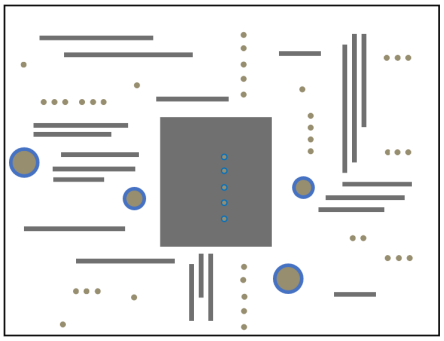


Figure 13. Inner layer layout. Create an isolated island with no flooded plane.

On the bottom layer, similar to the inner layers, create an isolated thermal island. Typically, there is more area available on the bottom area for a larger thermal pad. The top and bottom layers have better thermal performance than the inner layers because they are exposed to the atmosphere. See example in Figure 14.

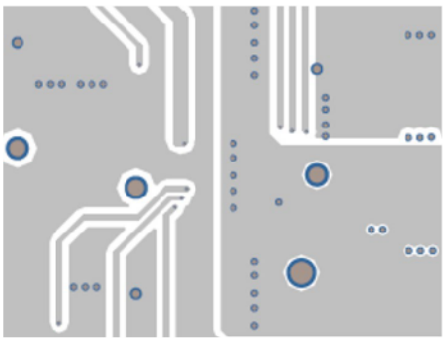
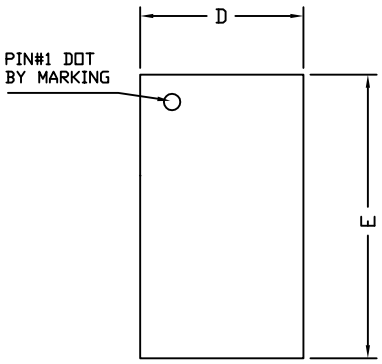
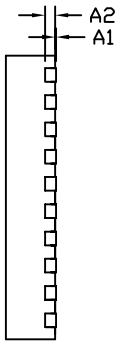


Figure 14. Bottom layer layout. Create a large electrically isolated thermal pad.

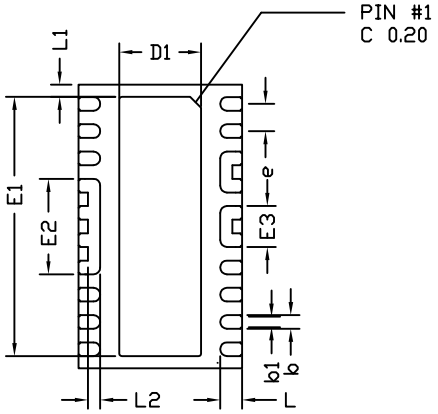
Package Dimensions, DFN3x5.2-20L



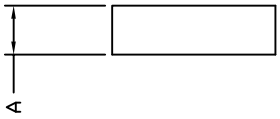
TOP VIEW



SIDE VIEW



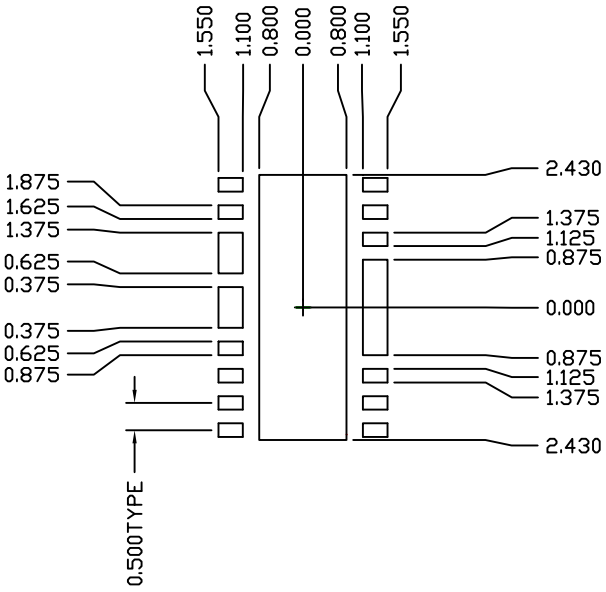
BOTTOM VIEW



SIDE VIEW

SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.850	0.900	0.950	0.033	0.035	0.037
A1	0.000	–	0.050	0.000	–	0.002
A2		0.2REF			0.008REF	
D	2.900	3.000	3.100	0.114	0.118	0.122
E	5.100	5.200	5.300	0.201	0.205	0.209
D1	1.450	1.500	1.550	0.057	0.059	0.061
E1	4.710	4.760	4.810	0.185	0.187	0.189
E2	1.700	1.750	1.800	0.067	0.069	0.071
E3	0.700	0.750	0.800	0.028	0.030	0.031
L	0.350	0.400	0.450	0.014	0.016	0.018
L1	0.170	0.220	0.270	0.007	0.009	0.011
L2	0.174	0.224	0.274	0.007	0.009	0.011
b	0.200	0.250	0.300	0.008	0.010	0.012
b1	0.140	0.190	0.240	0.006	0.007	0.009
e		0.50BSC			0.02BSC	

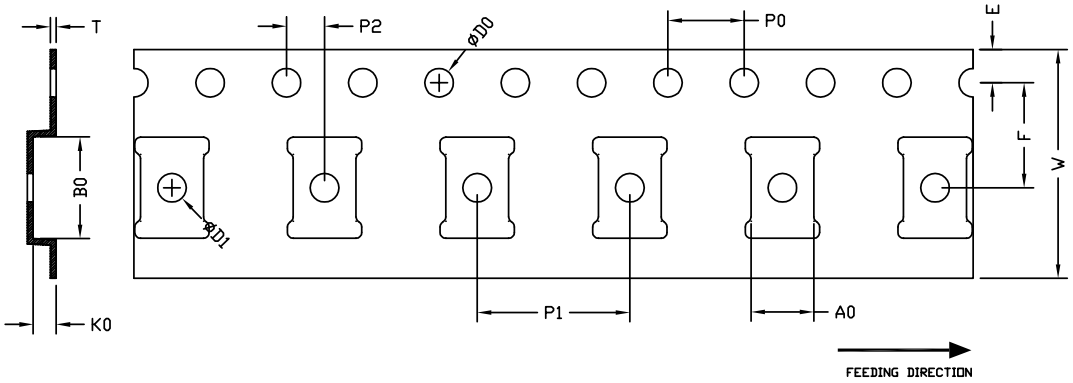
RECOMMENDED LAND PATTERN



NOTE
CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

Tape and Reel Dimensions, DFN3x5.2-20L

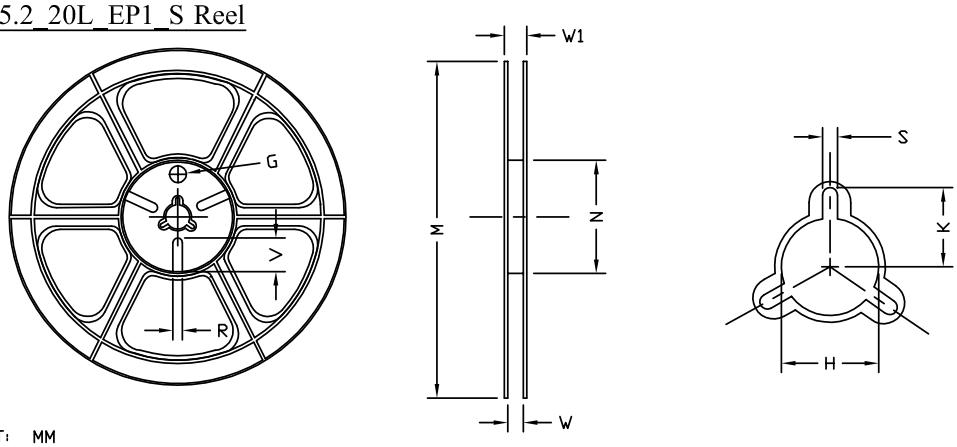
DFN3x5.2_20L_EP1_S Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	W	E	F	P0	P1	P2	T
DFN3x5.2	3.30 ±0.1	5.50 ±0.1	1.20 ±0.1	Ø1.50 +0.1 −0.0	Ø1.50 +0.2 −0.0	12.00 +0.3 −0.1	1.75 ±0.1	5.50 ±0.05	4.00 ±0.1	8.00 ±0.1	2.00 ±0.05	0.30 ±0.03

DFN3x5.2_20L_EP1_S Reel



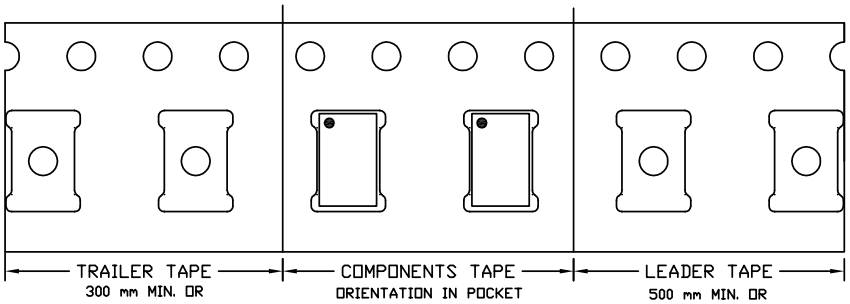
UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	Ø330	Ø330.00 ±0.50	Ø97.00 ±0.10	13.00 ±0.30	17.40 ±1.00	Ø13.00 +0.50 −0.20	10.60	2.00 ±0.50	---	---	---

DFN3x5.2_20L_EP1_S Package Tape

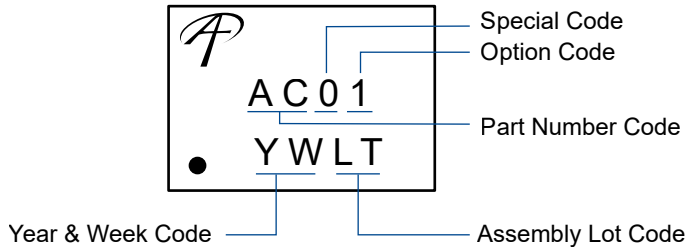
Leader / Trailer & Orientation

Unit Per Reel: 5000pcs



Part Marking

AOZ1382DI-01
(DFN3x5.2)



LEGAL DISCLAIMER

Applications or uses as critical components in life support devices or systems are not authorized. Alpha and Omega Semiconductor does not assume any liability arising out of such applications or uses of its products. AOS reserves the right to make changes to product specifications without notice. It is the responsibility of the customer to evaluate suitability of the product for their intended application. Customer shall comply with applicable legal requirements, including all applicable export control rules, regulations and limitations.

AOS's products are provided subject to AOS's terms and conditions of sale which are set forth at:
http://www.aosmd.com/terms_and_conditions_of_sale

LIFE SUPPORT POLICY

ALPHA AND OMEGA SEMICONDUCTOR PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.