# DSC12X2/3/4

## High Performance Differential MEMS Oscillators

### Features

- Very Low RMS Phase Jitter: <650 fs (typ.)
- High Stability: ±20 ppm, ±25 ppm, ±50 ppm
- Wide Temperature Range:
  - Automotive: –40°C to +125°C (DSC12x LVDS Only)
  - Ext. Industrial: –40°C to +105°C
  - Industrial: –40°C to +85°C
  - Commercial: –20°C to +70°C
- Supports LVPECL, LVDS, or HCSL Differential Outputs
- PCIe Gen1-6 Compliant Output
- Wide Frequency Range: 2.5 MHz to 450 MHz
- Small Industry Standard Footprints:
  - 2.5 mm x 2.0 mm
  - 3.2 mm x 2.5 mm
  - 5.0 mm x 3.2 mm
  - 7.0 mm x 5.0 mm
- Excellent Shock and Vibration Immunity
  - Qualified to MIL-STD-883
- High Reliability
  - 20x Better MTF than Quartz Oscillators
- Supply Range of 2.25 to 3.6V
- Standby, Frequency Select, and Output Enable Functions
- Lead-Free and RoHS Compliant

### Applications

- Storage Area Networks
- Passive Optical Networks
- 10/100G Ethernet
- HD/SD/SDI Video and Surveillance
- PCI Express Gen 1/2/3/4/5/6
- Display Port

### General Description

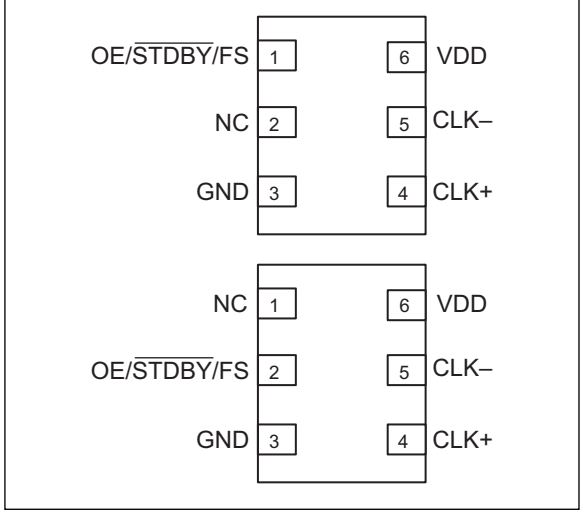
The DSC12x2/3/4 family of high performance oscillators utilizes the latest generation of silicon MEMS technology that reduces close-in noise and provides excellent jitter and stability over a wide range of supply voltages and temperatures. By eliminating the need for quartz or SAW technology, MEMS oscillators significantly enhance reliability and accelerate product development, while meeting stringent clock performance criteria for a variety of communications, storage, and networking applications.

The DSC12x2/3/4 family features a control function on pin 1 or pin 2 that permits either a standby feature (complete power down when $\overline{\text{STDBY}}$ is low), output enable (output is tri-stated with OE low), or a frequency select (choice of two frequencies selected by FS high/low). See the Product Identification System section for detailed information.

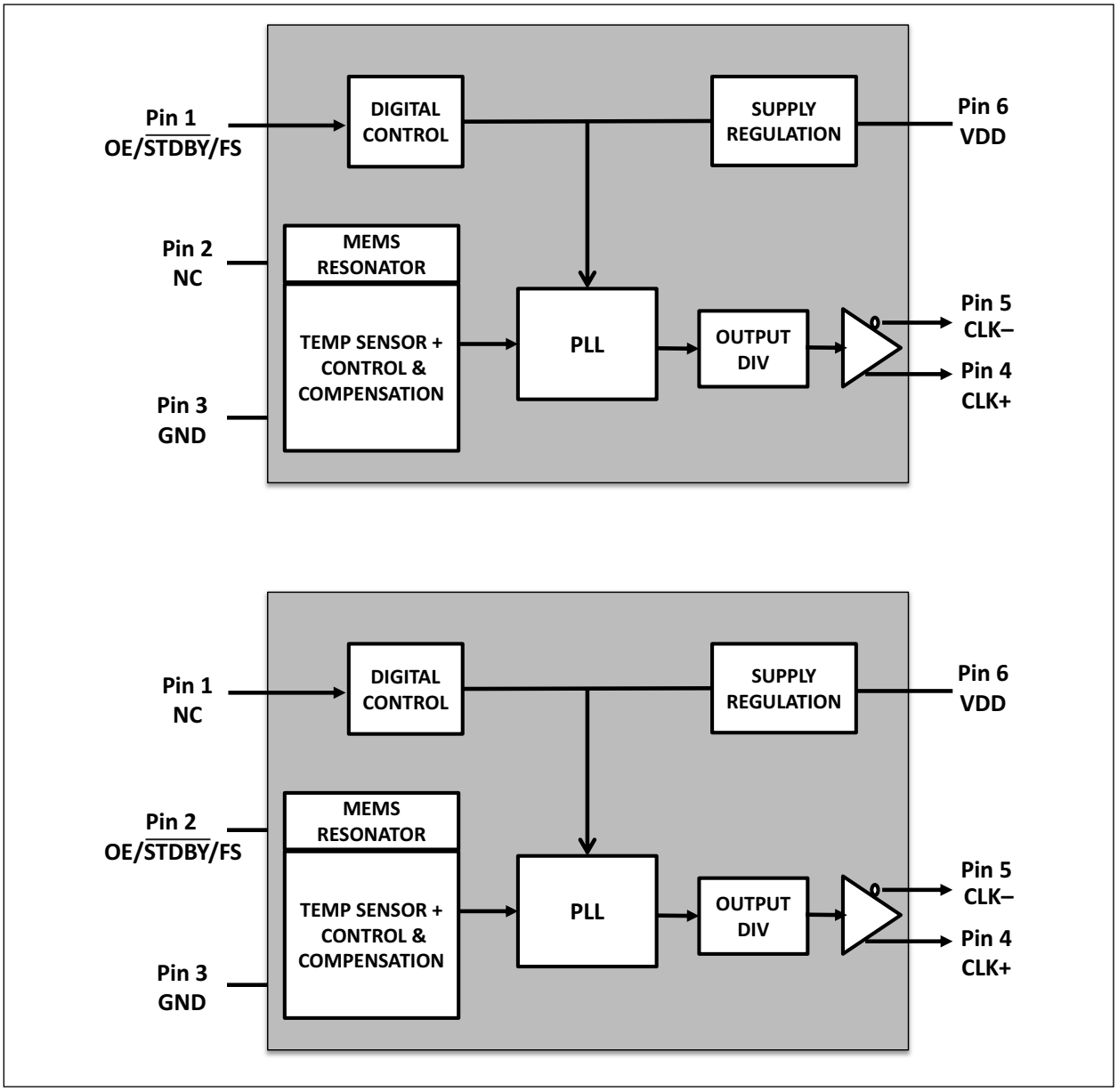
All oscillators are available in industry-standard packages, including the small 2.5 mm x 2.0 mm, and are “drop-in” replacements for standard 6-pin LVPECL/LVDS/HCSL crystal oscillators.

### Package Types

**DSC12x2/3/4**
6-Lead CDFN/VDFN



### Functional Block Diagrams



# 1.0 ELECTRICAL CHARACTERISTICS

## Absolute Maximum Ratings †

Supply Voltage ..... –0.3V to +4.0V
Input Voltage ..... –0.3V to $V_{DD}$ + 0.3V
ESD Protection (HBM) ..... 4 kV
ESD Protection (MM) ..... 400V
ESD Protection (CDM) ..... 1.5 kV

**† Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

**Electrical Characteristics:** $V_{DD}$ = 2.5V ±10% or 3.3V ±10%; $T_A$ = –40°C to +105°C, unless noted.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 2.25 | — | 3.63 | V | Note 1 |
| Supply Current | $I_{DD}$ | — | 50 | — | mA | LVPECL, $f_{OUT}$ = 100 MHz |
| | | — | 32 | — | | LVDS, $f_{OUT}$ = 100 MHz |
| | | — | 40 | — | | HCSL, $f_{OUT}$ = 100 MHz |
| | | — | 23 | — | | Output disabled (tri-state), $f_{OUT}$ = 100 MHz |
| Standby Current | $I_{STDBY\_}$ | — | 2.5 | 5 | µA | Input pin = $\overline{\text{STDBY}}$ = Asserted, ($V_{DD}$ = 3.3V) |
| Frequency Stability | Δf | — | — | ±20 | ppm | Includes frequency variations due to initial tolerance, temp., and power supply voltage |
| | | — | — | ±25 | | |
| | | — | — | ±50 | | |
| Aging | Δf | — | — | ±5 | ppm | First year @ 25°C |
| | | — | — | ±1 | | Per year after first year |
| Startup Time | $t_{SU}$ | — | 5.5 | 6 | ms | From 90% $V_{DD}$ to valid clock output, T = +25°C, Note 2 |
| Input Logic Levels | $V_{IH}$ | 0.75 x $V_{DD}$ | — | — | V | Input logic high |
| | $V_{IL}$ | — | — | 0.25 x $V_{DD}$ | | Input logic low |
| Output Disable Time | $t_{DA}$ | — | — | 25 | ns | Note 3 |
| Output Enable Time | $t_{EN}$ | — | — | 6 | ms | $\overline{\text{STDBY}}$ |
| | | — | — | 350 | ns | OE |
| Enable Pull-Up Resistor | — | — | 1.5 | — | MΩ | Pull-up resistor on pin 1, Note 4 |

**Note 1:** $V_{DD}$ pin should be filtered with 0.1 µF capacitor.
**2:** $t_{SU}$ is time to 100 ppm stable output frequency after $V_{DD}$ is applied and outputs are enabled.
**3:** $t_{DA}$: See the Output Waveforms and the Test Circuits sections for more information.
**4:** Output is enabled if pad is floated (not connected).
**5:** Jitter limits are established by Gen 1.1, Gen 2.1, and Gen 3.0 PCIe standards.

## ELECTRICAL CHARACTERISTICS (CONTINUED)

**Electrical Characteristics:** $V_{DD}$ = 2.5V ±10% or 3.3V ±10%; $T_A$ = –40°C to +105°C, unless noted.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **LVPECL (DSC12x2)** | | | | | | |
| Frequency | $f_0$ | 2.5 | — | 450 | MHz | — |
| Output Logic Levels | $V_{OH}$ | $V_{DD}$ – 1.145 | — | — | V | $R_L$ = 50Ω |
| | $V_{OL}$ | — | — | $V_{DD}$ – 1.695 | | |
| Peak-to-Peak Output Swing | $V_{PP}$ | — | 800 | — | mV | Single-Ended |
| Output Transition Time | $t_R$ | — | 200 | 250 | ps | 20% to 80%, $R_L$ = 50Ω |
| | $t_F$ | — | 250 | 300 | | |
| Output Duty Cycle | SYM | 48 | — | 52 | % | Differential |
| Period Jitter RMS | $J_{PER}$ | — | 2.0 | — | ps | $f_0$ = 156.25 MHz, 10k cycles |
| Period Jitter Peak-to-Peak | $J_{PTP}$ | — | 20 | — | ps | $f_0$ = 156.25 MHz, 10k cycles |
| Integrated Phase Noise (Random) | $J_{PH}$ | — | 0.65 | — | $ps_{RMS}$ | 12 kHz to 20 MHz @156.25 MHz |
| **LVDS (DSC12x3)** | | | | | | |
| Frequency | $f_0$ | 2.3 | — | 450 | MHz | — |
| Output Offset Voltage | $V_{OS}$ | 1.15 | 1.25 | 1.35 | V | R = 100Ω Differential |
| Peak-to-Peak Output Swing | $V_{PP}$ | 250 | 350 | 450 | mV | Single-Ended |
| Output Transition Time | $t_R$ | 120 | 170 | 220 | ps | 20% to 80%, $R_L$ = 100Ω |
| | $t_F$ | | | | | |
| Output Duty Cycle | SYM | 40 | — | 52 | % | Differential |
| Period Jitter RMS | $J_{PER}$ | — | 2.5 | — | ps | $f_0$ = 156.25 MHz, 10k cycles |
| Period Jitter Peak-to-Peak | $J_{PTP}$ | — | 20 | — | ps | $f_0$ = 156.25 MHz, 10k cycles |
| Period Jitter RMS | $J_{PER}$ | — | 3 | — | ps | $f_0$ = 156.25 MHz, $T_A$ = –40°C to +125°C |
| Period Jitter Peak-to-Peak | $J_{PTP}$ | — | 25 | — | ps | $f_0$ = 156.25 MHz, $T_A$ = –40°C to +125°C |
| Integrated Phase Noise (Random) | $J_{PH}$ | — | 0.65 | — | $ps_{RMS}$ | 12 kHz to 20 MHz @156.25 MHz, $T_A$ = –40°C to +105°C |
| | | — | 0.9 | — | | 2 kHz to 20 MHz @156.25 MHz, $T_A$ = –40°C to +105°C |
| Phase Jitter | $J_{RMS-CC}$ | — | 0.025 | 0.1 | $ps_{RMS}$ | PCIe Gen 6.0, 64 GT/s |

**Note 1:** $V_{DD}$ pin should be filtered with 0.1 µF capacitor.

**2:** $t_{SU}$ is time to 100 ppm stable output frequency after $V_{DD}$ is applied and outputs are enabled.

**3:** $t_{DA}$: See the Output Waveforms and the Test Circuits sections for more information.

**4:** Output is enabled if pad is floated (not connected).

**5:** Jitter limits are established by Gen 1.1, Gen 2.1, and Gen 3.0 PCIe standards.

## ELECTRICAL CHARACTERISTICS (CONTINUED)

**Electrical Characteristics:** $V_{DD}$ = 2.5V ±10% or 3.3V ±10%; $T_A$ = –40°C to +105°C, unless noted.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **HCSL (DSC12x4)** | | | | | | |
| Frequency | $f_0$ | 2.3 | — | 450 | MHz | — |
| Output Logic Levels | $V_{OH}$ | 0.64 | — | — | V | $R_L$ = 50Ω |
| | $V_{OL}$ | — | — | 0.1 | | |
| Peak-to-Peak Output Swing | $V_{PP}$ | — | 750 | — | mV | Single-Ended |
| Output Transition Time | $t_R$ | 200 | 260 | 400 | ps | 20% to 80%, $R_L$ = 50Ω |
| | $t_F$ | 250 | 370 | 500 | | |
| Output Duty Cycle | SYM | 48 | — | 52 | % | Differential |
| Period Jitter RMS | $J_{PER}$ | — | 2 | — | ps | $f_0$ = 100.00 MHz, 10k cycles |
| Period Jitter Peak-to-Peak | $J_{PTP}$ | — | 16 | — | ps | $f_0$ = 100.00 MHz, 10k cycles |
| Integrated Phase Noise (Random) | $J_{PH}$ | — | 0.617 | — | $ps_{RMS}$ | 12 kHz to 20 MHz @100 MHz $T_A$ = –40°C to +105°C |
| | | — | 0.460 | — | | 100 kHz to 20 MHz @100 MHz $T_A$ = –40°C to +105°C |
| | | — | 0.212 | — | | 1.875 MHz to 20 MHz @100 MHz $T_A$ = –40°C to +105°C |
| Phase Jitter | $T_J$ | — | 3.42 | 86 | $ps_{PP}$ | PCIe Gen 1.1, $T_J = D_J + 14.069 \times R_J$ (BER $10^{-12}$), Note 5 |
| | $J_{RMS-CCHF}$ | — | 0.247 | 3.1 | $ps_{RMS}$ | PCIe Gen 2.1, 1.5 MHz to Nyquist, Note 5 |
| | $J_{RMS-CCHF}$ | — | 0.08 | 3.0 | $ps_{RMS}$ | PCIeGen2.1,10 kHzto1.5 MHz, Note 5 |
| | $J_{RMS-CC}$ | — | 0.107 | 1.0 | $ps_{RMS}$ | PCIe Gen 3.0, Note 5 |
| | | — | 0.107 | 0.30 | | PCIe Gen 4.0, 16 GT/s |
| | | — | 0.043 | 0.12 | | PCIe Gen 5.0, 32 GT/s |
| | | — | 0.054 | 0.1 | | PCIe Gen 6.0, 64 GT/s |

**Note 1:** $V_{DD}$ pin should be filtered with 0.1 µF capacitor.

**2:** $t_{SU}$ is time to 100 ppm stable output frequency after $V_{DD}$ is applied and outputs are enabled.

**3:** $t_{DA}$: See the Output Waveforms and the Test Circuits sections for more information.

**4:** Output is enabled if pad is floated (not connected).

**5:** Jitter limits are established by Gen 1.1, Gen 2.1, and Gen 3.0 PCIe standards.

## TEMPERATURE SPECIFICATIONS (Note 1)

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Temperature Ranges** | | | | | | |
| Maximum Junction Temperature | $T_J$ | — | — | +150 | °C | — |
| Storage Temperature Range | $T_S$ | –55 | — | +150 | °C | — |
| Lead Temperature | — | — | — | +260 | °C | Soldering, 40 sec. |

**Note 1:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., $T_A$, $T_J$, $\theta_{JA}$). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.

## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1 and Table 2-2.

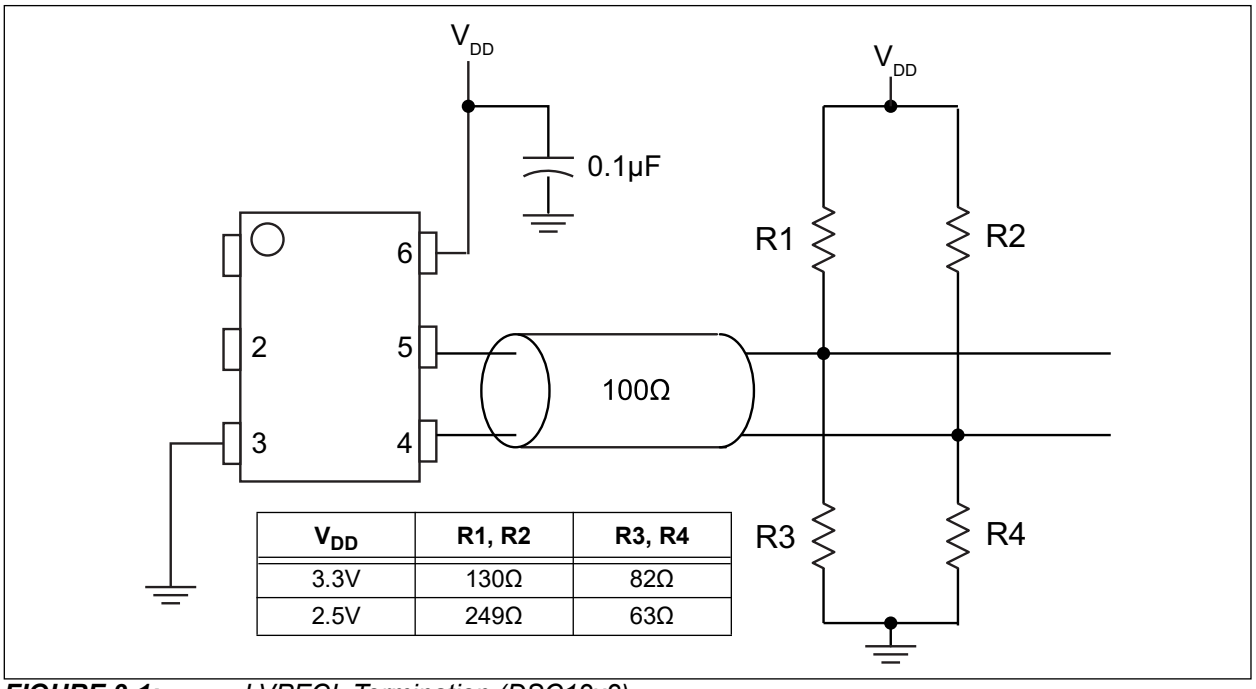
**TABLE 2-1: DSC120x/1x/2x PIN FUNCTION TABLE**

| Pin Number | Pin Name | Description |
|---|---|---|
| 1 | OE/$\overline{\text{STDBY}}$/FS | Control pin: Output enable/standby/frequency select. |
| 2 | NC | No connect. |
| 3 | GND | Power supply ground. |
| 4 | CLK+ | Clock output +. |
| 5 | CLK– | Clock output –. |
| 6 | VDD | Power supply. |

**TABLE 2-2: DSC123x/4x/5x PIN FUNCTION TABLE**

| Pin Number | Pin Name | Description |
|---|---|---|
| 1 | NC | No connect. |
| 2 | OE/$\overline{\text{STDBY}}$/FS | Control pin: Output enable/standby/frequency select. |
| 3 | GND | Power supply ground. |
| 4 | CLK+ | Clock output +. |
| 5 | CLK– | Clock output –. |
| 6 | VDD | Power supply. |

## 3.0 TERMINATION SCHEME




| $V_{DD}$ | R1, R2 | R3, R4 |
|---|---|---|
| 3.3V | 130Ω | 82Ω |
| 2.5V | 249Ω | 63Ω |

***FIGURE 3-1:*** *LVPECL Termination (DSC12x2).*

In Figure 3-1, Thevenin termination for 3.3V operation. Values will differ for $V_{DD}$ = 2.5V

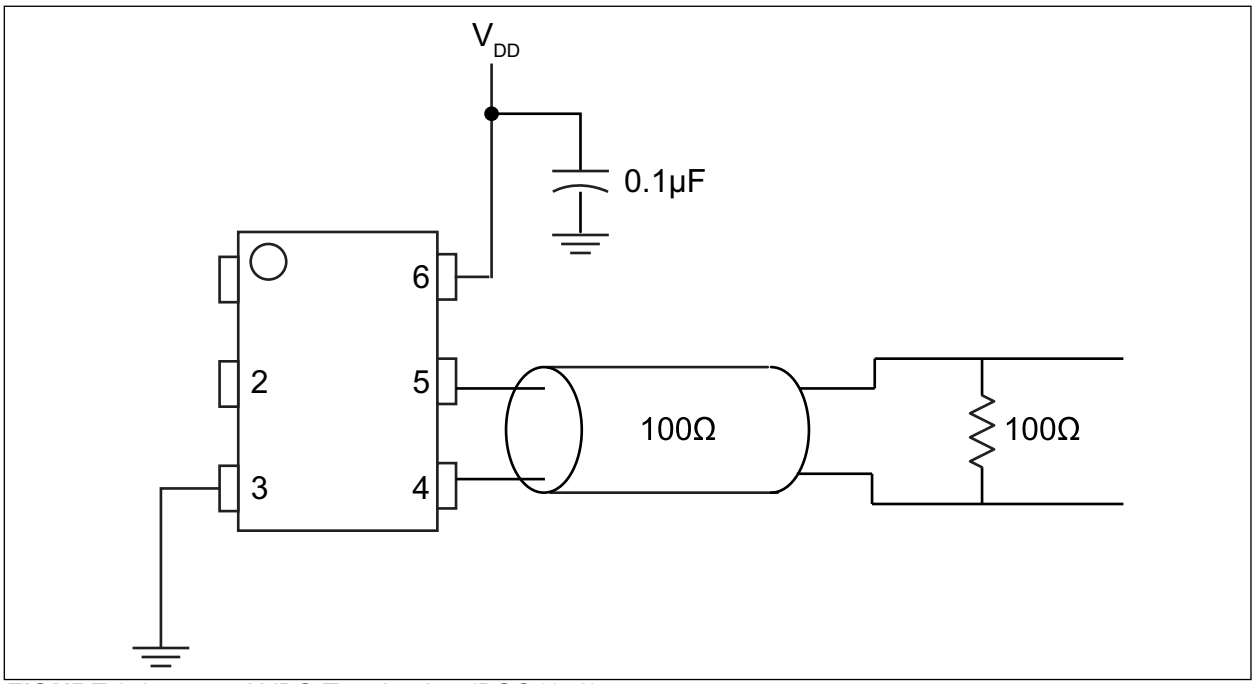



***FIGURE 3-2:*** *LVDS Termination (DSC12x3).*

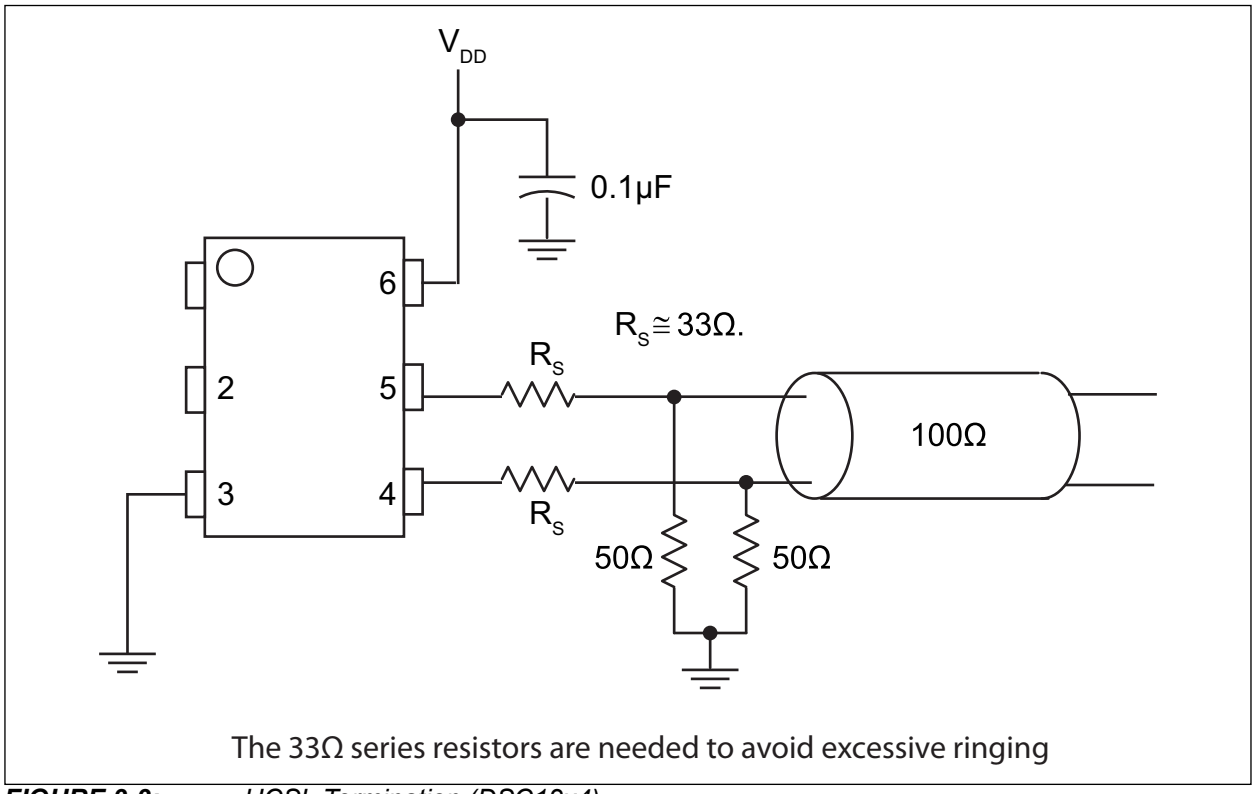



***FIGURE 3-3:*** *HCSL Termination (DSC12x4).*

## 4.0 OUTPUT WAVEFORM

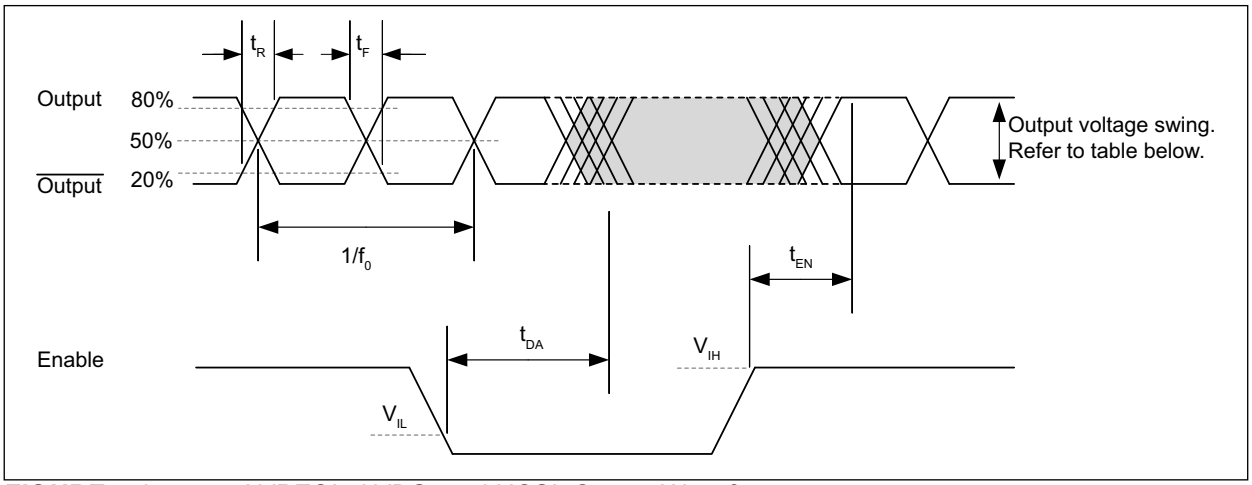



***FIGURE 4-1:*** *LVPECL, LVDS, and HCSL Output Waveform.*

**TABLE 4-1: OUTPUT VOLTAGE SWING BY LOGIC TYPE**

| Output Logic Protocol | Typical Peak-to-Peak Output Swing |
|---|---|
| LVPECL | 830 mV |
| LVDS | 350 mV |
| HCSL | 675 mV |

## 5.0 TEST CIRCUITS

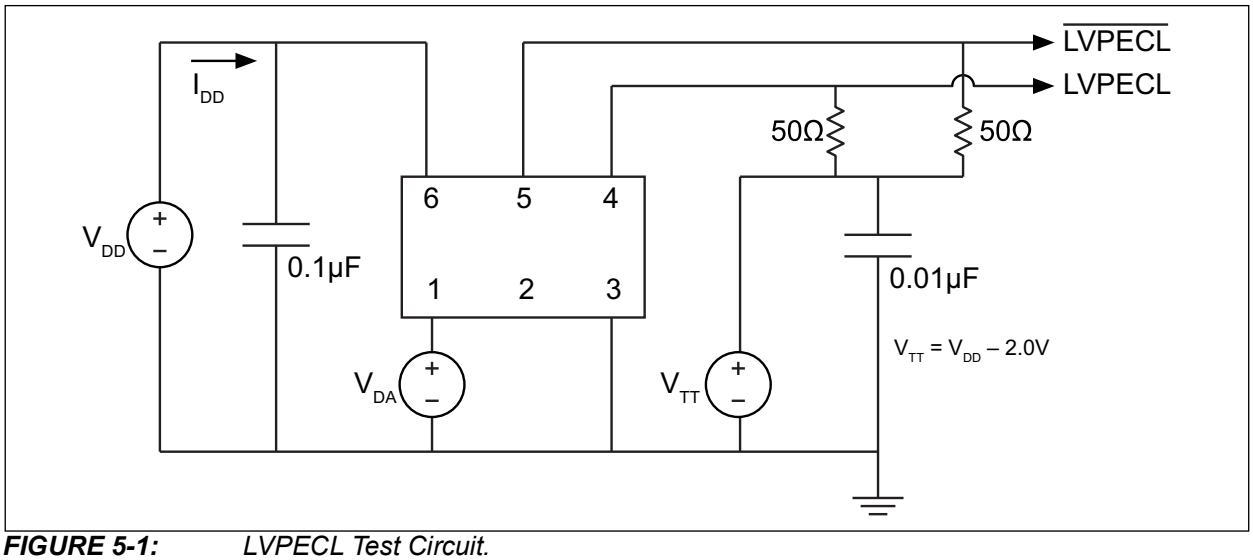



***FIGURE 5-1:*** *LVPECL Test Circuit.*

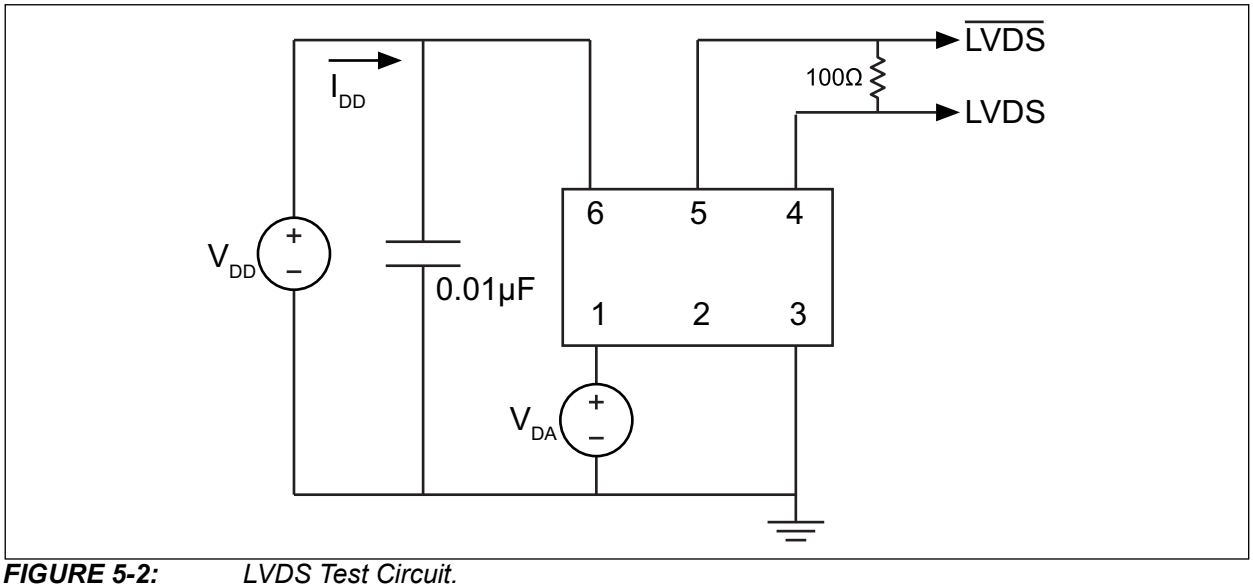



***FIGURE 5-2:*** *LVDS Test Circuit.*

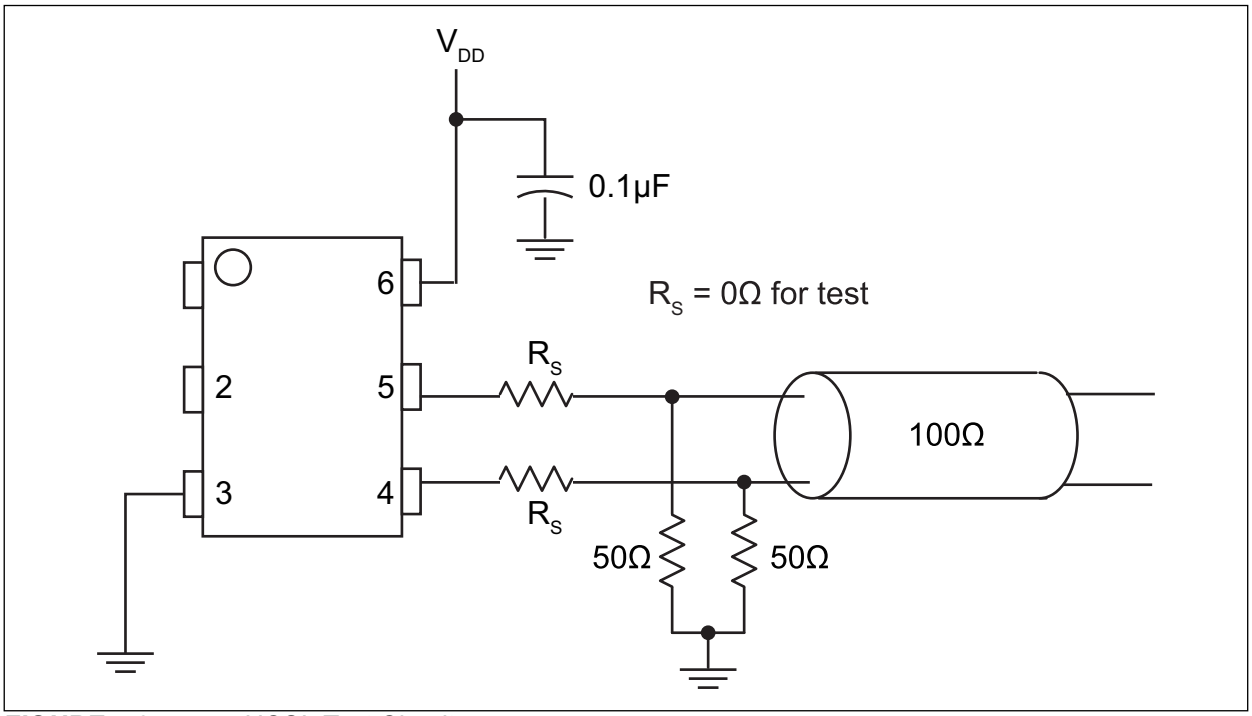



***FIGURE 5-3:*** *HCSL Test Circuit.*

## 6.0 SOLDER REFLOW PROFILE

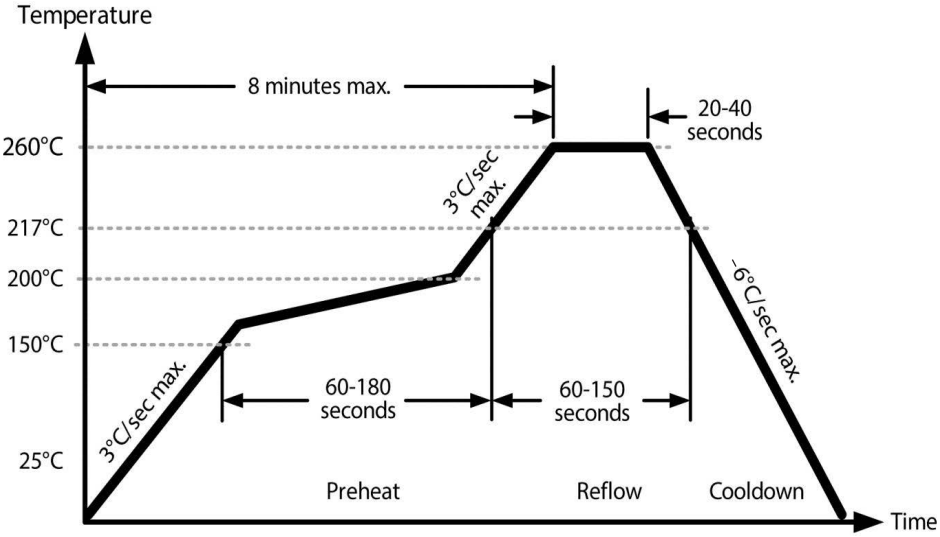



***FIGURE 6-1:*** *Solder Reflow Profile.*

**TABLE 6-1: SOLDER REFLOW**

| MSL 1 @ 260°C refer to JSTD-020C | |
|---|---|
| Ramp-Up Rate (200°C to Peak Temp) | 3°C/Sec. Max. |
| Preheat Time 150°C to 200°C | 60-180 Sec. |
| Time Maintained Above 217°C | 60-150 Sec. |
| Peak Temperature | 255°C to 260°C |
| Time within 5°C of Actual Peak | 20-40 Sec. |
| Ramp-Down Rate | 6°C/Sec. Max. |
| Time 25°C to Peak Temperature | 8 minute Max. |

## 7.0 BOARD LAYOUT (RECOMMENDED)

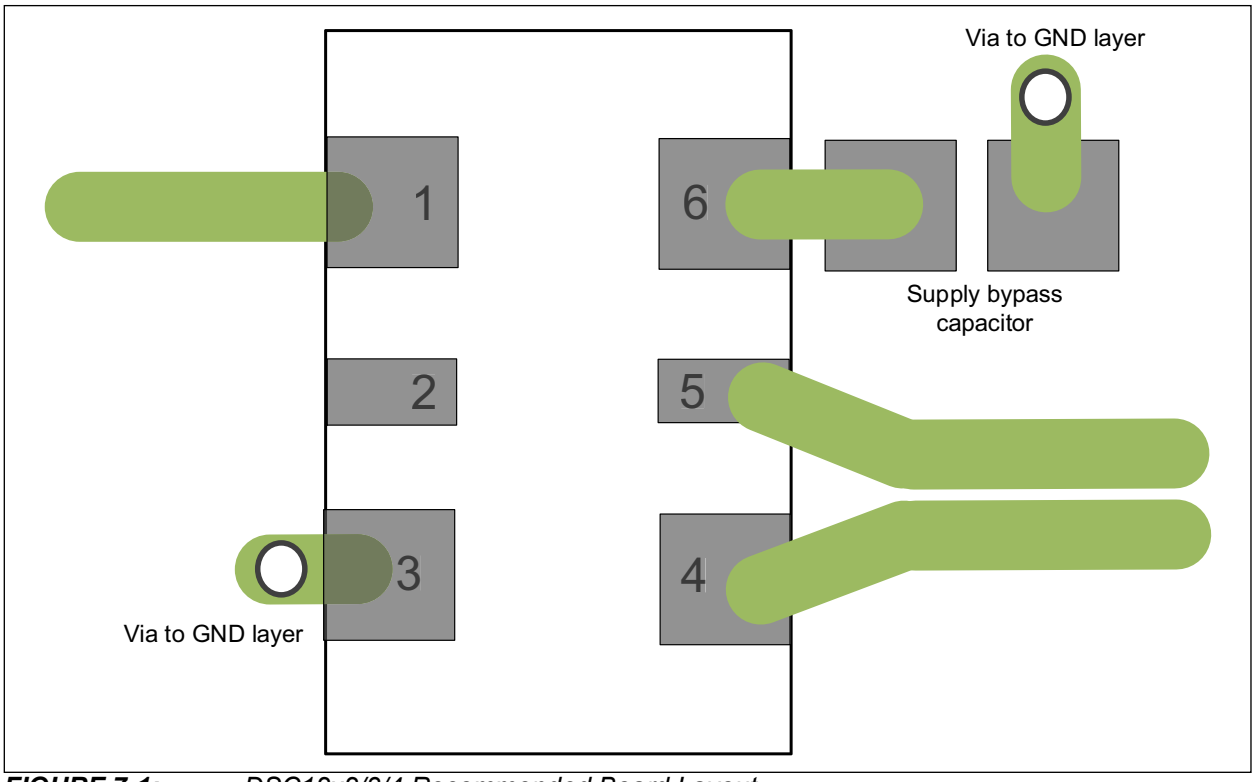



***FIGURE 7-1:*** *DSC12x2/3/4 Recommended Board Layout.*

## 8.0 PHASE NOISE

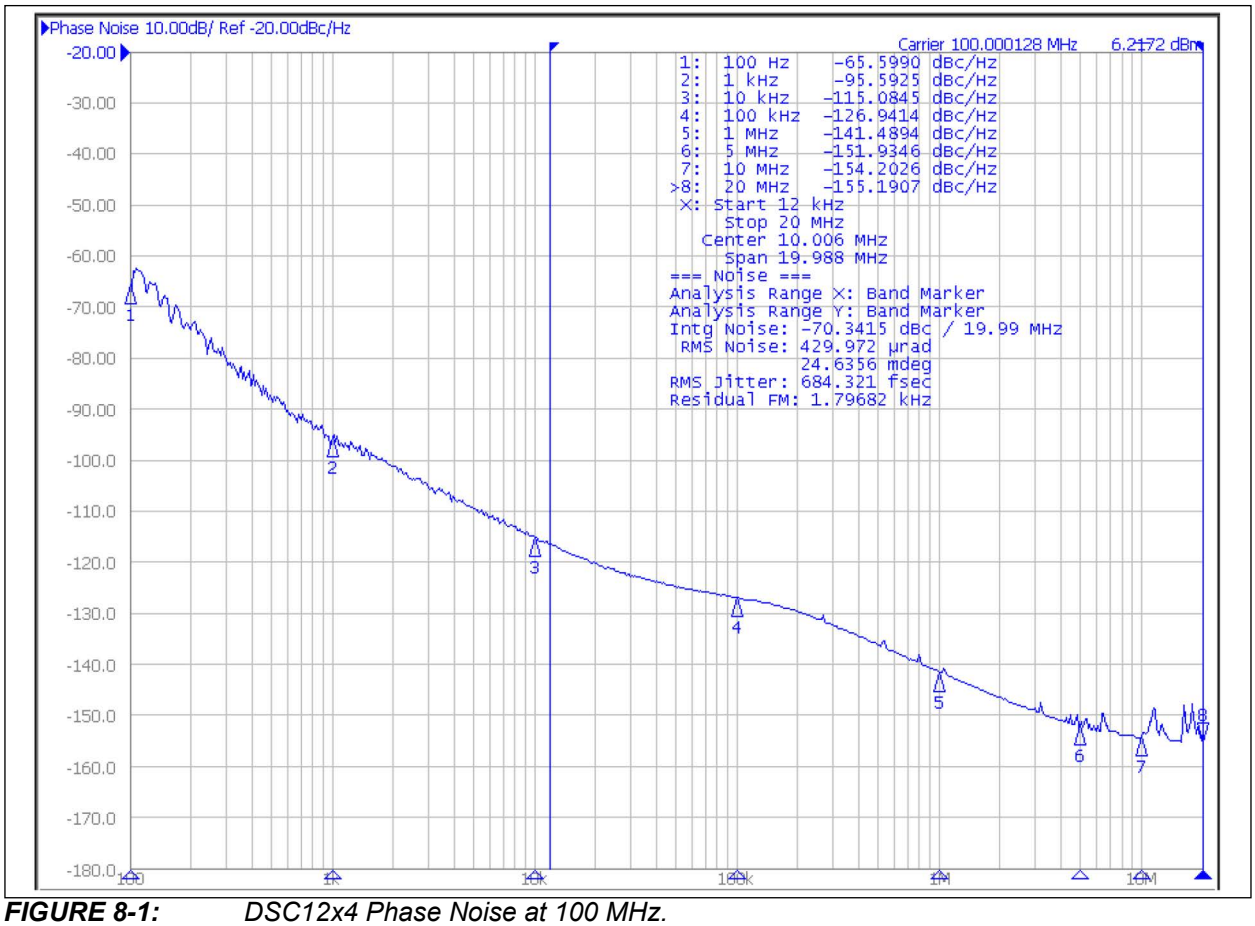



***FIGURE 8-1:*** *DSC12x4 Phase Noise at 100 MHz.*

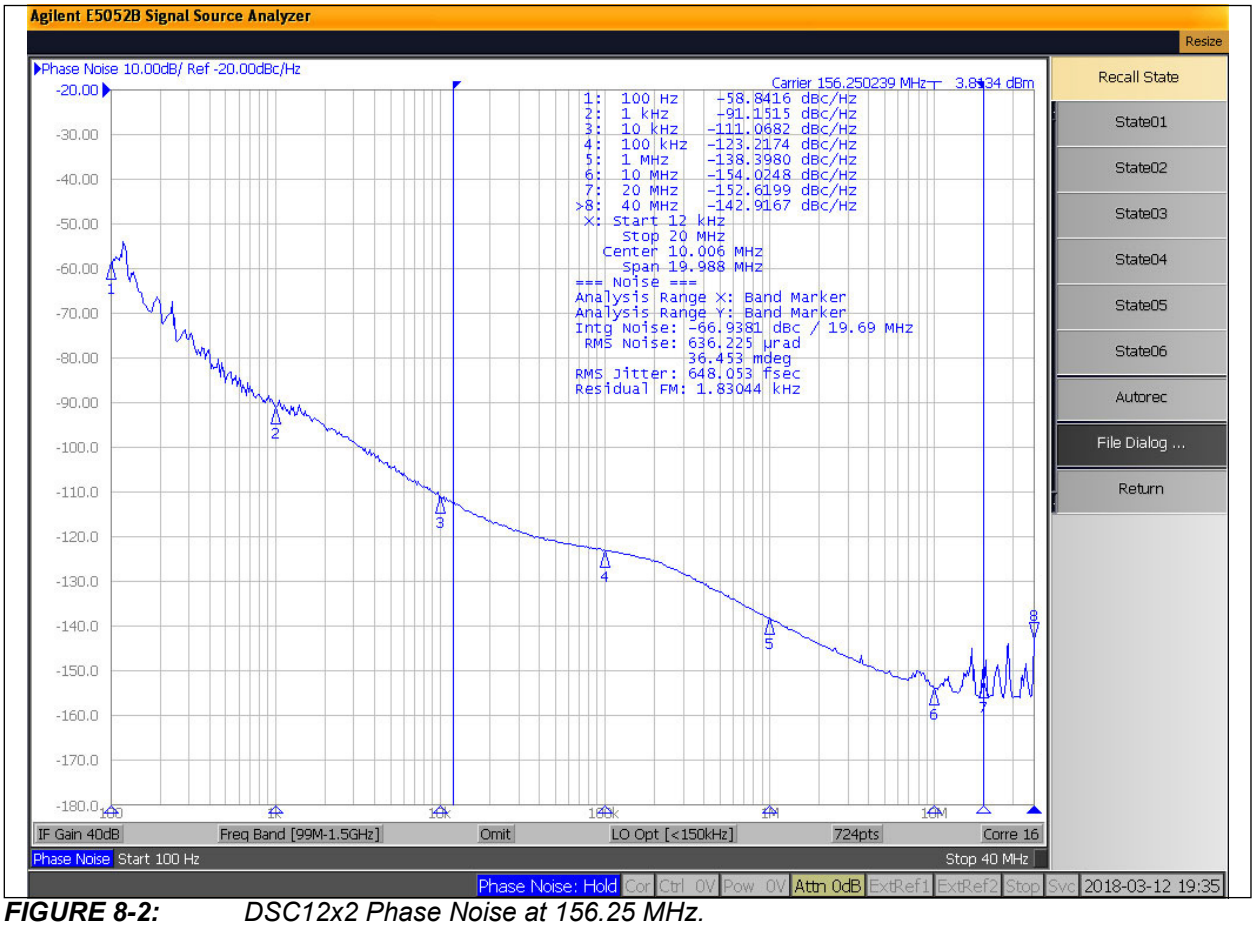
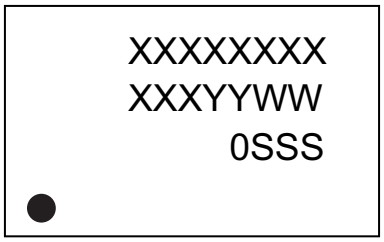



***FIGURE 8-2:*** *DSC12x2 Phase Noise at 156.25 MHz.*

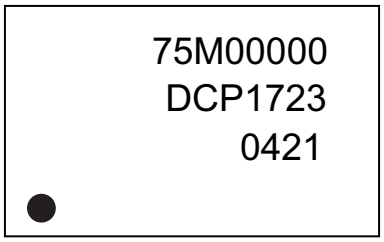
## 9.0 PACKAGING INFORMATION

### 9.1 Package Marking Information

6-Pin CDFN/VDFN*




Example




| | | |
|---|---|---|
| **Legend:** | XX...X | Product code, customer-specific information, or frequency in MHz without printed decimal point |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | SSS | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |
| | ●, ▲, ▼ | Pin one index is identified by a dot, delta up, or delta down (triangle |

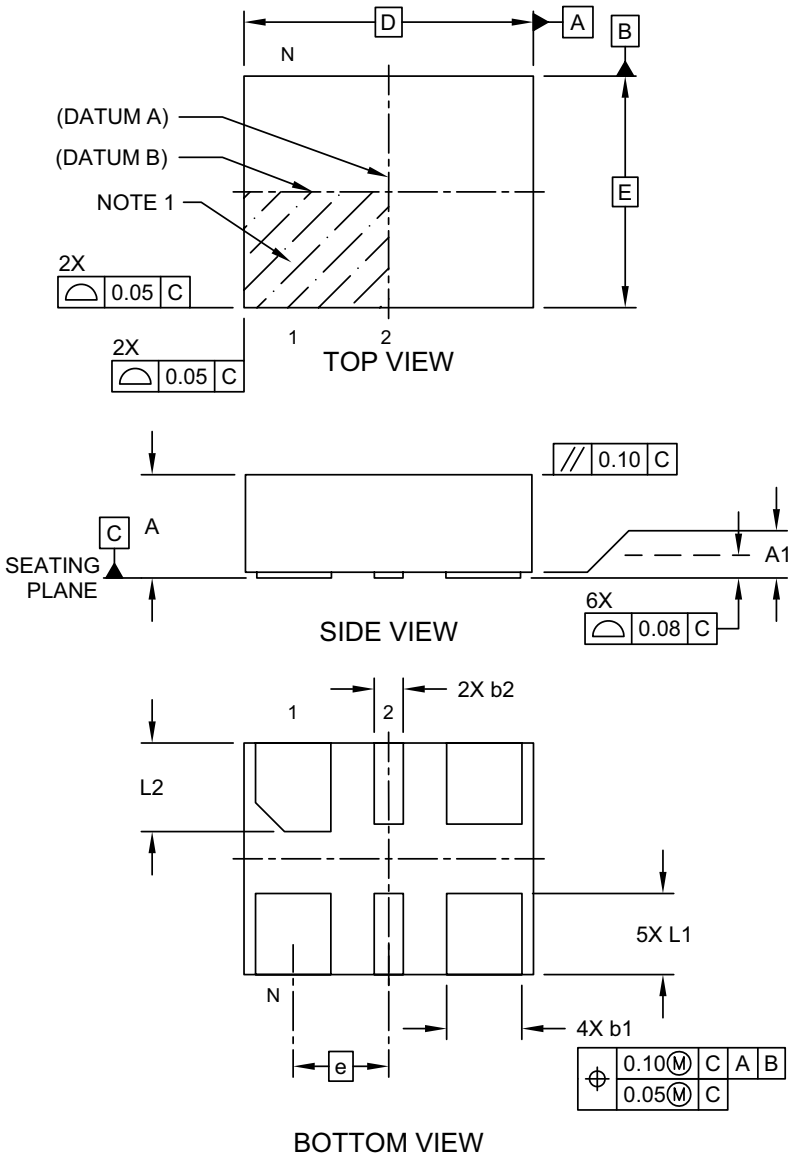
**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

## 6-Lead VDFN 2.5 mm x 2.0 mm Package Outline and Recommended Land Pattern

### 6-Lead Very Thin Dual Flatpack No-Leads (J7A) - 2.5x2.0 mm Body [VDFN]

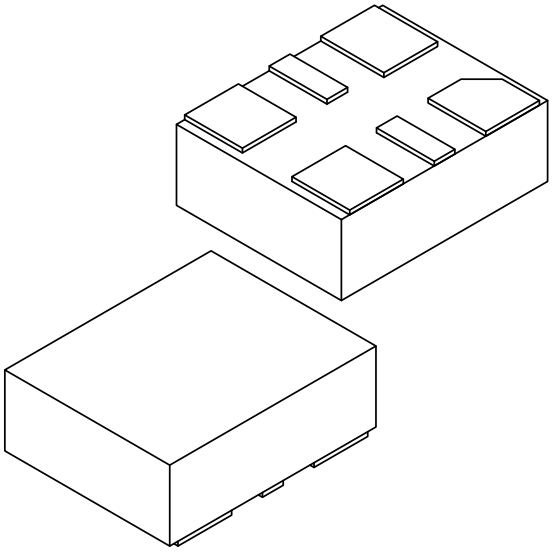
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-1005 Rev C Sheet 1 of 2

### 6-Lead Very Thin Dual Flatpack No-Leads (J7A) - 2.5x2.0 mm Body [VDFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 6 | |
| Pitch | e | | 0.825 BSC | |
| Overall Height | A | 0.80 | 0.85 | 0.90 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Overall Length | D | | 2.50 BSC | |
| Overall Width | E | | 2.00 BSC | |
| Terminal Width | b1 | 0.60 | 0.65 | 0.70 |
| Terminal Width | b2 | 0.20 | 0.25 | 0.30 |
| Terminal Length | L1 | 0.60 | 0.70 | 0.80 |
| Terminal Length | L2 | 0.665 | 0.765 | 0.865 |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

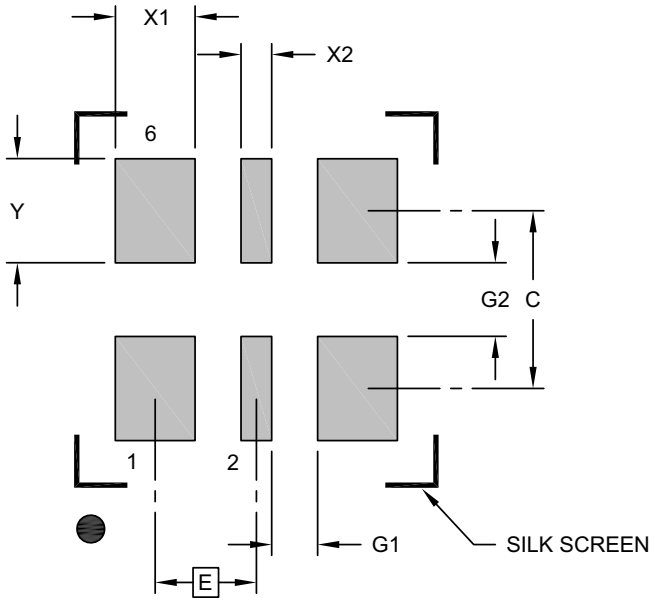
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1005 Rev C Sheet 2 of 2

**6-Lead Very Thin Dual Flatpack No-Leads (J7A) - 2.5x2.0 mm Body [VDFN]**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.825 BSC | |
| Contact Pad Width (X4) | X1 | | | 0.65 |
| Contact Pad Width (X2) | X2 | | | 0.25 |
| Contact Pad Length (X6) | Y | | | 0.85 |
| Contact Pad Spacing | C | | 1.45 | |
| Space Between Contacts (X4) | G1 | 0.38 | | |
| Space Between Contacts (X3) | G2 | 0.60 | | |

Notes:

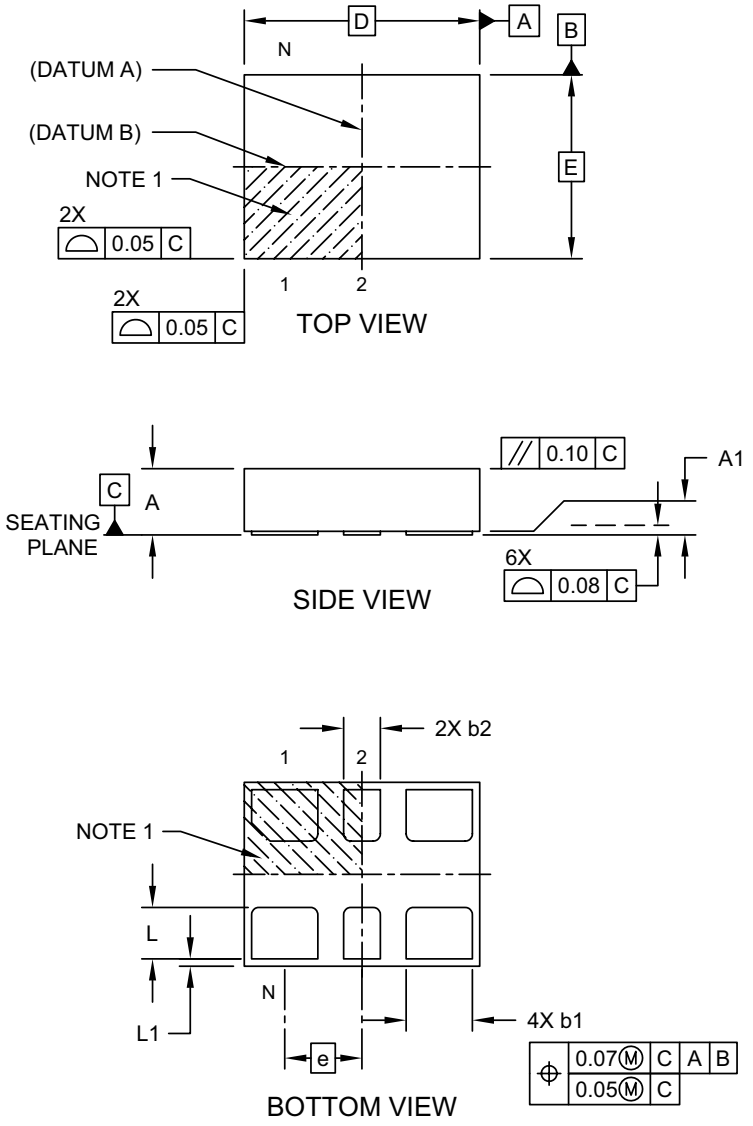
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3005 Rev C

## 6-Lead VDFN 3.2 mm x 2.5 mm Package Outline and Recommended Land Pattern

**6-Lead Very Thin Plastic Dual Flatpack No-Lead (H5A) - 3.2x2.5 mm Body [VDFN]**

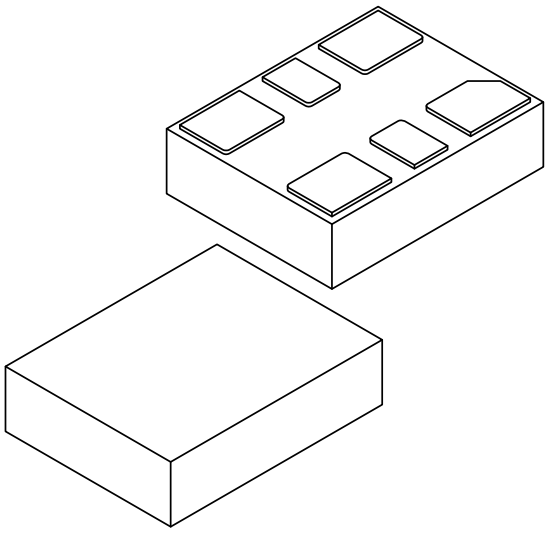
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-1007A Sheet 1 of 2

### 6-Lead Very Thin Plastic Dual Flatpack No-Lead (H5A) - 3.2x2.5 mm Body [VDFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 6 | |
| Pitch | e | | 1.05 BSC | |
| Overall Height | A | 0.80 | 0.85 | 0.90 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Overall Length | D | | 3.20 BSC | |
| Overall Width | E | | 2.50 BSC | |
| Terminal Width | b1 | 0.85 | 0.90 | 0.95 |
| Terminal Width | b2 | 0.45 | 0.50 | 0.55 |
| Terminal Length | L | 0.65 | 0.70 | 0.75 |
| Terminal Pullback | L1 | | 0.10 REF | |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

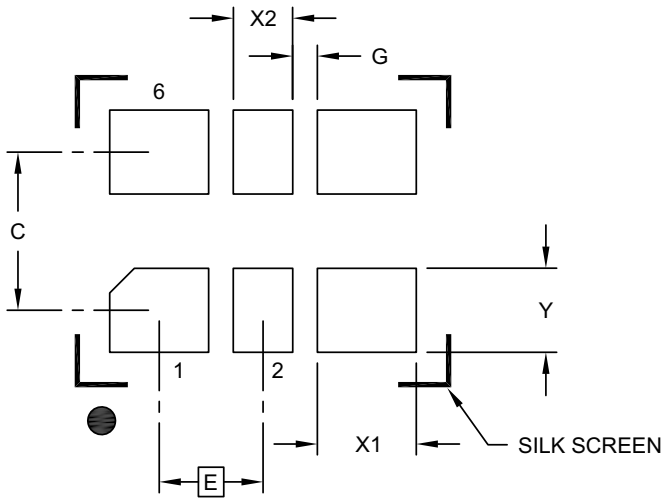
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1007A Sheet 2 of 2

**6-Lead Very Thin Plastic Dual Flatpack No-Lead (H5A) - 3.2x2.5 mm Body [VDFN]**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.05 BSC | |
| Contact Pad Spacing | C | | 1.60 | |
| Contact Pad Width (X4) | X1 | | | 1.00 |
| Contact Pad Width (X2) | X2 | | | 0.60 |
| Contact Pad Length (X6) | Y | | | 0.85 |
| Space Between Contacts (X4) | G1 | 0.25 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

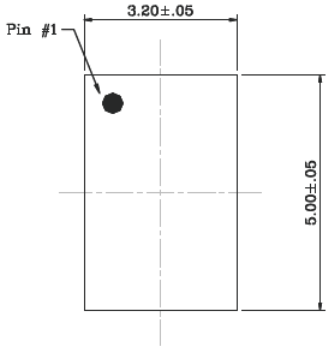
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3007A

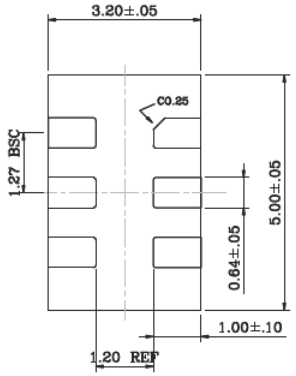
## 6-Lead CDFN 5.0 mm x 3.2 mm Package Outline and Recommended Land Pattern

**TITLE**
6 LEAD CDFN 5.0x3.2mm COL PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

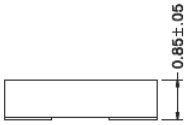
| DRAWING # | CDFN5032-6LD-PL-1 | UNIT | MM |
|---|---|---|---|



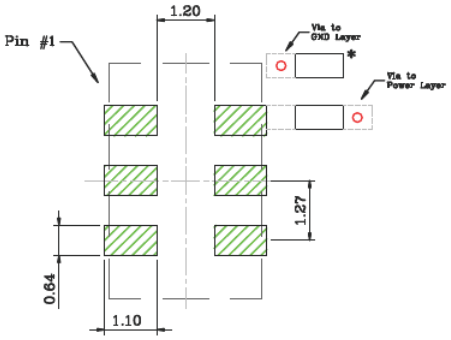

Top View




Bottom View




Side View




Recommended Land Pattern

NOTE:

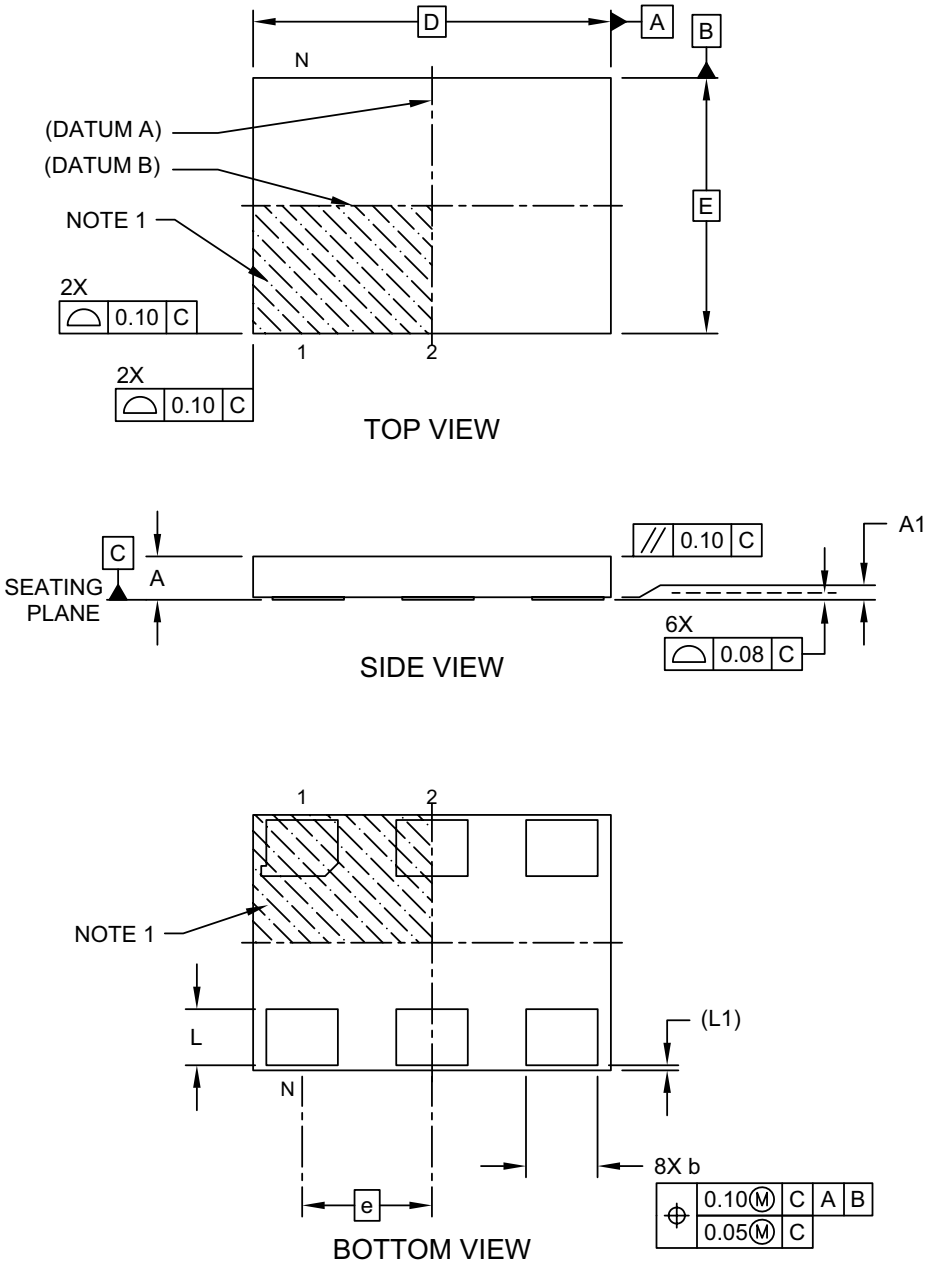
1. * Power Supply Decoupling Capacitor is required in Recommended Land Pattern.
2. Green shaded rectangles in Recommended Land Pattern are solder stencil opening.
3. Red circles in Recommended Land Pattern are thermal VIA.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

## 6-Lead VDFN 7.0 mm x 5.0 mm Package Outline and Recommended Land Pattern

### 6-Lead Very Thin Dual Flatpack, No Lead Package (HPA) - 7x5 mm Body [VDFN]

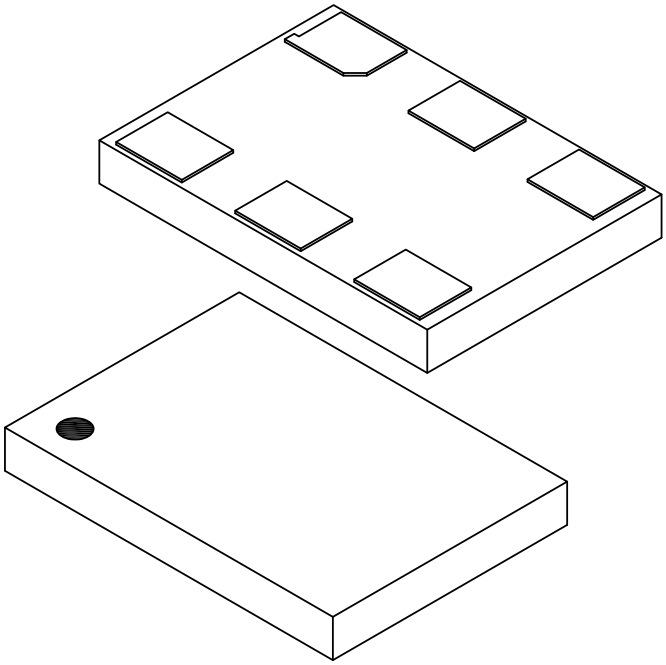
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-1227 Rev A Sheet 1 of 2

### 6-Lead Very Thin Dual Flatpack, No Lead Package (HPA) - 7x5 mm Body [VDFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 6 | |
| Pitch | e | | 2.54 BSC | |
| Overall Height | A | 0.80 | 0.85 | 0.90 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Overall Length | D | | 7.00 BSC | |
| Overall Width | E | | 5.00 BSC | |
| Terminal Width | b | 1.30 | 1.40 | 1.50 |
| Terminal Length | L | 1.00 | 1.10 | 1.20 |
| Pullback | L1 | | 0.10 REF | |

Notes:

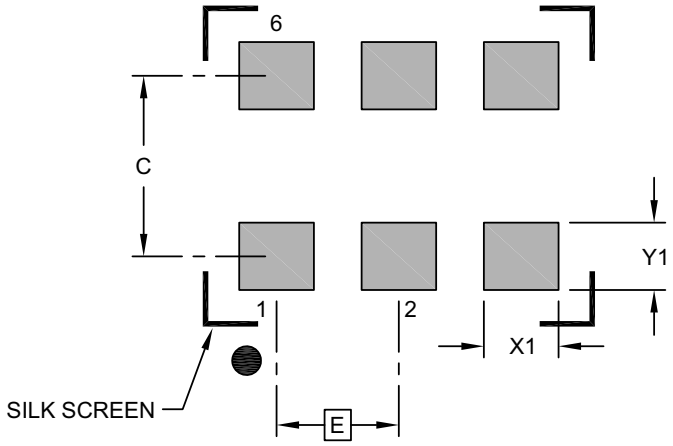
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1227 Rev A Sheet 2 of 2

**6-Lead Very Thin Dual Flatpack, No Lead Package (HPA) - 7x5 mm Body [VDFN]**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 2.54 BSC | |
| Contact Pad Spacing | C | | 3.90 | |
| Contact Pad Width (X6) | X1 | | | 1.55 |
| Contact Pad Length (X6) | Y1 | | | 1.40 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3227 Rev A

**NOTES:**

# APPENDIX A: REVISION HISTORY

## Revision A (April 2019)

- Initial release of DSC12x2/3/4 as Microchip data sheet DS20006011A.

## Revision B (June 2020)

- Revisions to the data sheet made in the Electrical Characteristics table under HCSL: Added new rows for Integrated Phase Noise and Phase Jitter.
- Also added a new bullet under the Features section.

## Revision C (January 2021)

- Updated Phase Jitter maximum values for $J_{RMS-CC}$ in the Electrical Characteristics table and added a sixth note.
- Updated package drawing for 6-Lead VDFN 2.5 mm x 2.0 mm Package Outline and Recommended Land Pattern.
- Updated Figure 3-1.

## Revision D (March 2021)

- Removed Note 6 from the Electrical Characteristics table.

## Revision E (March 2022)

- Added PCI Express Gen 5 to the Applications list.

## Revision F (May 2023)

- Added PCI Express Gen 6 to the Applications list and the.Features list.
- Corrected the maximum value for Peak-to-Peak Output Swing in the LVDS (DSC12x3) section of the Electrical Characteristics table.
- Added PCIe Gen 6 Phase Jitter values to the LVDS (DSC12x3) and HCSL (DSC12x4) sections of the Electrical Characteristics table.

**NOTES:**

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| PART NO. | X | X | X | X | X | -XXXXXXXX | X |
|---|---|---|---|---|---|---|---|
| Device | Control Pin | Output Format | Package | Temperature | Freq. Stability | Output Frequency | Media Type |

| | | | |
|---|---|---|---|
| **Device:** | DSC12: | | High Performance Differential MEMS Oscillators |
| **Control Pin:** | 0 | = | Pin 1 $\overline{\text{STDBY}}$ with Pull-up |
| | 1 | = | Pin 1 Frequency Select with Pull-up |
| | 2 | = | Pin 1 OE with Pull-up |
| | 3 | = | Pin 2 $\overline{\text{STDBY}}$ with Pull-up |
| | 4 | = | Pin 2 Frequency Select with Pull-up |
| | 5 | = | Pin 2 OE with Pull-up |
| **Output Format:** | 2 | = | LVPECL |
| | 3 | = | LVDS |
| | 4 | = | HCSL |
| **Package:** | N | = | 7 mm x 5 mm 6-Lead VDFN |
| | B | = | 5 mm x 3.2 mm 6-Lead CDFN |
| | C | = | 3.2 mm x 2.5 mm 6-Lead VDFN |
| | D | = | 2.5 mm x 2 mm 6-Lead VDFN |
| **Temperature:** | A | = | –40°C to +125°C(Available on certain options) |
| | L | = | –40°C to +105°C |
| | I | = | –40°C to +85°C |
| | E | = | –20°C to +70°C |
| **Frequency Stability:** | 1 | = | ±50 ppm |
| | 2 | = | ±25 ppm |
| | 3 | = | ±20 ppm |
| **Output Frequency:** | xMxxxxxx= | | <10 MHz |
| | xxMxxxxx= | | <100 MHz |
| | xxxMxxxx= | | >100 MHz |
| | CCCCC= | | with Frequency Select |
| | PROG | = | TimeFlash |
| **Media Type:** | <blank>= | | Bulk |
| | T | = | 1,000/Reel |
| | B | = | 3,000/Reel |

Please visit the Microchip ClockWorks Configurator® website to configure the part number for customized frequency select settings.

http://clockworks.microchip.com/timing

**Examples:**

a) DSC1202NE1-25M00000T: Pin 1 $\overline{\text{STDBY}}$ with Pull-up, LVPECL Output, 7x5 VDFN, –20°C to +70°C, ±50 ppm, 25 MHz Output Frequency, 1,000/Reel

b) DSC1243CL3-C0013: Pin 2 Frequency Select with Pull-up, LVDS Output, 3.2x2.5 VDFN, –40°C to +105°C, ±20 ppm, Multiple Output Frequency, Bulk

c) DSC1224BI2-19M50000B: Pin 1 OE with Pull-up, HCSL Output, 5x3.2 CDFN, –40°C to +85°C, ±25 ppm, 19.5 MHz Output Frequency, 3,000/Reel

d) DSC1232DL3-55M82000T: Pin 2 $\overline{\text{STDBY}}$ with Pull-up, LVPECL Output, 2.5x2 VDFN, –40°C to +105°C, ±20 ppm, 55.82 MHz Output Frequency, 1,000/Reel

e) DSC1213NI1-C0014B: Pin 1 Frequency Select with Pull-up, LVDS Output, 7x5 VDFN, –40°C to +85°C, ±50 ppm, Multiple Output Frequency, 3,000/Reel

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

**NOTES:**

**Note the following details of the code protection feature on Microchip products:**

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable" Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.



*For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.*

**Trademarks**



ISBN: 978-1-6683-2579-7

# Worldwide Sales and Service

## AMERICAS

**Corporate Office**
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

**Atlanta**
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

**Austin, TX**
Tel: 512-257-3370

**Boston**
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

**Chicago**
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

**Dallas**
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

**Detroit**
Novi, MI
Tel: 248-848-4000

**Houston, TX**
Tel: 281-894-5983

**Indianapolis**
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

**Los Angeles**
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

**Raleigh, NC**
Tel: 919-844-7510

**New York, NY**
Tel: 631-435-6000

**San Jose, CA**
Tel: 408-735-9110
Tel: 408-436-4270

**Canada - Toronto**
Tel: 905-695-1980
Fax: 905-695-2078

## ASIA/PACIFIC

**Australia - Sydney**
Tel: 61-2-9868-6733

**China - Beijing**
Tel: 86-10-8569-7000

**China - Chengdu**
Tel: 86-28-8665-5511

**China - Chongqing**
Tel: 86-23-8980-9588

**China - Dongguan**
Tel: 86-769-8702-9880

**China - Guangzhou**
Tel: 86-20-8755-8029

**China - Hangzhou**
Tel: 86-571-8792-8115

**China - Hong Kong SAR**
Tel: 852-2943-5100

**China - Nanjing**
Tel: 86-25-8473-2460

**China - Qingdao**
Tel: 86-532-8502-7355

**China - Shanghai**
Tel: 86-21-3326-8000

**China - Shenyang**
Tel: 86-24-2334-2829

**China - Shenzhen**
Tel: 86-755-8864-2200

**China - Suzhou**
Tel: 86-186-6233-1526

**China - Wuhan**
Tel: 86-27-5980-5300

**China - Xian**
Tel: 86-29-8833-7252

**China - Xiamen**
Tel: 86-592-2388138

**China - Zhuhai**
Tel: 86-756-3210040

## ASIA/PACIFIC

**India - Bangalore**
Tel: 91-80-3090-4444

**India - New Delhi**
Tel: 91-11-4160-8631

**India - Pune**
Tel: 91-20-4121-0141

**Japan - Osaka**
Tel: 81-6-6152-7160

**Japan - Tokyo**
Tel: 81-3-6880- 3770

**Korea - Daegu**
Tel: 82-53-744-4301

**Korea - Seoul**
Tel: 82-2-554-7200

**Malaysia - Kuala Lumpur**
Tel: 60-3-7651-7906

**Malaysia - Penang**
Tel: 60-4-227-8870

**Philippines - Manila**
Tel: 63-2-634-9065

**Singapore**
Tel: 65-6334-8870

**Taiwan - Hsin Chu**
Tel: 886-3-577-8366

**Taiwan - Kaohsiung**
Tel: 886-7-213-7830

**Taiwan - Taipei**
Tel: 886-2-2508-8600

**Thailand - Bangkok**
Tel: 66-2-694-1351

**Vietnam - Ho Chi Minh**
Tel: 84-28-5448-2100

## EUROPE

**Austria - Wels**
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

**Denmark - Copenhagen**
Tel: 45-4485-5910
Fax: 45-4485-2829

**Finland - Espoo**
Tel: 358-9-4520-820

**France - Paris**
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

**Germany - Garching**
Tel: 49-8931-9700

**Germany - Haan**
Tel: 49-2129-3766400

**Germany - Heilbronn**
Tel: 49-7131-72400

**Germany - Karlsruhe**
Tel: 49-721-625370

**Germany - Munich**
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

**Germany - Rosenheim**
Tel: 49-8031-354-560

**Israel - Ra'anana**
Tel: 972-9-744-7705

**Italy - Milan**
Tel: 39-0331-742611
Fax: 39-0331-466781

**Italy - Padova**
Tel: 39-049-7625286

**Netherlands - Drunen**
Tel: 31-416-690399
Fax: 31-416-690340

**Norway - Trondheim**
Tel: 47-7288-4388

**Poland - Warsaw**
Tel: 48-22-3325737

**Romania - Bucharest**
Tel: 40-21-407-87-50

**Spain - Madrid**
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

**Sweden - Gothenberg**
Tel: 46-31-704-60-40

**Sweden - Stockholm**
Tel: 46-8-5090-4654

**UK - Wokingham**
Tel: 44-118-921-5800
Fax: 44-118-921-5820