

GreenBridge™ 2 Series of High-Efficiency Bridge Rectifiers



ON Semiconductor®

www.onsemi.com

FDMQ8205A

General Description

FDMQ8205A is GreenBridge 2 series of quad MOSFETs for a bridge application so that the input will be insensitive to the polarity of a power source coupled to the device. Many known bridge rectifier circuits can be configured using typical diodes. The conventional diode bridge has relatively high power loss that is undesirable in many applications. Especially, Power over Ethernet (PoE) Power Device (PD) application requires high-efficiency bridges because it should be operated with the limited power delivered from Power Source Equipment (PSE) which is classified by IEEE802.3at. FDMQ8205A is configured with low $r_{DS(on)}$ dual P-ch MOSFETs and N-ch MOSFETs so that it can reduce the power loss caused by the voltage drop, compared to the conventional diode bridge. FDMQ8205A enables the application to maximize the available power and voltage and to eliminate the thermal design problems in PoE PD applications.

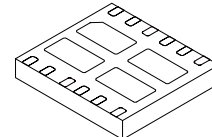
FDMQ8205A GreenBridge 2 is compatible with IEEE802.3at PoE standard by not compromising detection and classification requirement as well as small backfeed voltage.

Features

- Low Power Loss GreenBridge Replaces Diode Bridge
- Self Driving Circuitry for MOSFETs
- Low $r_{DS(on)}$ 100 V Rated MOSFETs
- Maximizing Available Power and Voltage
- Eliminating Thermal Design Problems
- IEEE802.3af/at and 3bt Compatible
 - ◆ Meet Detection and Classification Requirement
 - ◆ Work with 2 and 4-pair Architecture
 - ◆ Small Backfeed Voltage
- Compact MLP 4.5x5 Package
- This is a Pb-Free Device

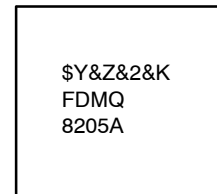
Applications

- Power over Ethernet (PoE) Power Device (PD)
- IP Phones
- Network Cameras
- Wireless Access Points
- Thin Clients
- Microcell
- Femtocell



WDFN12 5x4.5, 0.8P
CASE 511CS

MARKING DIAGRAM



FDMQ8205A = Specific Device Code
\$Y = ON Semiconductor Logo
&Z = Assembly Plant Code
&2 = 2-Digit Data Code
&K = 2-Digits Lot Run Traceability Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

FDMQ8205A

TYPICAL APPLICATION

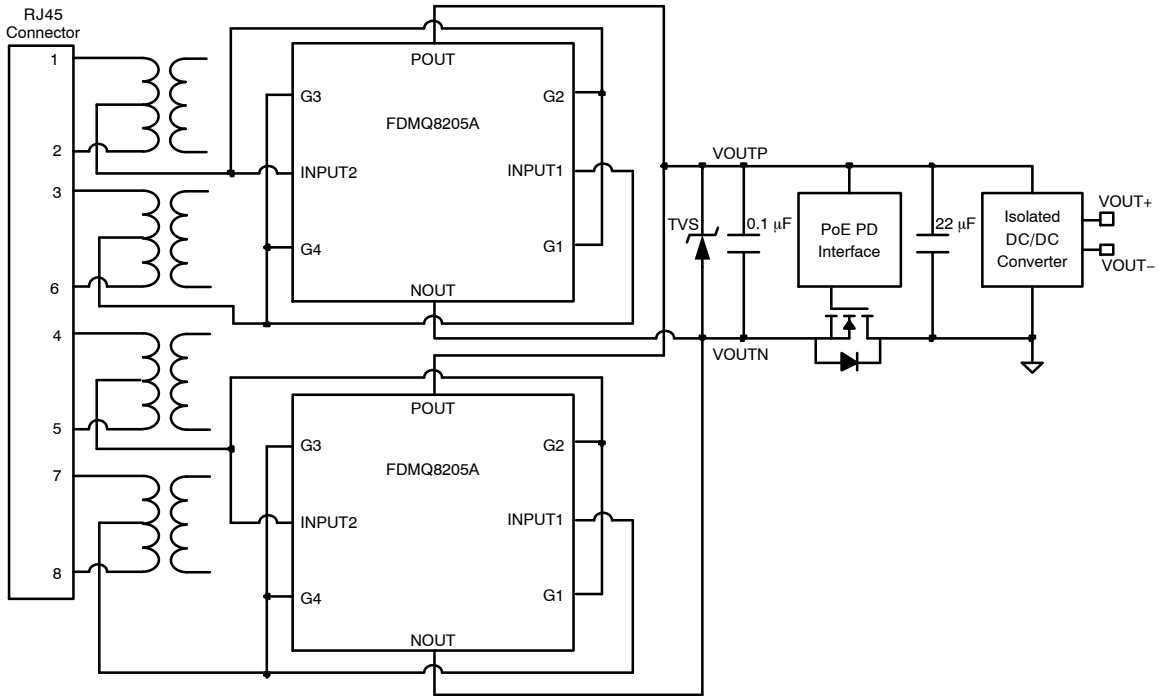


Figure 1. Typical Application of Power Device for 2-Pair Architecture of IEEE802.3af/at Power over Ethernet Standard

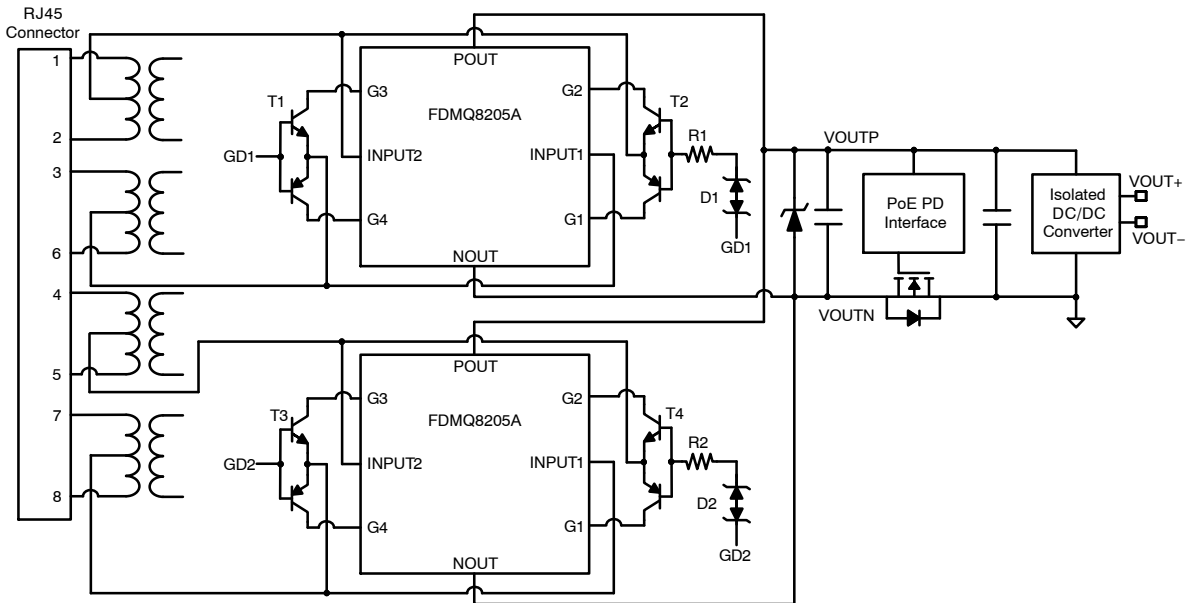


Figure 2. Typical Application of Power Device for IEEE802.3bt Power over Ethernet Standard

TYPICAL BOM OF GATE DRIVING CIRCUITS

Reference	Description	Part Name
T1, T2, T3, T4	NPN & PNP Transistors	BC846BPDW1T1
D1, D2	Dual Common Anode Zeners	MMBZ27VALT1G
R1, R2	162 kΩ Resistor	RC0603FR-07162KL

FDMQ8205A

BLOCK DIAGRAM

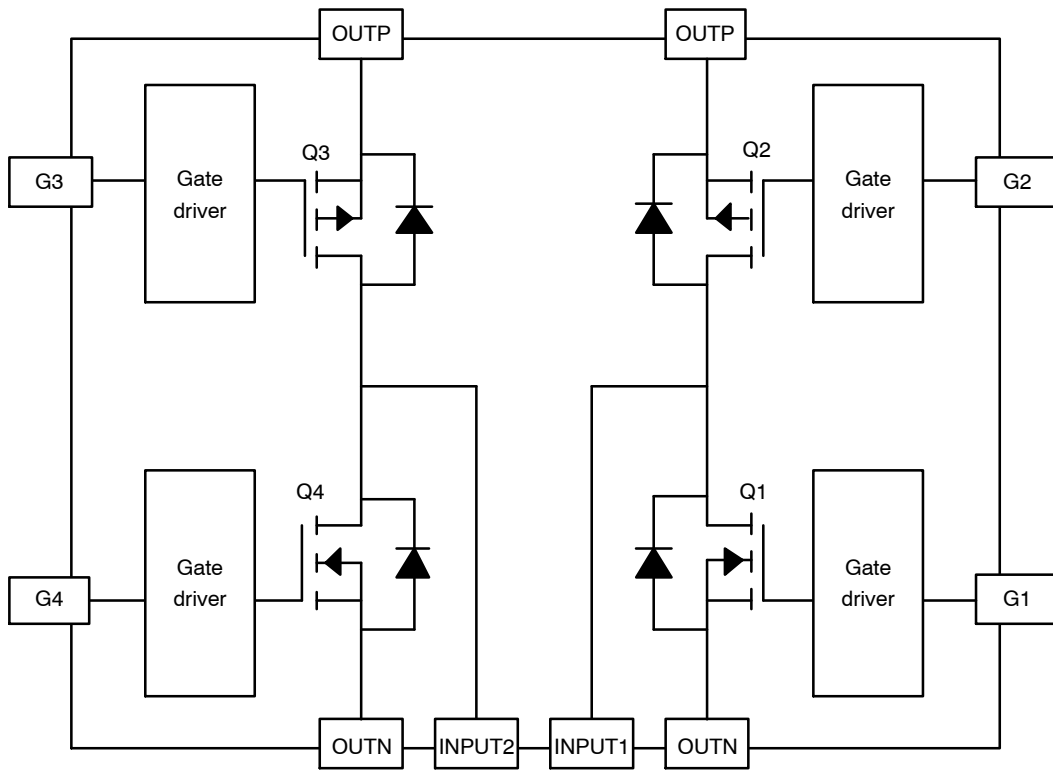


Figure 3. Block Diagram

FDMQ8205A

PIN CONFIGURATION

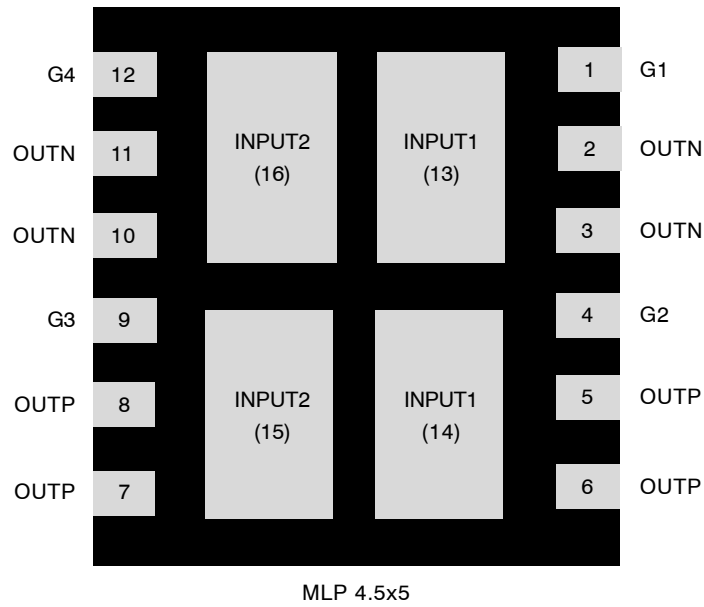


Figure 4. Pin Assignment (Bottom View)

PIN DESCRIPTION

Pin No.	Name	Description
1	G1	Gate of Q1 N-ch MOSFET
4	G2	Gate of Q2 P-ch MOSFET
9	G3	Gate of Q3 P-ch MOSFET
12	G4	Gate of Q4 N-ch MOSFET
13, 14	INPUT1	Input1 of GreenBridge
15, 16	INPUT2	Input2 of GreenBridge
2, 3, 11, 10	OUTN	Negative Output of GreenBridge
5, 6, 7, 8	OUTP	Positive Output of GreenBridge

1. Show the feature that provides orientation or pin 1 location.

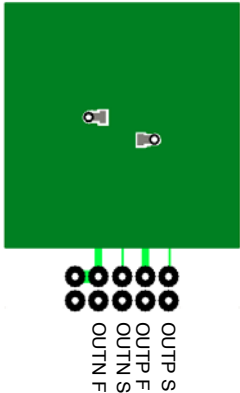
FDMQ8205A

ABSOLUTE MAXIMUM RATINGS

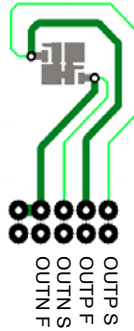
		Min	Max	Unit
INPUT1, INPUT2 to OUTN		-	100	V
OUTP to INPUT1, INPUT2		-	100	V
INPUT1 to INPUT2		-	100	V
INPUT2 to INPUT1		-	100	V
OUTP to OUTN		-	100	V
G1, G2, G3, G4 to OUTN		-	70	V
OUTP to G1, G2, G3, G4		-	70	V
VG_TRANSIENT	Transient Gate Voltage, Pulse Width < 200 μ s, Duty Cycle < 0.003%	-	100	V
Continuous I_{INPUT} (GreenBridge Current, Q1 + Q3 or Q2 + Q4)	$T_A = 25^\circ\text{C}$ (Note 2a)	-	3.0	A
	$T_A = 25^\circ\text{C}$ (Note 2b)	-	1.7	A
Pulsed I_{INPUT} (Q1 + Q3 or Q2 + Q4)	Pulse Width < 300 μ s, Duty Cycle < 2% (Note 3)	-	58	A
P_D (Power Dissipation, Q1 + Q3 or Q2 + Q4)	$T_A = 25^\circ\text{C}$ (Note 2a)	-	2.5	W
	$T_A = 25^\circ\text{C}$ (Note 2b)	-	0.78	W
Max Junction Temperature		-	150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 50 $^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper, the board designed Q1 + Q3 or Q2 + Q4.



b. 160 $^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper, the board designed Q1 + Q3 or Q2 + Q4.

3. Pulse Id measured at $t_d \leq 300 \mu\text{s}$, refer to SOA graph for more details.

THERMAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	-	5.1	-	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 2a)	-	50	-	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 2b)	-	160	-	

FDMQ8205A

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{INPUT}	Input Voltage of Bridge	INPUT1 to INPUT2 or INPUT2 to INPUT1	-	57	V
V_G	Gate Voltage of MOSFETs	G1, G4 to OUTN G2, G3 to OUTP	-	57	V
I_{INPUT}	Input Current of Bridge	Bridge Current through Q2 and Q4 or (Q3 and Q1)	-	1.7	A
Ambient Operation Temperature (T_A)			-40	85	°C
Junction Operating Temperature (T_J) (Note 4)			-40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

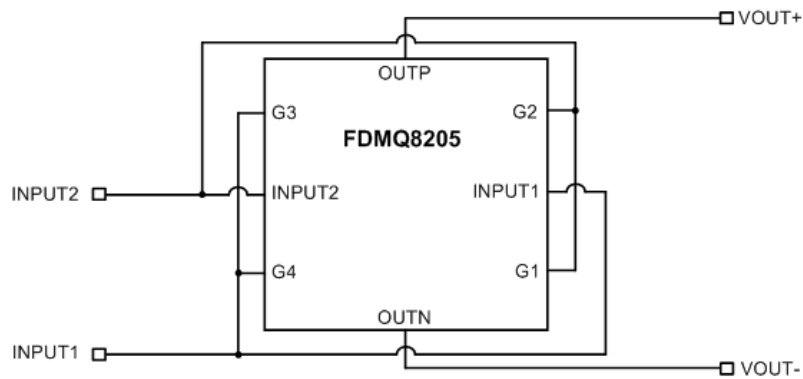
4. Backfeed Voltage can not be guaranteed for junction temperature in excess of 85°C. See V_{BF} in Electrical Characteristics Table.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{INPUT}	Input Voltage of Bridge	At INPUT1 to INPUT2 or INPUT2 to INPUT1	-	-	57	V
V_G	Gate Voltage of MOSFETs	At G1, G4 to OUTN and G2, G3 to OUTP	-	-	57	V
I_Q	Quiescent Current	Detection Mode $1.5\text{ V} < V_{INPUT} = V_G < 10.1\text{ V}$ (Note 5)	-	-	5	μA
		Classification Mode $10.2\text{ V} < V_{INPUT} = V_G < 23.9\text{ V}$ (Note 5)	-	-	400	μA
		Power On Mode Maximum $V_{INPUT} = V_G = 57\text{ V}$ (Note 5)	-	-	3.2	mA
V_{TURN_ON}	Turn-On Voltage of MOSFETs	Turn-On of MOSFETs while V_G Increases (Note 4)	32	-	36	V
$I_{LEAKAGE}$	Turn-Off Leakage Current	$V_{OUTP} = 57\text{ V}$, $V_{OUTN} = 0\text{ V}$ $T_J = -40^\circ\text{C}$ to 85°C (Note 5)	-	-	700	μA
V_{BF}	Backfeed Voltage	$V_{OUTP} = 57\text{ V}$, $V_{OUTN} = 0\text{ V}$, 100 k Ω between INPUT1 and INPUT2 $T_J = -40^\circ\text{C}$ to 85°C (Note 5)	-	-	2.7	V
$r_{DS(on)}$	N-ch MOSFET	$V_G = 42\text{ V}$, $I_{INPUT} = 1.5\text{ A}$, $T_A = 25^\circ\text{C}$	-	35	51	m Ω
		$V_G = 48\text{ V}$, $I_{INPUT} = 1.5\text{ A}$, $T_A = 25^\circ\text{C}$	-	29	44	m Ω
		$V_G = 57\text{ V}$, $I_{INPUT} = 1.5\text{ A}$, $T_A = 25^\circ\text{C}$	-	26	37	m Ω
	P-ch MOSFET	$V_G = -42\text{ V}$, $I_{INPUT} = -1.5\text{ A}$, $T_A = 25^\circ\text{C}$	-	95	147	m Ω
		$V_G = -48\text{ V}$, $I_{INPUT} = -1.5\text{ A}$, $T_A = 25^\circ\text{C}$	-	83	125	m Ω
		$V_G = -57\text{ V}$, $I_{INPUT} = -1.5\text{ A}$, $T_A = 25^\circ\text{C}$	-	76	107	m Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. INPUT1 is connected to G3 and G4 and also INPUT2 is connected to G1 and G2 like below.



TYPICAL CHARACTERISTICS (Q1 OR Q4 N-CHANNEL)

($T_J = 25^\circ\text{C}$ unless otherwise noted.)

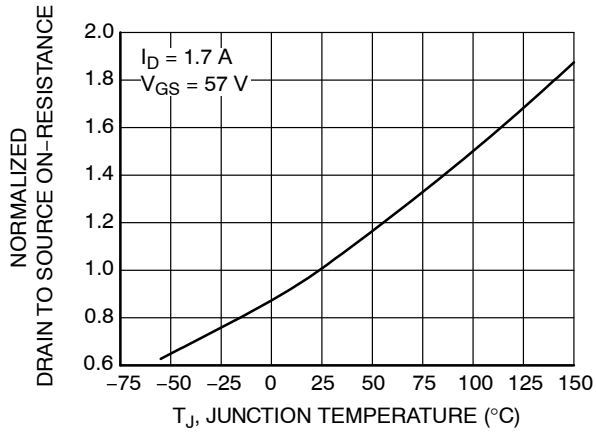


Figure 5. Normalized On Resistance vs. Junction Temperature

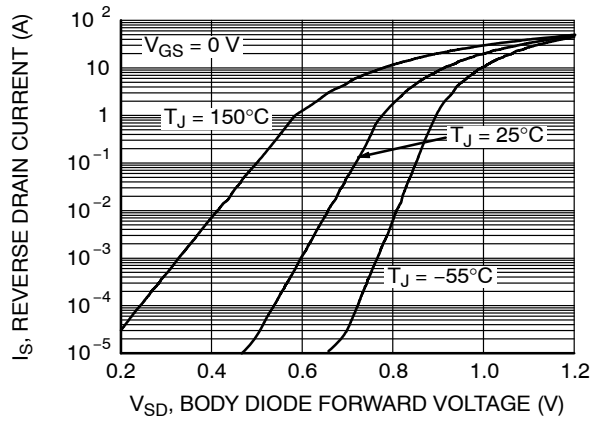


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

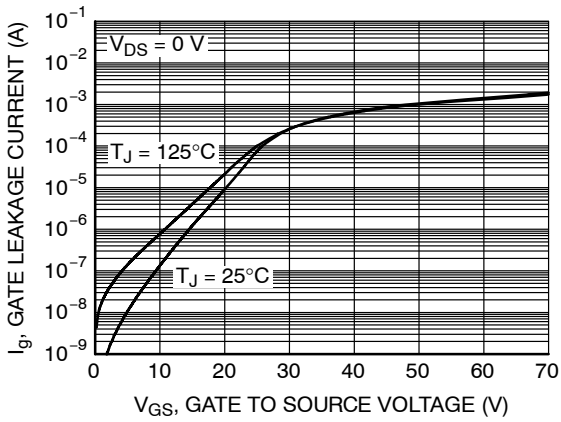


Figure 7. Gate Leakage Current vs. Gate to Source Voltage

TYPICAL CHARACTERISTICS (Q2 OR Q3 P-CHANNEL)

($T_J = 25^\circ\text{C}$ unless otherwise noted.)

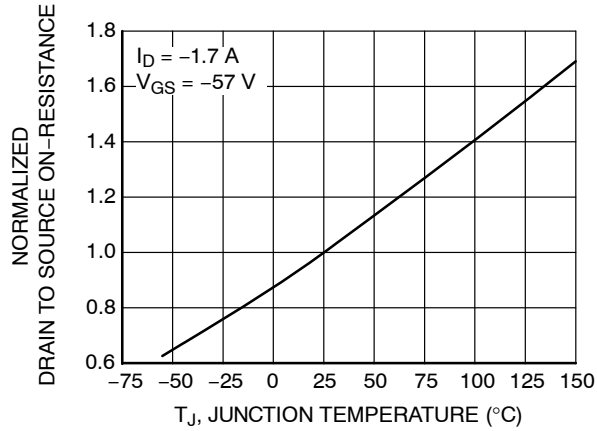


Figure 8. Normalized On Resistance vs. Junction Temperature

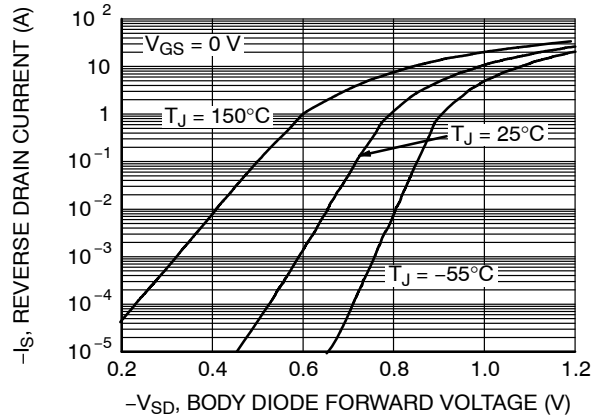


Figure 9. Source to Drain Diode Forward Voltage vs. Source Current

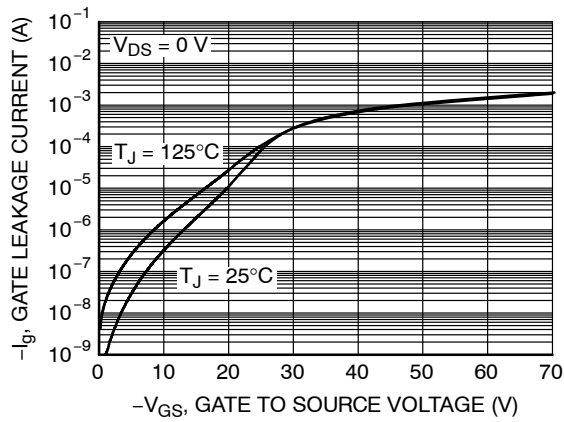


Figure 10. Gate Leakage Current vs. Gate to Source Voltage

FDMQ8205A

TYPICAL CHARACTERISTICS (Q1 + Q3 OR Q2 + Q4 IN SERIAL)

($T_J = 25^\circ\text{C}$ unless otherwise noted.)

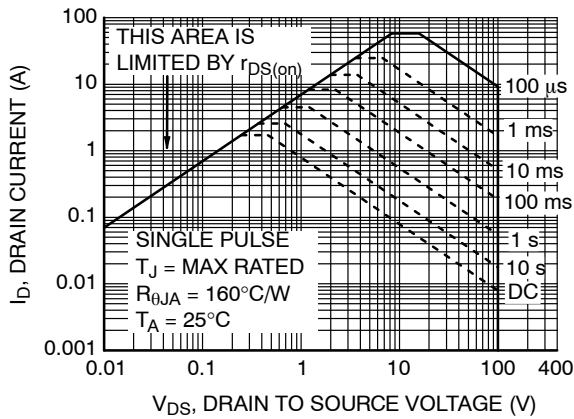


Figure 11. Forward Bias Safe Operating Area

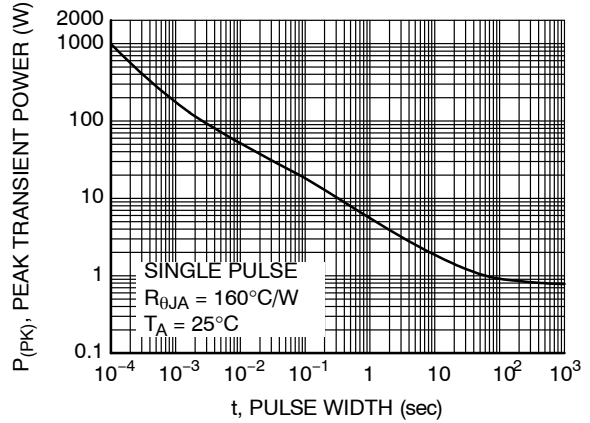


Figure 12. Single Pulse Maximum Power Dissipation

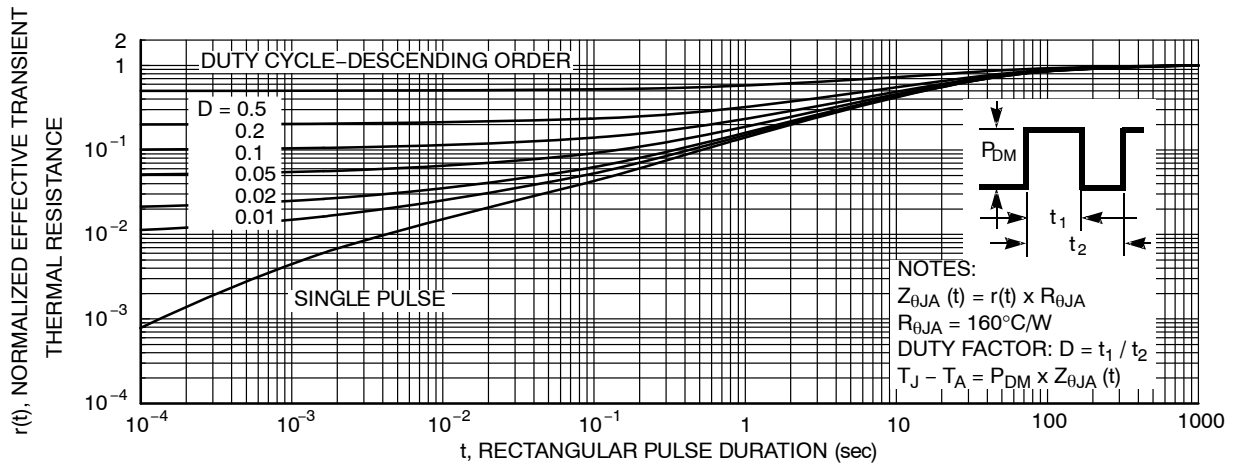


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Shipping [†]
FDMQ8205A	FDMQ8205A	WDFN12 5x4.5, 0.8P MLP4.5x5 (Pb-Free)	13"	12 mm	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

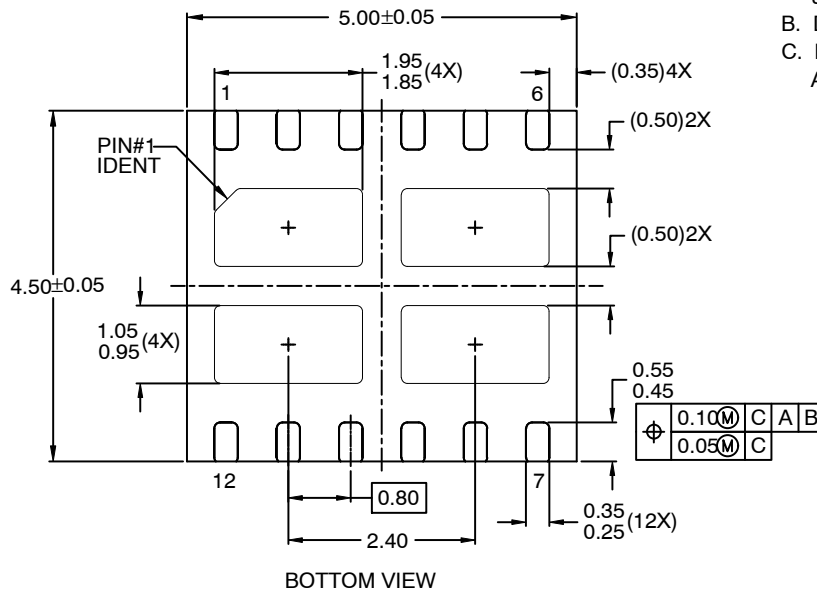
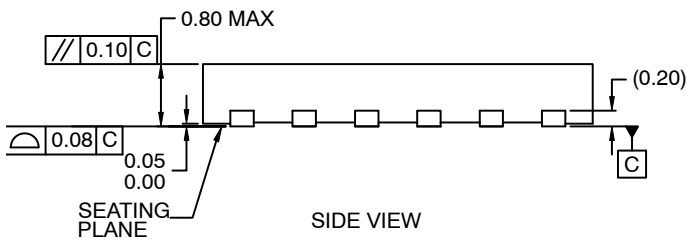
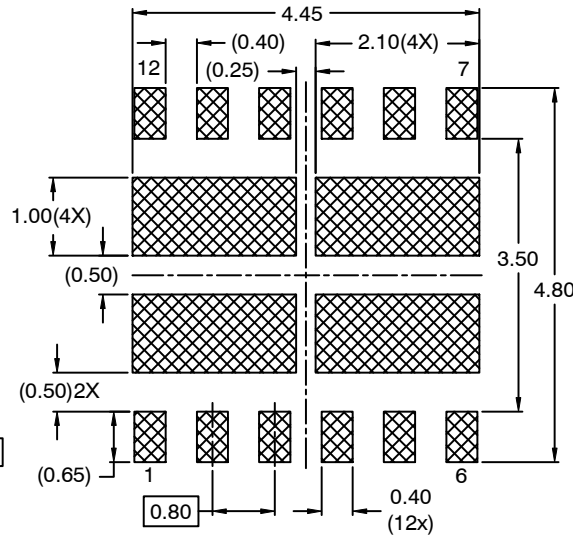
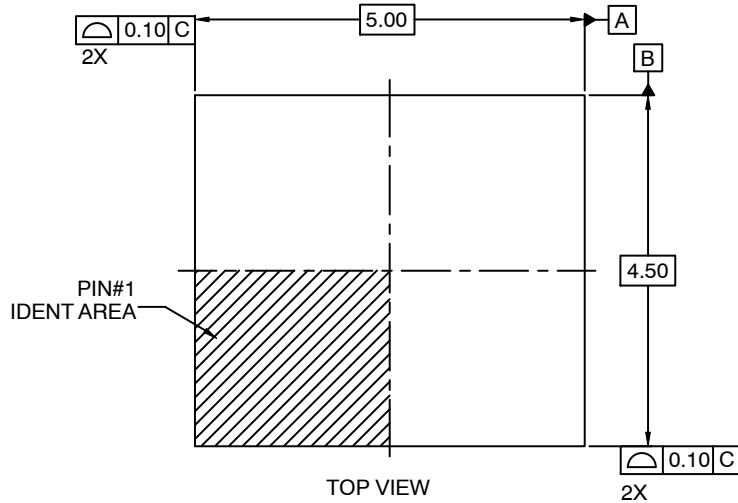
PACKAGE DIMENSIONS

ON Semiconductor®



WDFN12 5x4.5, 0.8P
CASE 511CS
ISSUE O

DATE 31 AUG 2016



NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO-229 REGISTRATION
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

DOCUMENT NUMBER:	98AON13607G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	WDFN12 5X4.5, 0.8P	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales