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# A5191HRT

# HART Modem

## Description

The A5191HRT is a single−chip, CMOS modem for use in highway addressable remote transducer (HART) field instruments and masters. The modem and a few external passive components provide all of the functions needed to satisfy HART physical layer requirements including modulation, demodulation, receive filtering, carrier detect, and transmit−signal shaping.

The A5191HRT uses phase continuous frequency shift keying (FSK) at 1200 bits per second. To conserve power the receive circuits are disabled during transmit operations and vice versa. This provides the half−duplex operation used in HART communications.

## Features

- Single−chip, Half−duplex 1200 Bits per Second FSK Modem
- Bell 202 Shift Frequencies of 1200 Hz and 2200 Hz
- 3.0 V – 5.5 V Power Supply
- Transmit−signal Wave Shaping
- Receive Band−pass Filter
- Low Power: Optimal for Intrinsically Safe Applications
- Compatible with 3.3 V or 5 V Microcontroller
- Internal Oscillator Requires 460.8 kHz Crystal or Ceramic Resonator
- Meets HART Physical Layer Requirements
- Industrial Temperature Range of −40°C to +85°C
- Available in 28−pin PLCC, 32−pin QFN and 32−pin LQFP Packages
- These are Pb−Free Devices

## Applications

- HART Multiplexers
- HART Modem Interfaces
- 4 – 20 mA Loop Powered Transmitters

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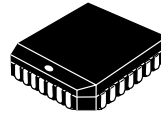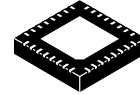
| PLCC–28 | QFN–32 | LQFP–32 |
|---|---|---|
| P SUFFIX | N SUFFIX | L SUFFIX |
| CASE 776AA | CASE 488AM | CASE 561AB |

**MARKING DIAGRAMS**

(Top Views)

1 28

A5191HRTPG
AWLYYWW

A5191
HRTL
AWLYYWWG

32
1

1

A5191
HRTNG
AWLYYWW
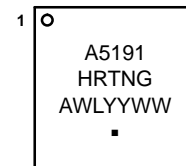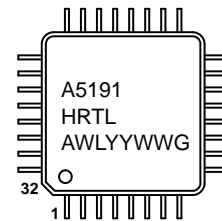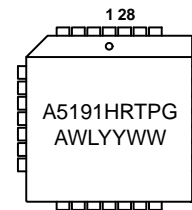
A5191HRTxx = Specific Device Code
xx = P (PLCC), L (LQFP) or N (QFN)
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G or ▪ = Pb−Free Package

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

**April, 2018 – Rev. 10**

Publication Order Number:
**A5191HRT/D**

# A5191HRT
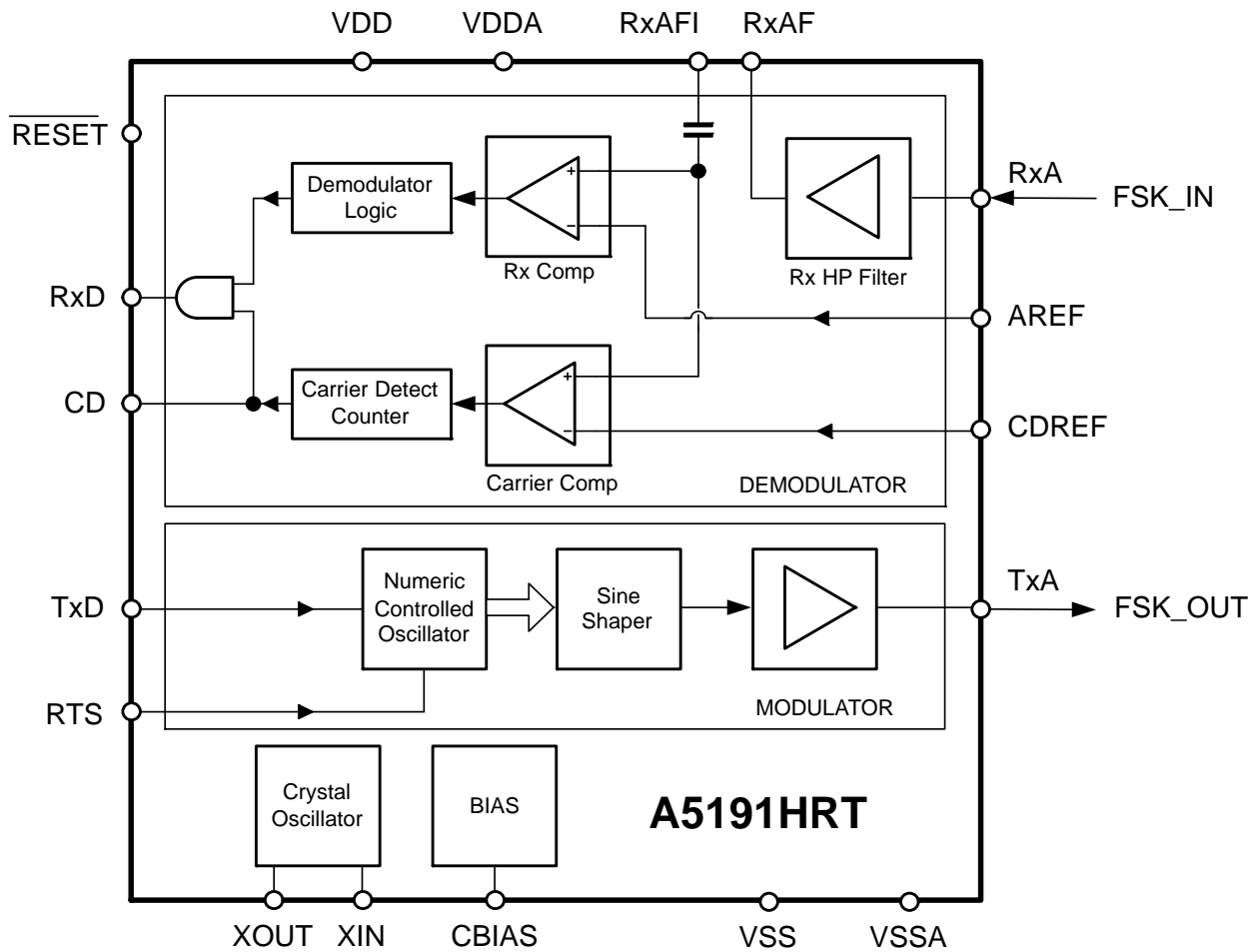
## BLOCK DIAGRAM



**Figure 1. Block Diagram A5191HRT**

## ELECTRICAL SPECIFICATIONS

**Table 1. ABSOLUTE MAXIMUM RATINGS** (Notes 1 and 2)

| Symbol | Parameter | Min | Max | Units |
|--------|-----------|-----|-----|-------|
| $T_A$ | Ambient | −40 | +85 | °C |
| $T_S$ | Storage Temperature | −55 | +150 | °C |
| $T_J$ | Junction Temperature | −40 | +85 | °C |
| $V_{DD}$ | Supply Voltage | −0.3 | 6.0 | V |
| $V_{IN}$, $V_{OUT}$ | DC Input, Output | −0.3 | VDD + 0.3 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. CMOS devices are damaged by high–energy electrostatic discharge. Devices must be stored in conductive foam or with all pins shunted. Precautions should be taken to avoid application of voltages higher than the maximum rating. Stresses above absolute maximum ratings may result in damage to the device.
2. Remove power before insertion or removal of this device.

# A5191HRT

**Table 2. DC CHARACTERISTICS** ($V_{DD}$ = 3.0 V to 5.5 V, $V_{SS}$ = 0 V, $T_A$ = −40°C to +85°C)

| Symbol | Parameter | $V_{DD}$ | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Voltage, Low | 3.0 – 5.5 V | | | 0.3 * $V_{DD}$ | V |
| $V_{IH}$ | Input Voltage, High | 3.0 – 5.5 V | 0.7 * $V_{DD}$ | | | V |
| $V_{OL}$ | Output Voltage, Low ($I_{OL}$ = 0.67 mA) | 3.0 – 5.5 V | | | 0.4 | V |
| $V_{OH}$ | Output Voltage, High ($I_{OH}$ = −0.67 mA) | 3.0 – 5.5 V | 2.4 | | | V |
| $C_{IN}$ | Input Capacitance of:<br>Analog Input<br>RXA<br>Digital Input | | | 2.9<br>25<br>3.5 | | pF<br>pF<br>pF |
| $I_{IL}/I_{IH}$ | Input Leakage Current | | | | ±500 | nA |
| $I_{OLL}$ | Output Leakage Current | | | | ±10 | µA |
| $I_{DDA}$ | Power Supply Current<br>(RBIAS = 500 kΩ, AREF = 1.235 V) | 3.3 V<br>5.0 V | 150<br>150 | 330<br>300 | 450<br>600 | µA<br>µA |
| $I_{DDD}$ | Dynamic Digital Current | 5.0 V | 25 | | 200 | µA |
| $A_{REF}$ | Analog Reference | 3.3 V<br>5.0 V | 1.2 | 1.235<br>2.5 | 2.6 | V<br>V |
| $CD_{REF}$ (Note 3) | Carrier Detect Reference (AREF − 0.08 V) | 3.3 V<br>5.0 V | | 1.15<br>2.42 | | V |
| $C_{BIAS}$ | Comparator Bias Current<br>(RBIAS = 500 kΩ, AREF = 1.235 V) | | | 2.5 | | µA |

3. The HART specification requires carrier detect (CD) to be active between 80 and 120 mVp−p. Setting CDREF at AREF − 0.08 VDC will set the carrier detect to a nominal 100 mVp−p.

**Table 3. AC CHARACTERISTICS** ($V_{DD}$ = 3.0 V to 5.5 V, $V_{SS}$ = 0 V, $T_A$ = −40°C to +85°C) (Note 4)

| Pin Name | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| RxA | Receive analog input<br>Leakage current<br>Frequency – mark (logic 1)<br>Frequency – space (logic 0) | 1190<br>2180 | 1200<br>2200 | ±150<br>1210<br>2220 | nA<br>Hz<br>Hz |
| RxAF | Output of the high−pass filter<br>Slew rate<br>Gain bandwidth (GBW)<br>Voltage range | 150<br>0.15 | 0.025 | $V_{DD}$ − 0.15 | V/µs<br>kHz<br>V |
| RxAFI | Carrier detect and receive filter input<br>Leakage current | | | ±500 | nA |
| TxA | Modulator output<br>Frequency – mark (logic 1)<br>Frequency – space (logic 0)<br>Amplitude (AREF 1.235 V)<br>Slew Rate – mark (logic 1)<br>Slew Rate – space (logic 0)<br>Loading (AREF = 1.235 V) | 30 | 1196.9<br>2194.3<br>500<br>1860<br>3300 | | Hz<br>Hz<br>mV<br>V/s<br>V/s<br>kΩ |
| RxD | Receive digital output<br>Rise/fall time | 20 | | | ns |
| CD | Carrier detect output<br>Rise/fall time | 20 | | | ns |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
4. The modular output frequencies are proportional to the input clock frequency (460.8 kHz).

# A5191HRT

**Table 4. MODEM CHARACTERISTICS** ($V_{DD}$ = 3.0 V to 5.5 V, $V_{SS}$ = 0 V, $T_A$ = −40°C to +85°C)

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| Demodulator jitter<br>Conditions<br>1. Input frequencies at 1200 Hz ± 10 Hz, 2200 Hz ± 20 Hz<br>2. Clock frequency of 460.8 kHz ± 0.1%<br>3. Input (RxA) asymmetry, 0 | | | 12 | % of 1 bit |

**Table 5. CERAMIC RESONATOR – External Clock Specifications** ($V_{DD}$ = 3.0 V to 5.5 V, $V_{SS}$ = 0 V, $T_A$ = −40°C to +85°C)

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| Resonator<br>  Tolerance<br>  Frequency | | <br><br>460.8 | 1.0 | %<br>kHz |
| External<br>  Clock frequency<br>  Duty cycle<br>  Amplitude | <br>456.2<br>40 | <br>460.8<br>50<br>$V_{OH} - V_{OL}$ | <br>465.4<br>60 | <br>kHz<br>%<br>V |

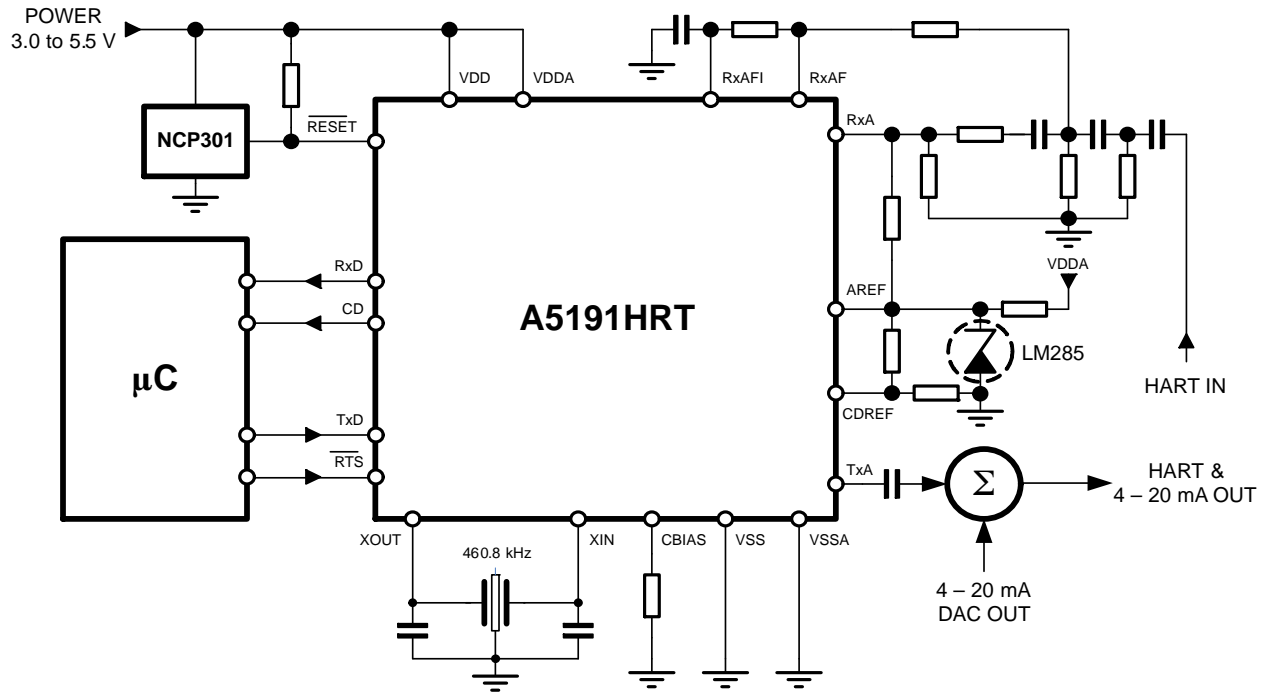## TYPICAL APPLICATION



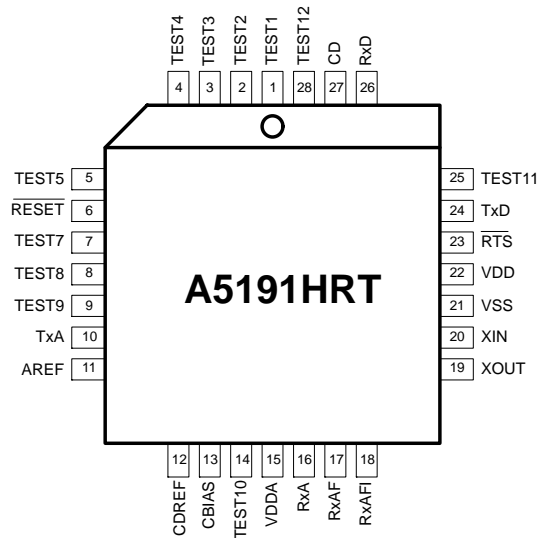**Figure 2. Application Diagram A5191HRT**

# A5191HRT



**Figure 3. Pin Out A5191HRT in 28-pin PLCC**

**Table 6. PIN OUT SUMMARY 28–PIN PLCC**

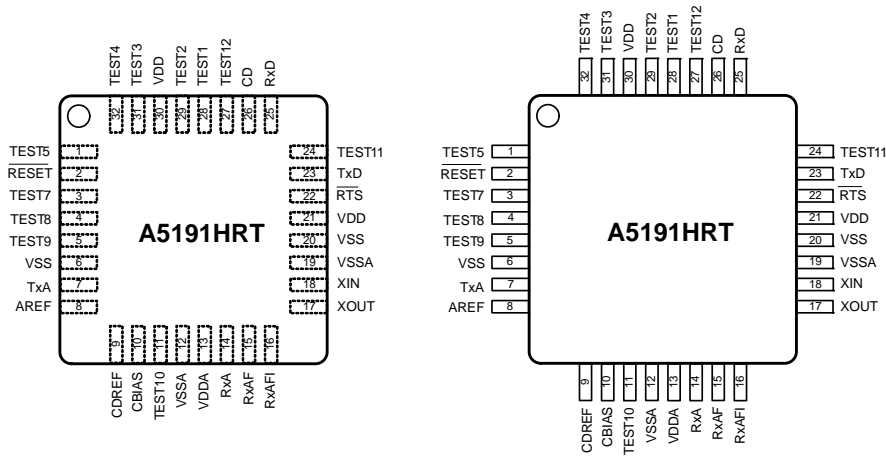| Pin No. | Signal Name | Type | Pin Description |
|---|---|---|---|
| 1 | TEST1 | Input | Connect to VSS |
| 2, 3, 4 | TEST2, 3, 4 | – | Do Not Connect |
| 5 | TEST5 | Input | Connect to VSS |
| 6 | RESETB | Input | Reset all digital logic when low |
| 7, 8, 9 | TEST7, 8, 9 | Input | Connect to VSS |
| 10 | TxA | Output | Transmit Data Modulator output |
| 11 | AREF | Input | Analog reference voltage |
| 12 | CDREF | Input | Carrier detect reference voltage |
| 13 | CBIAS | Output | Comparator bias current |
| 14 | TEST10 | Input | Connect to VSS |
| 15 | VDDA | Power | Analog supply voltage |
| 16 | RxA | Input | Receive Data Modulator input |
| 17 | RxAF | Output | Analog receive filter output |
| 18 | RxAFI | Input | Analog receive comparator input |
| 19 | XOUT | Output | Crystal oscillator output |
| 20 | XIN | Input | Crystal oscillator input |
| 21 | VSS | Ground | Ground |
| 22 | VDD | Power | Digital supply voltage |
| 23 | RTSB | Input | Request to send |
| 24 | TxD | Input | Input transmit date, transmitted HART data stream from microcontroller |
| 25 | TEST11 | – | Do Not Connect |
| 26 | RxD | Output | Received demodulated HART data to microcontroller |
| 27 | CD | Output | Carrier detect output |
| 28 | TEST12 | – | Do Not Connect |

# A5191HRT



**Figure 4. Pin Out A5191HRT in 32-pin QFN and LQFP (top view)**

**Table 7. PIN OUT SUMMARY 32−PIN QFN AND LQFP**

| Pin No. | Signal Name | Type | Pin Description |
|---------|-------------|------|-----------------|
| 1 | TEST5 | Input | Connect to VSS |
| 2 | RESETB | Input | Reset all logic when low, connect to VDD for normal operation |
| 3, 4, 5 | TEST7, 8, 9 | Input | Connect to VSS |
| 6 | VSS | Ground | Digital ground |
| 7 | TxA | Output | Transmit Data Modulator output |
| 8 | AREF | Input | Analog reference voltage |
| 9 | CDREF | Input | Carrier detect reference voltage |
| 10 | CBIAS | Output | Comparator bias current |
| 11 | TEST10 | Input | Connect to VSS |
| 12 | VSSA | Ground | Analog ground |
| 13 | VDDA | Power | Analog supply voltage |
| 14 | RxA | Input | Receive Data Modulator input |
| 15 | RxAF | Output | Analog receive filter output |
| 16 | RxAFI | Input | Analog receive comparator input |
| 17 | XOUT | Output | Crystal oscillator output |
| 18 | XIN | Input | Crystal oscillator input |
| 19 | VSSA | Ground | Analog ground |
| 20 | VSS | Ground | Digital ground |
| 21 | VDD | Power | Digital supply voltage |
| 22 | RTSB | Input | Request to send |
| 23 | TxD | Input | Input transmit data, transmit HART data stream from microcontroller |
| 24 | TEST11 | – | Do Not Connect |
| 25 | RxD | Output | Received demodulated HART data to microcontroller |
| 26 | CD | Output | Carrier detect output |
| 27 | TEST12 | – | Do Not Connect |
| 28 | TEST1 | Input | Connect to VSS |
| 29 | TEST2 | – | Do Not Connect |
| 30 | VDD | Power | Digital supply voltage |
| 31, 32 | TEST3, 4 | – | Do Not Connect |
| EP | Exposed Pad | Power | Connect to VSS (QFN only) |

# A5191HRT

**Pin Descriptions**

### Table 8. PIN DESCRIPTIONS

| Symbol | Pin Name | Description |
|---|---|---|
| AREF | Analog reference voltage | Receiver Reference Voltage. Normally 1.23 V is selected (in combination with VDDA = 3.3 V). See Table 2. |
| CDREF | Carrier detect reference voltage | Carrier Detect Reference voltage. The value should be 85 mV below AREF to set the carrier detection to a nominal of 100 $mV_{p-p}$. |
| RESETB | Reset digital logic | When at logic low ($V_{SS}$) this input holds all the digital logic in reset. During normal operation RESETB should be at $V_{DD}$. RESETB should be held low for a minimum of 10 nS after $V_{DD}$ = 2.5 V as shown in Figure 14. |
| RTSB | Request to send | Active−low input selects the operation of the modulator. TxA is enabled when this signal is low. This signal must be held high during power−up. |
| RxA | Analog receive input | Receive Data Demodulator Input. Accepts a HART 1200 / 2200 Hz FSK modulated waveform input. |
| RxAFI | Analog receive comparator input | Positive input of the carrier detect comparator and the receiver filter comparator. |
| TxD | Digital transmit input | Input to the modulator accepts digital data in NRZ form. When TxD is low, the modulator output frequency is 2200 Hz. When TxD is high, the modulator output frequency is 1200 Hz. |
| XIN | Oscillator input | Input to the internal oscillator must be connected to a parallel mode 460.8 kHz ceramic resonator when using the internal oscillator or grounded when using an external 460.8 kHz clock signal. |
| CBIAS | Comparator bias current | Connection to the external bias resistor. $R_{BIAS}$ should be selected such that AREF / $R_{BIAS}$ = 2.5 μA ± 5 % |
| CD | Carrier detect output | Output goes high when a valid input is recognized on RxA. If the received signal is greater than the threshold specified on CDREF for four cycles of the RxA signal, the valid input is recognized. |
| RxAF | Analog receive filter output | The output of the three pole high pass receive data filter |
| RxD | Digital receive output | Signal outputs the digital receive data. When the received signal (RxA) is 1200 Hz, RxD outputs logic high. When the received signal (RxA) is 2200 Hz, RxD outputs logic low. The HART receive data stream is only active if Carrier Detect (CD) is high. |
| TxA | Analog transmit output | Transmit Data Modulator Output. A trapezoidal shaped waveform with a frequency of 1200 Hz or 2200 Hz corresponding to a data value of 1 or 0 respectively applied to TxD. TxA is active when RTSB is low. TxA equals 0.5 V when RTSB is high. |
| XOUT | Oscillator output | Output from the internal oscillator must be connected to an external 460.8 kHz clock signal or to a parallel mode 460.8 kHz ceramic resonator when using the internal oscillator. |
| TEST(12:1) | Factory test | Factory test pins; for normal operation, tie these signals as per Tables 6 and 7 |
| VDD | Digital power | Power for the digital modem circuitry |
| VDDA | Analog supply voltage | Power for the analog modem circuitry |
| VSS | Ground | Digital ground (and Analog ground in the case of PLCC package) |
| VSSA | Analog ground | Analog ground |

## Functional Description

The A5191HRT is a single-chip modem for use in Highway Addressable Remote Transducer (HART) field instruments and masters. The modem IC contains a transmit data modulator with signal shaper, carrier detect circuitry, an analog receiver, demodulator circuitry and a crystal oscillator, as shown in the block diagram in Figure 1.

The modulator accepts digital data at its digital input TxD and generates a sine shaped FSK modulated signal at the analog output TxA. A digital "1" or mark is represented with a frequency of 1200 Hz. A digital "0" or space is represented with a frequency of 2200 Hz. The used bit rate is 1200 baud.

The demodulator receives the FSK signal at its analog input, filters it with a band-pass filter and generates 2 digital signals: RxD: Received Data and CD: Carrier Detect. At the digital output RxD the original modulated signal is received. CD outputs the Carrier Detect signal. It goes logic high if the received signal is above 100 mVpp during 4 consecutive carrier periods.

The oscillator provides the modem with a stable time base using either a simple external resonator or an external clock source.

## Detailed Description

### Modulator

The modulator accepts digital data in NRZ form at the TxD input and generates the FSK modulated signal at the TxA output.
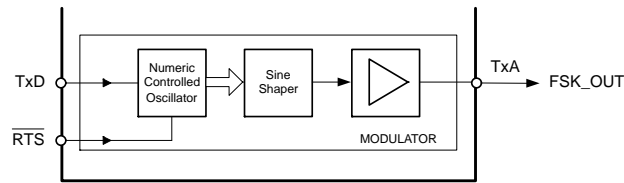


**Figure 5. Modulator Block Diagram**

A logic "1" or mark is represented by a frequency fm = 1200 Hz. A logic "0"or space is represented by a frequency fs = 2200 Hz.
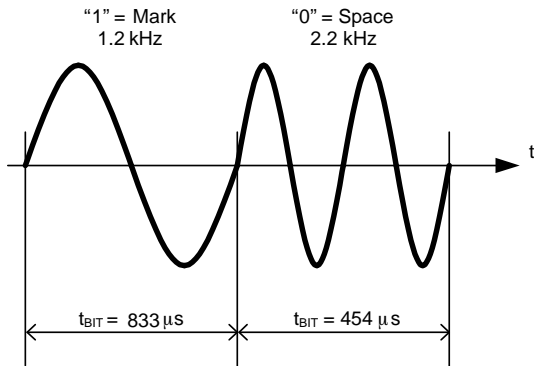


**Figure 6. Modulation Timing**

The Numeric Controlled Oscillator NCO works in a phase continuous mode preventing abrupt phase shifts when switching between mark and space frequency. The control signal Request To Send RTSB enables the NCO. When RTSB is logic low the modulator is active and A5191HRT is in transmit mode. When RTSB is logic high the modulator is disabled and A5191HRT is in receive mode.

The digital outputs of the NCO are shaped in the Wave Shaper block to a trapezoidal signal. This circuit controls the rising and falling edge to be inside the standard HART waveshape limits. Figure 7 shows the transmit-signal forms captured at TxA for mark and space frequency. The slew rates are $SR_m$ = 1860 V/s at the mark frequency and $SR_s$ = 3300 V/s at the space frequency. For AREF = 1.235 V, TxA will have a voltage swing from approximately 0.25 to 0.75 $V_{DC}$.
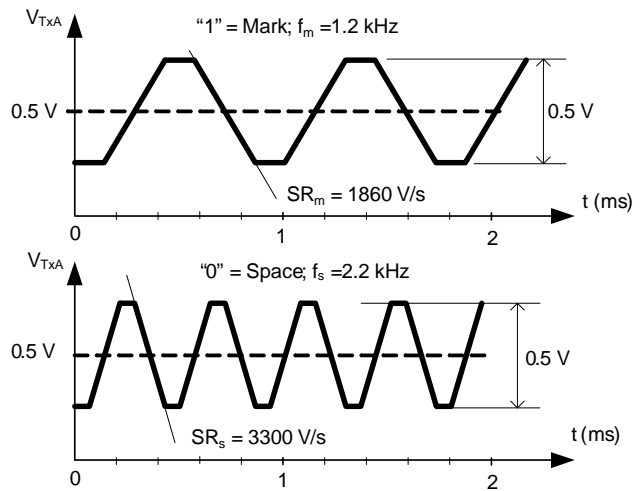


**Figure 7. Modulator shaped output signal for Mark and Space frequency at TxA pin.**

### Demodulator

The demodulator accepts a FSK signal at the RxA input and reconstructs the original modulated signal at the RxD output. Figure 8 illustrates the demodulation process.
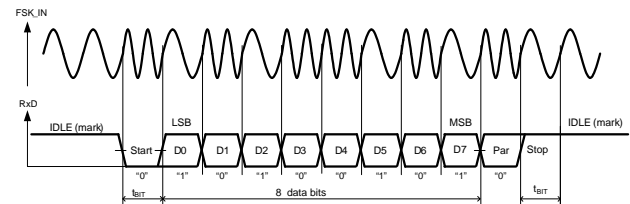


**Figure 8. Modulation Timing**

This HART bit stream follows a standard 11-bit UART frame with 1 startbit, 8 databits, 1 paritybit (odd) and 1 stopbit. The communication speed is 1200 baud.

# A5191HRT

## Receive Filter and Comparator

The received FSK signal first is filtered using a band-pass filter build around the low noise receiver operational amplifier "Rx HP filter". This filter blocks interferences outside the HART signal band.
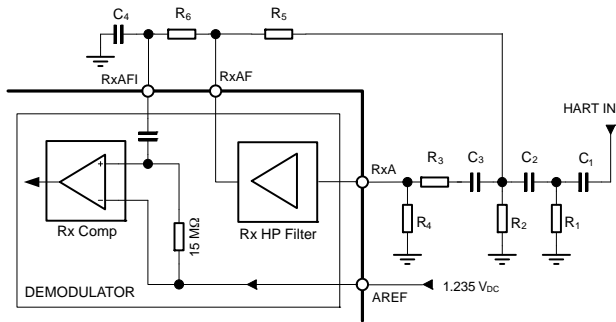


**Figure 9. Demodulator Receive Filter and Signal Comparator**

The filter output is fed into the Rx comparator. The threshold value equals the analog ground making the comparator to toggle on every zero crossing of the filtered FSK signal. The maximum demodulator jitter is 12 % of one bit given the input frequencies are within the HART specifications, a clock frequency of 460.8 kHz (±1.0 %) and zero input (RxA) asymmetry.

## Carrier Detect Circuitry

Low HART input signal levels increases the risk for the generation of bit errors. Therefore the minimum signal amplitude is set to 80 – 120 mVpp. If the received signal is below this level the demodulator is disabled.

This level detection is done in the Carrier Detector. The output of the demodulator is qualified with the carrier detect signal (CD), therefore, only RxA signals large enough to be detected (100 mVp-p typically) by the carrier detect circuit produce received serial data at RxD.
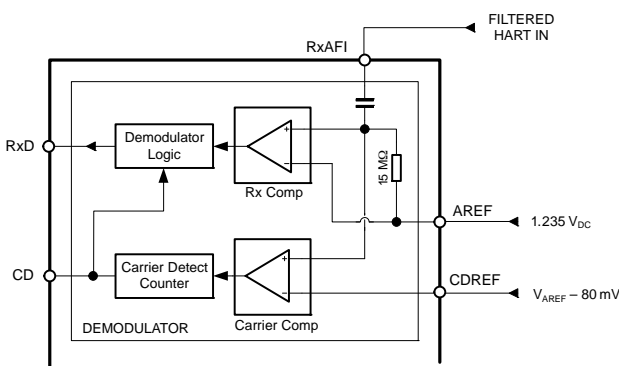


**Figure 10. Demodulator Carrier and Signal Comparator**

The carrier detect comparator shown in Figure 10 generates logic low output if the RxAFI voltage is below CDREF. The comparator output is fed into a carrier detect block. The carrier detect block drives the carrier detect

output pin CD high if RTSB is high and four consecutive pulses out of the comparator have arrived. CD stays high as long as RTSB is high and the next comparator pulse is received in less than 2.5 ms. Once CD goes inactive, it takes four consecutive pulses out of the comparator to assert CD again. Four consecutive pulses amount to 3.33 ms when the received signal is 1200 Hz and to 1.82 ms when the received signal is 2200 HZ.

## Miscellaneous Analog Circuitry

### Voltage References

The A5191HRT requires two voltage references, AREF and CDREF. AREF sets the DC operating point of the internal operational amplifiers and is the reference for the Rx comparator. If A5191HRT operates at $V_{DD}$ = 3.3 V the ON Semiconductor LM285D 1.235 V reference is recommended.

The level at which CD (Carrier Detect) becomes active is determined by the DC voltage difference (CDREF - AREF). Selecting a voltage difference of 80 mV will set the carrier detect to a nominal 100 $mV_{p-p}$.

### Bias Current Resistor

The A5191HRT requires a bias current resistor $R_{BIAS}$ to be connected between CBIAS and $V_{SS}$. The bias current controls the operating parameters of the internal operational amplifiers and comparators and should be set to 2.5 μA.
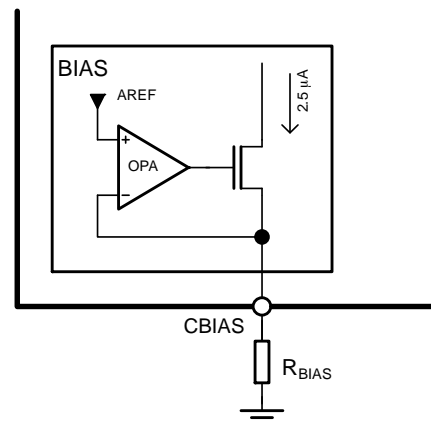


**Figure 11. Bias Circuit**

The value of the bias current resistor is determined by the reference voltage AREF and the following formula:

$$R_{BIAS} = \frac{AREF}{2.5 \ \mu A}$$

The recommended bias current resistor is 500 KΩ when AREF is equal to 1.235 V.

### Oscillator

The A5191HRT requires a 460.8 kHz clock signal. This can be provided by an external clock or a resonator connected to the A5191HRT internal oscillator.

## Internal Oscillator Option

The oscillator cell will function with either a 460.8 kHz crystal or ceramic resonator. A parallel resonant ceramic resonator can be connected between XIN and XOUT. Figure 12 illustrates the crystal option for clock generation using a 460.8 kHz (±1 % tolerance) parallel resonant crystal and two tuning capacitors Cx. The actual values of the capacitors may depend on the recommendations of the manufacturer of the resonator. Typically, capacitors in the range of 100 pF to 470 pF are used.
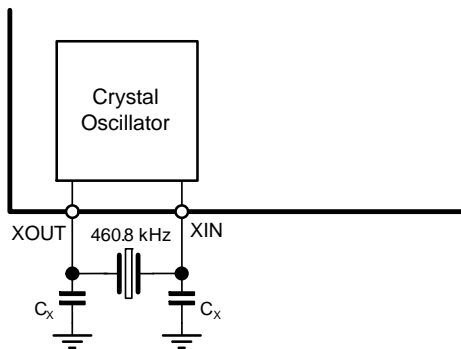


**Figure 12. Crystal Oscillator**

## External Clock Option

It may be desirable to use an external 460.8 kHz clock as shown in Figure 13 rather than the internal oscillator. In addition, the A5191HRT consumes less current when an external clock is used. Minimum current consumption occurs with the clock connected to XOUT and XIN connected to $V_{SS}$.
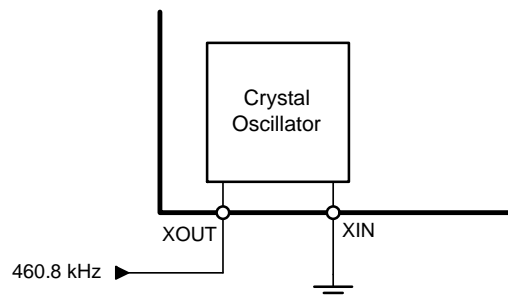


**Figure 13. Oscillator with External Clock**

## Power On Reset

During start-up the RESETB pin should be kept low until the voltage level on $V_{DD}$ is above the minimum level $V_{DDH}$ = 2.5 V to guarantee correct operation of the digital circuitry. As illustrated in Figure 14 RESETB should be kept low for at least $t_{POR}$ = 10 ns after this threshold level is reached.
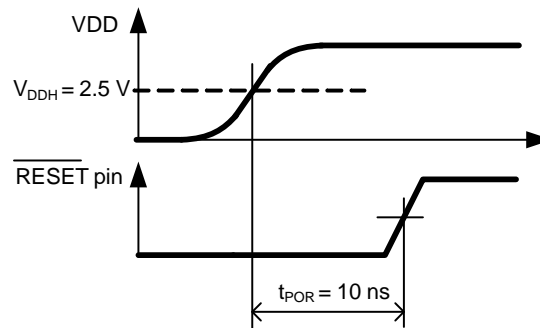


**Figure 14. Power On Reset Timing**

**Ordering Information**

The A5191HRT is available in a 28−pin plastic leaded chip carrier (PLCC), 32−pin quad flat no−lead (QFN) and 32−pin low−profile quad flat pack (LQFP). Use the following part numbers when ordering. Contact your local sales representative for more information: www.onsemi.com.

**Table 9. ORDERING INFORMATION**

| Part Number | Package | Shipping Configuration | Temperature Range |
|---|---|---|---|
| A5191HRTLG−XTD (Industrial) | 32−pin LQFP Green / RoHS compliant | 250 Units / Tray | −40°C to +85°C |
| A5191HRTLG−XTP (Industrial) | 32−pin LQFP Green / RoHS compliant | 2500 Units / Tape & Reel | −40°C to +85°C |
| A5191HRTPG−XTD (Industrial) | 28−pin PLCC Green / RoHS compliant | 37 Units / Tube | −40°C to +85°C |
| A5191HRTPG−XTP (Industrial) | 28−pin PLCC Green / RoHS compliant | 750 Units / Tape & Reel | −40°C to +85°C |
| A5191HRTNG−XTD (Industrial) | 32−pin QFN Green / RoHS compliant | 60 Units / Tube/Tray | −40°C to +85°C |
| A5191HRTNG−XTP (Industrial) | 32−pin QFN Green / RoHS compliant | 5000 Units / Tape & Reel | −40°C to +85°C |
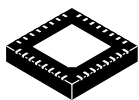
**QFN32 5x5, 0.5P**
CASE 488AM
ISSUE A

DATE 23 OCT 2013

**SCALE 2:1**

1   32

**PIN ONE LOCATION**

| △ | 0.15 | C |

| △ | 0.15 | C |
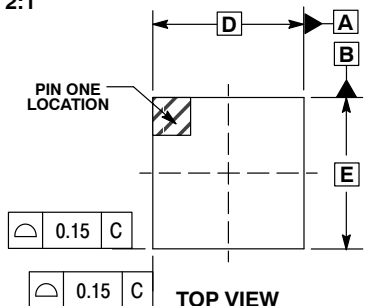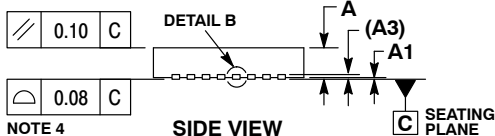
**TOP VIEW**
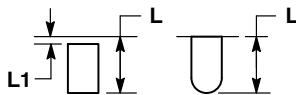
**DETAIL A**
**ALTERNATE TERMINAL CONSTRUCTIONS**

| ∥ | 0.10 | C |

**DETAIL B**

| △ | 0.08 | C |

**NOTE 4**    **SIDE VIEW**

A
(A3)
A1

C **SEATING PLANE**

**EXPOSED Cu**    **MOLD CMPD**
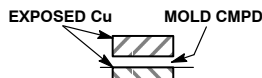
**DETAIL B**
**ALTERNATE CONSTRUCTION**

**DETAIL A**

D2    K

9

8

32X L    17

E2

1

32    25

32X b

e

e/2

**BOTTOM VIEW**

| ⊕ | 0.10 Ⓜ | C | A | B |
| ⊕ | 0.05 Ⓜ | C | | NOTE 3 |

**NOTES:**
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | |
| | MIN | MAX |
| --- | --- | --- |
| A | 0.80 | 1.00 |
| A1 | --- | 0.05 |
| A3 | 0.20 REF | |
| b | 0.18 | 0.30 |
| D | 5.00 BSC | |
| D2 | 2.95 | 3.25 |
| E | 5.00 BSC | |
| E2 | 2.95 | 3.25 |
| e | 0.50 BSC | |
| K | 0.20 | --- |
| L | 0.30 | 0.50 |
| L1 | --- | 0.15 |

**GENERIC MARKING DIAGRAM***

1  O

XXXXXXXX
XXXXXXXX
AWLYYWW▪

▪
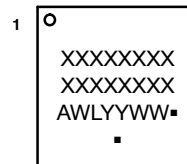
XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb–Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb–Free indicator, "G" or microdot " ▪ ", may or may not be present.
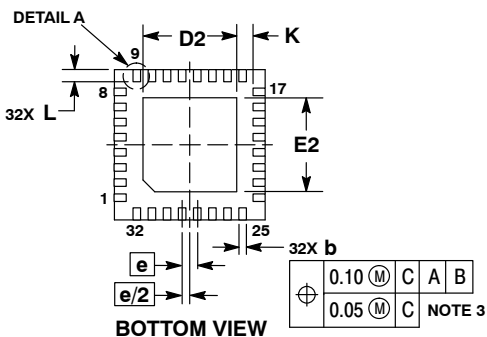
**RECOMMENDED SOLDERING FOOTPRINT***

5.30

3.35

32X 0.63

3.35    5.30

0.50 PITCH

32X 0.30
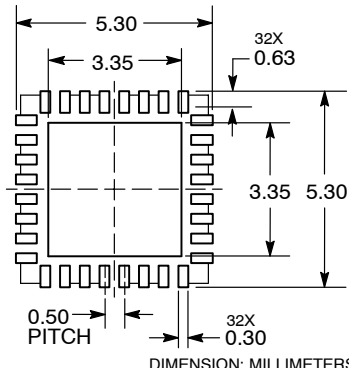
DIMENSION: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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| **DESCRIPTION:** | **QFN32 5x5 0.5P** | | **PAGE 1 OF 1** |

**LQFP–32, 7x7**
CASE 561AB–01
ISSUE O

DATE 19 JUN 2008
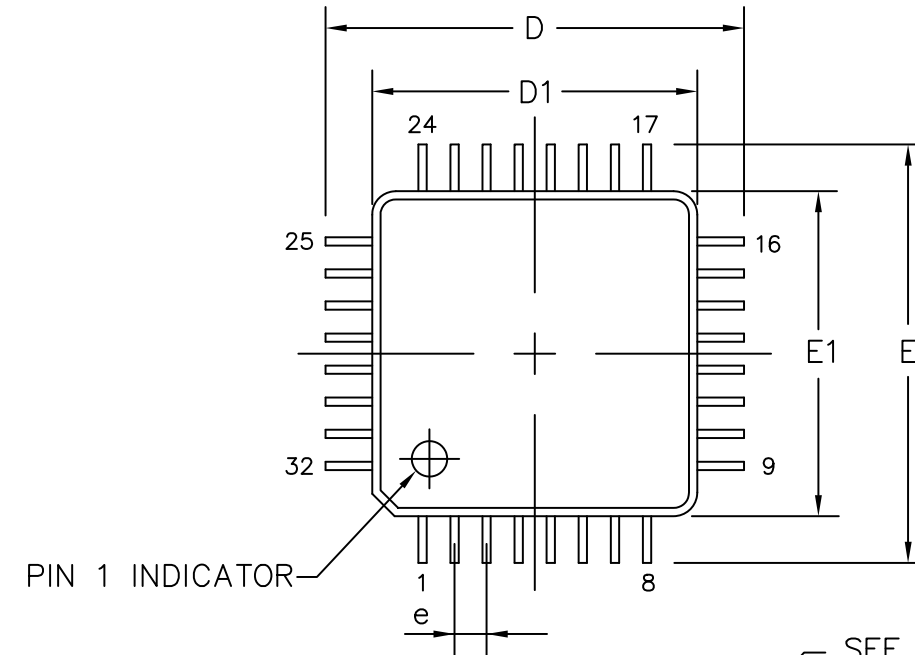
| SYMBOL | MIN | NOM | MAX |
|--------|-----|-----|-----|
| A | – | – | 1.60 |
| A1 | 0.05 | – | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| B | 0.30 | 0.37 | 0.45 |
| B1 | 0.30 | 0.35 | 0.40 |
| C | 0.09 | – | 0.20 |
| C1 | 0.09 | – | 0.16 |
| D | 9.00 BSC | | |
| D1 | 7.00 BSC | | |
| E | 9.00 BSC | | |
| E1 | 7.00 BSC | | |
| e | 0.80 BSC. | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 | | |
| R1 | 0.08 | – | 0.20 |
| $\alpha°$ | 11 | – | 13 |
| $\beta°$ | 0 | – | 7 |
| $\gamma°$ | 0 | – | – |

PIN 1 INDICATOR

SEE DETAIL A

SEE DETAIL B

DETAIL B

R1 RADIUS

DETAIL A
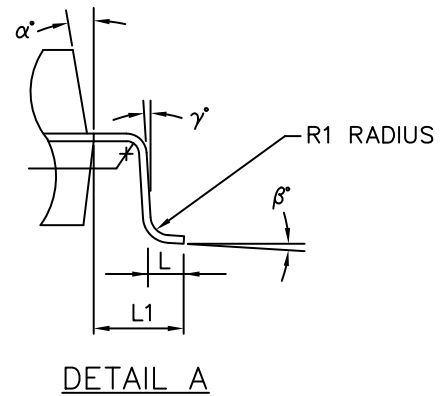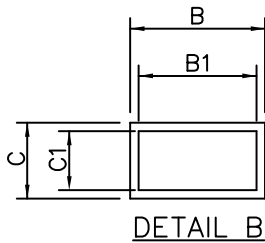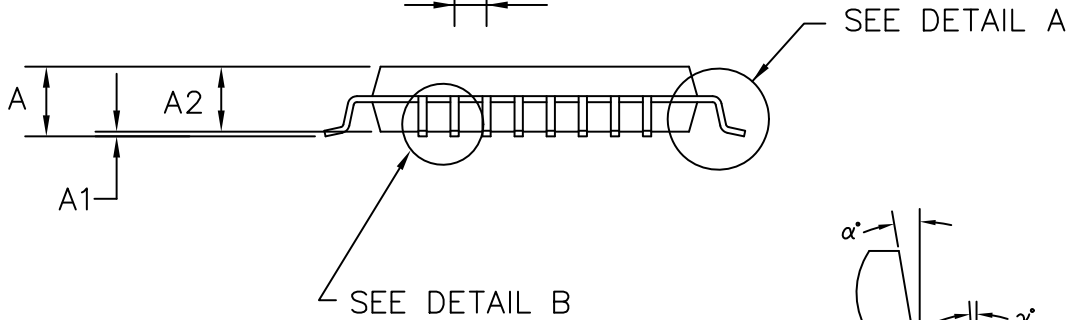
ALL DIMENSIONS IN MM

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|---|---|---|---|
| DESCRIPTION: | 32 LEAD LQFP, 7X7 | | PAGE 1 OF 1 |

**PLCC 28 LEAD**
CASE 776AA–01
ISSUE O

DATE 19 JUN 2008

.048/.042
2 PLCS

PIN 1
IDENTIFIER & ZONE

TOP VIEW

D

D1

E

E1

BOTTOM VIEW

B1

C

A

A2

A1

SEATING PLANE

e

B

R .045/.025

D2/E2

D2/E2
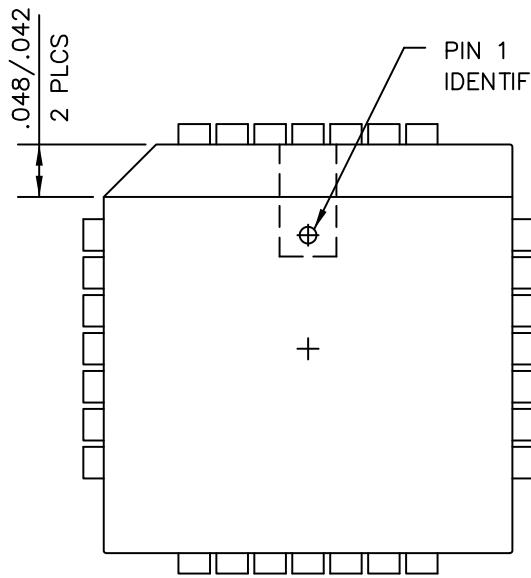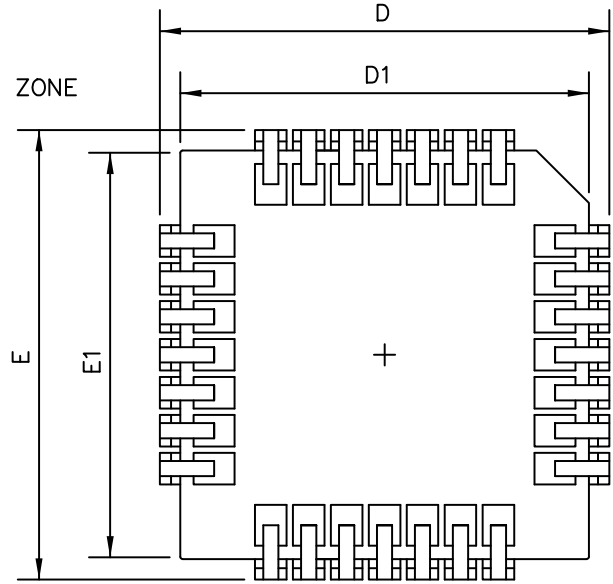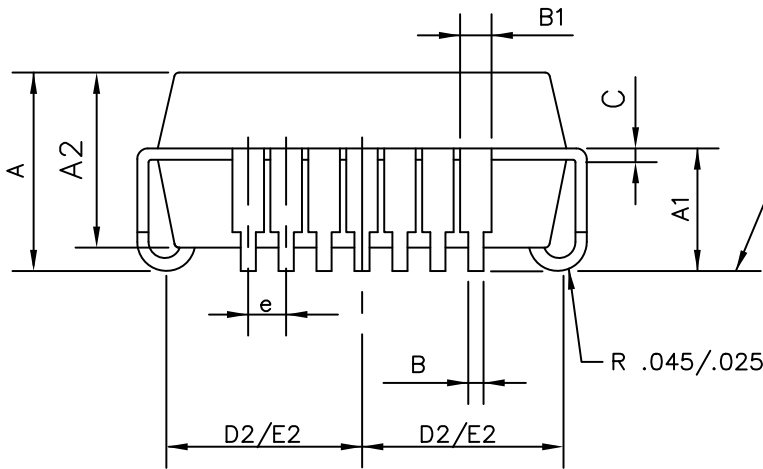
SIDE VIEW

| SYMBOL | MIN | NOM | MAX |
|--------|-------|-------|-------|
| A | 0.165 | 0.172 | 0.180 |
| A1 | 0.090 | 0.105 | 0.120 |
| A2 | 0.148 | 0.152 | 0.156 |
| B | 0.013 | 0.017 | 0.021 |
| B1 | 0.026 | 0.029 | 0.032 |
| C | 0.008 | 0.010 | 0.012 |
| D | 0.485 | 0.490 | 0.495 |
| D1 | 0.450 | 0.453 | 0.456 |
| D2 | 0.195 | 0.210 | 0.215 |
| E | 0.485 | 0.490 | 0.495 |
| E1 | 0.450 | 0.453 | 0.456 |
| E2 | 0.195 | 0.210 | 0.215 |
| e | 0.050 REF. | | |

ALL DIMENSIONS ARE IN INCHES.

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|---|---|---|---|
| DESCRIPTION: | PLCC 28 LEAD | | PAGE 1 OF 1 |

## PUBLICATION ORDERING INFORMATION

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