

SAMA7G5 System-In-Package (SIP) MPU with up to 1 Gbit, 2 Gbit or 4 Gbit DDR3L SDRAM

SAMA7G5 SIP



Scope

This document is an overview of the main features of the SAMA7G5 SIP microprocessor. The sole reference documents for product information on the SAMA7G5 and the DDR3L SDRAM memories are listed in [Reference Documents](#).

Introduction

The SAMA7G5 SIP integrates the Arm® Cortex®-A7 processor-based SAMA7G54 MPU with up to 4-Gbit DDR3L SDRAM. By combining the SAMA7G54 with a DDR3L SDRAM in a single package, PCB routing complexity, area and number of layers are reduced in the majority of cases. This makes board design easier and more robust by facilitating design for EMI, ESD and signal integrity.

The following DDR3L SDRAM memory densities are available:

- 1-Gbit DDR3L SDRAM
- 2-Gbit DDR3L SDRAM
- 4-Gbit DDR3L SDRAM

Reference Documents

Type	Name	Available	Ref. No.
Data sheet	SAMA7G5 Series	www.microchip.com	DS60001765
Application note	SAMA7G54 Hardware Design Considerations	www.microchip.com	DS00004598
Data sheet	1-Gbit 8M x 8 BANKS x 16 BIT DDR3L SDRAM	www.winbond.com	W631GU6NB
Data sheet	2-Gbit 16M x 8 BANKS x 16 BIT DDR3L SDRAM	www.winbond.com	W632GU6NG
Data sheet	4-Gbit 32M x 8 BANKS x 16 BIT DDR3L SDRAM	www.winbond.com	W634GU6NB

Features

- Arm Cortex-A7 Core
 - Arm TrustZone®
 - Arm® Neon™ multimedia architecture
 - Floating Point Unit
 - Embedded Trace module with instruction trace stream, including 16 Kbytes of CoreSight™ Embedded Trace buffer
 - 32 Kbytes of L1 data cache, 32 Kbytes of L1 instruction cache
 - 256 Kbytes of L2 cache
 - Up to 1 GHz operating frequency
 - Voltage and frequency scaling support
 - 64-bit generic timers
- Internal Memory Architecture

- 128 Kbytes of internal SRAM
- 80 Kbytes of maskable ROM, embedding a secure boot loader (boot on QSPI NOR, SLC NAND, SD, eMMC)
- 96 Kbytes ROM for NAND Flash ECC tables
- 40 Kbytes ROM for crypto-libraries (RSA, ECC, etc.)
- 11 Kbytes of internal OTP
- 16-bit high-bandwidth, DDR3L SDRAM up to 533 MHz, up to 4 Gbits
- External Memory Support
 - 16-bit static memory controller, FPGA support with synchronous clock
 - 8-bit SLC and MLC NAND controller with up to 32-bit error correcting code
 - One 8-bit high-speed memory card host eMMC 5.1 (HS400), SD3.0 SDR104 mode support
 - Two 4-bit high-speed memory card hosts eMMC 4.51 (HS200), SD3.01 SDR104 mode support
 - One octal Serial Peripheral Interface running up to 200 MHz DDR
 - One quad Serial Peripheral Interface
- System
 - Power-on reset cells, reset controller, shutdown controller, watchdog and secure watchdog timers running on internal slow RC oscillator (32 kHz typical) and real-time clock running on slow crystal oscillator (32.768 kHz)
 - Two internal trimmed RC oscillators with typical values: 32 kHz and 12 MHz
 - Two crystal oscillators: 32.768 kHz and 20 to 50 MHz
 - Eight PLLs for core, system bus and peripherals, serial interfaces, DDR I/Os, pixel clock, audio, USB, MIPI CSI-2 and Ethernet
 - Two 32-channel DMA with per-channel security configuration
 - One 8-channel DMA dedicated to memory-to-memory transactions
 - Eight programmable clock output signals
- Power Considerations
 - Different power domains and power modes to reduce power consumption
 - Low-power consumption in Backup mode with 5 Kbytes of secure backup SRAM and DDR-SDRAM in Self-Refresh mode
 - Low-power with SRAM and register retention, wake-up from various events (USB, CAN, Ethernet WOL, FLEXCOMs), internal events (RTC, timer) and I/O activity
 - Embedded LDOs for MIPI CSI-2, analog and PLLs, to enable low-cost power management solutions
 - Optimum connection to Microchip MCP16501/2 PMICs to enter and exit various power modes of the application
- Multimedia Peripherals
 - Audio
 - Two synchronous serial controllers, each with 16 channels of up to 32-bit TDM data
 - One inter-IC sound multi-channel controller with TDM256 support
 - Up to two 4-channel pulse density microphone controllers; support for eight microphones in parallel
 - One Sony/Philips digital interface transmitter and receiver
 - Audio sample rate converter including four stereo channels
 - Image

- Image sensor controller, ITU-R BT. 601/656 supporting up to eight megapixels for still images and 60 fps in 720p mode, 8 bits, raw Bayer, YCbCr, monochrome, camera ISP
- 2-lane MIPI CSI-2 (D-PHY) and 12-bit RGB interface support
- Peripherals
 - Two high-speed USB devices and three high-speed USB hosts sharing three on-chip transceivers
 - One 10/100/1000 Gigabit Ethernet MAC supporting RGMII, MII and RMII (GMAC0) and one 10/100 Ethernet MAC supporting MII and RMII (GMAC1) compliant with:
 - IEEE802.3az Energy-Efficient Ethernet
 - IEEE802.1AS Timestamping for Ethernet AVB support
 - IEEE802.1Qav Credit-based traffic shaping hardware support
 - IEEE1588 Precision Time Protocol
 - IEEE1588 Timestamp Unit (TSU) with TSU timer comparison signal triggering a timer counter and available on a PIO line
 - Six flexible data rate CAN-FD controllers with SRAM-based mailboxes with time- and event-triggered transmission
 - Twelve FLEXCOMs (USART, SPI and TWIHS)
 - Six 64-bit timers
 - Two three-channel 32-bit timer counters, with PWM generation
 - One four-channel 16-bit PWM controller
 - One 16-channel 12-bit analog-to-digital converter, up to 1 Msps
- Safety
 - Temperature and core voltage monitoring
 - Zero-power power-on reset cells
 - Main crystal monitor and clock failure detector with failsafe switchover to main RC oscillator
 - 32 kHz crystal monitor and clock failure detector with failsafe switchover to internal 32 kHz RC oscillator
 - Integrity check monitor based on SHA256
 - Safety critical modules (WDT, RSTC, SHDWC, etc.) running on always-on slow RC oscillator
 - Register write protection
- Security
 - TrustZone support
 - One Secure TrustZone watchdog timer running on RC oscillator, providing protection against TrustZone starvation
 - Temperature, voltage and frequency monitoring
 - Secure backup SRAM
 - 5 Kbytes scrambled with non-imprinting support powered with VBAT or VDDIN33:
 - 1 Kbyte non erasable on tamper detection
 - 4 Kbytes erasable on tamper detection
 - Four tamper pins for static or dynamic detection
 - Can be used as regular wake-up lines
 - 256-bit general purpose backup register, erasable on tamper detection
 - Programmable OTP with bits available for user purposes
 - Configurable JTAG security (full debug, non-secure-only debug, no debug)

- 128-bit AES on-the-fly encryption/decryption on DDR memory, SMC, QSPI0 and QSPI1, including automatic key load at start-up. Separate keys for secure and non-secure accesses (TZAESB).
- True random number generator compliant with NIST Special Publication 800-22 Tests Suite and FIPS PUB 140-2 and 140-3
- Secure RTC
- Cryptography
 - SHA (SHA1, SHA224, SHA256, SHA384, SHA512) compliant with FIPS Publications 180-2
 - AES: 256-, 192-, 128-bit key algorithm, compliant with FIPS PUB 197 specifications
 - TDES: two-key or three-key algorithms, compliant with FIPS PUB 46-3 specifications
 - Public Key Coprocessor (CPKCC) and associated Classical Public Key Cryptography Library (CPKCL) for RSA, DSA, ECC GF(2ⁿ), ECC GF_(p)⁽¹⁾
- Up to 136 I/Os
 - Fully programmable through set/clear registers
 - Multiplexing of eight peripheral functions per I/O line
 - Each I/O line can be assigned to a peripheral or used as a general purpose I/O
 - PIO controller featuring a synchronous output providing up to 32 bits of data output in a single write operation
- Design for Low ElectroMagnetic Interference (EMI)
 - Slewrate-controlled I/Os
 - DDR PHY with impedance-calibrated drivers
 - Spread spectrum PLLs
 - Careful BGA power/ground ball assignment to provide optimum decoupling capacitors placement
- Microchip Recommended Power Management Integrated Circuits (PMICs)
 - MCP16502, 6-channel PMIC with I²C control interface; supports dynamic voltage scaling and processor Low-Power modes (ULP2, BSR)
 - MCP16501, 4-channel PMIC optimized for compact PCB layout; supports processor Low-Power mode
- Operating Conditions
 - Junction temperature range (T_j): -40°C to +105°C
- Package
 - 427-ball TFBGA 18x21 mm², 0.8 mm pitch

Note:

1. CPKCC and CPKCL are described in the application note “Using CPKCL Version 02.08.01.xx on SAMA7G5” (Lit. No. DS00004438). This document is available under Non-Disclosure Agreement (NDA). Contact a Microchip Sales Representative for further details.

1. DDR3L SDRAM Features

The SAMA7G5 SIP is available with 1-Gbit, 2-Gbit or 4-Gbit DDR3L SDRAM memory options. For power consumption, electrical characteristics and timings of these memories, refer to the manufacturers' data sheets listed in [Reference Documents](#).

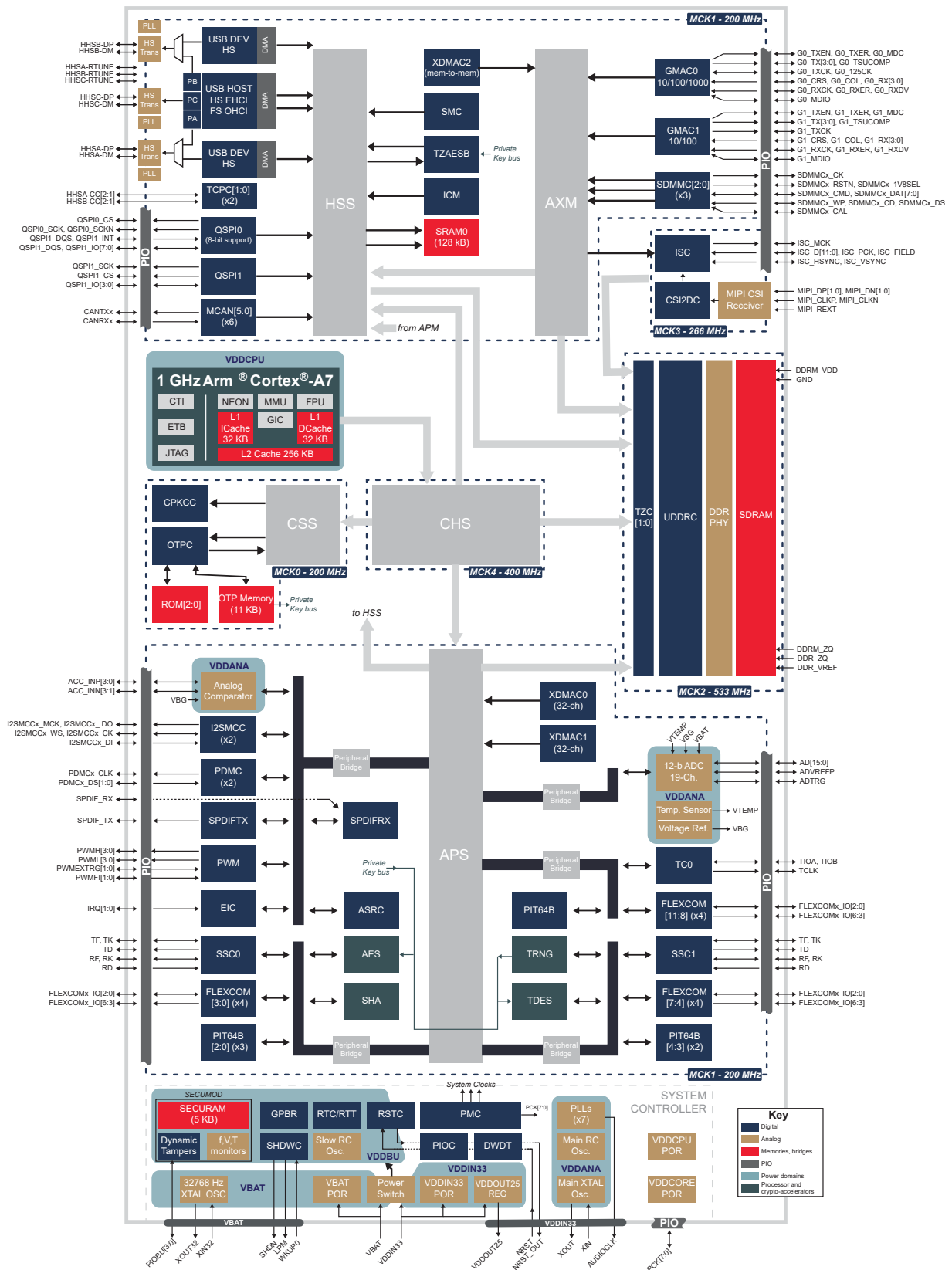
- Power supply: DDR3L DDRM_VDD = 1.283V to 1.45V
- 2-Kbyte page size (x16)
- 8-bank operation controlled by BA0, BA1 and BA2
- Burst lengths (BL): 8 and 4 with Burst Chop (BC)
- Precharge: auto-precharge option for each burst access
- Refresh: auto-refresh, self-refresh
- Average refresh period:
 - 7.8 μ s at $-40^{\circ}\text{C} \leq T_j \leq +85^{\circ}\text{C}$
 - 3.9 μ s at $+85^{\circ}\text{C} < T_j \leq +95^{\circ}\text{C}$
 - 1.95 μ s at $+95^{\circ}\text{C} < T_j \leq +105^{\circ}\text{C}$
- High-speed data transfer realized by the 8-bit prefetch pipelined architecture
- Double Data Rate architecture: two data transfers per clock cycle
- Bidirectional differential data strobe (DQS and /DQS) transmitted/received with data for capturing data at the receiver
- DQS edge-aligned with data for reads and center-aligned with data for writes
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted CAS by programmable additive latency for better command and data bus efficiency
- MultiPurpose Register (MPR) for predefined pattern read out
- ZQ calibration for DQ drive and ODT
- Programmable Partial Array Self-Refresh (PASR)
- Reset pin for power-up sequence and reset function
- Self-Refresh Temperature (SRT) range: normal/extended
- Automatic Self-Refresh (ASR)
- Programmable output driver impedance control

2. Configuration Summary

Feature	SAMA7G54D4G	SAMA7G54D2G	SAMA7G54D1G
Package	TFBGA427		
CPU	Cortex-A7		
CPU frequency	Up to 1 GHz		
External memory support	NAND Flash, QSPI (NAND, NOR)		
Number of PIOs	136		
SDMMC	3		
DDR datapath	16-bit, 533 MHz (internal)		
Internal SDRAM	4-Gbit DDR3L SDRAM	2-Gbit DDR3L SDRAM	1-Gbit DDR3L SDRAM
GMAC	RGMII/MII/RMII + MII/RMII		
CAN	6		
FLEXCOM	12		
ADC channels	16		
USB device/host	2/2 sharing 2 USB Type-C™ transceivers + 1 host		
I2SMCC channel outputs/inputs	8/8		
SSC	2		
ISC	MIPI + Parallel RGB		
PDMC channels	Up to 8 microphones		

3. Block Diagram

Figure 3-1. SAMA7G5 SIP Block Diagram



4. Chip Identifier

Table 4-1. Chip ID and Extended ID Definition

Chip Name	CHIPID_CIDR	CHIPID_EXID
SAMA7G54D1G	0x80162111	0x00000018
SAMA7G54D2G		0x00000020
SAMA7G54D4G		0x00000028

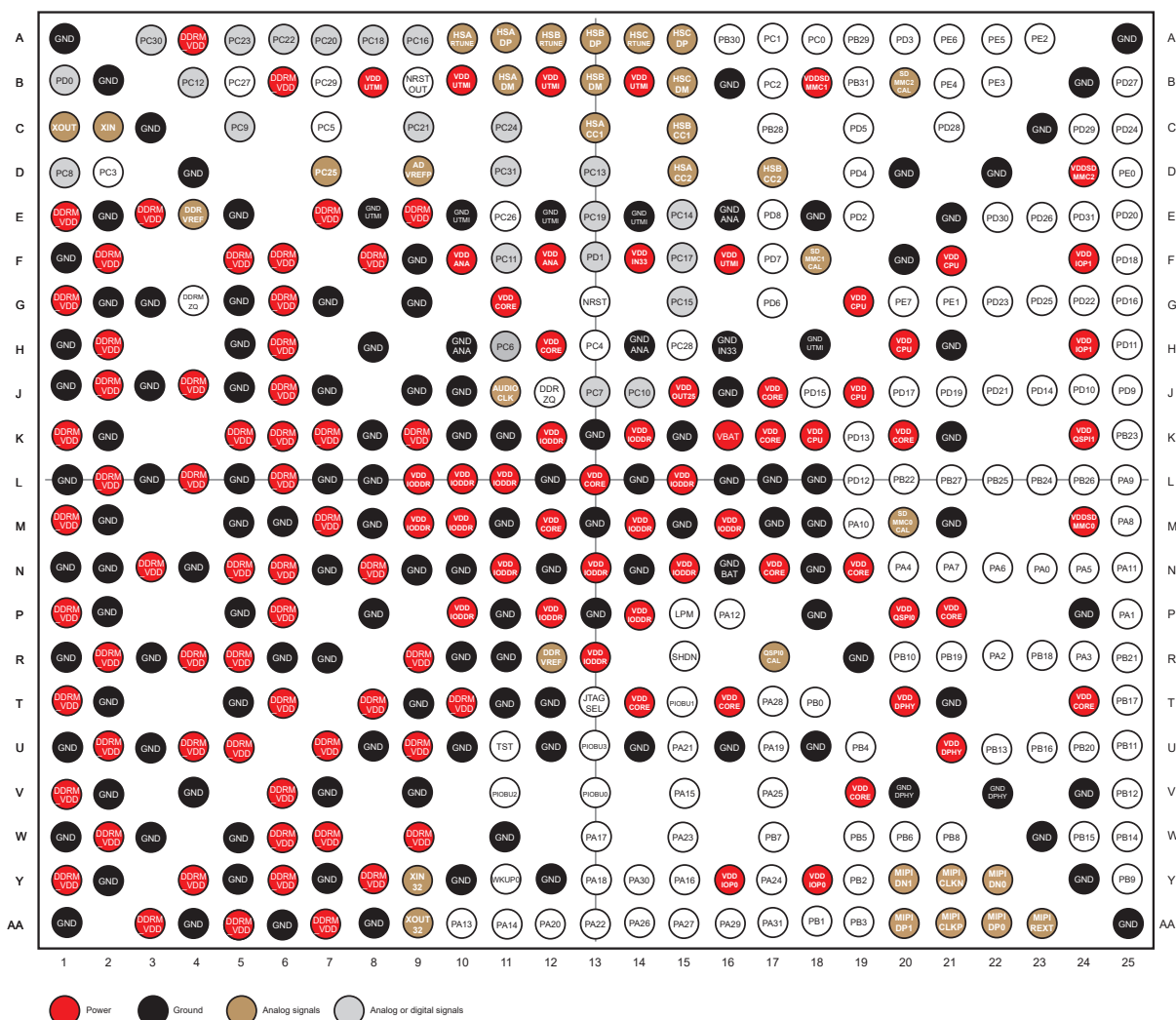
5. Package and Ballout

The 1-Gbit, 2-Gbit and 4-Gbit SAMA7G5 SIP devices are pin-to-pin compatible.

Package Name	Ball Count	Ball Pitch	Package Size
TFBGA427	427	0.8 mm	21 x 18 (mm)

5.1 TFBGA427 Package

Figure 5-1. 427-Ball TFBGA Pinout



5.2 Ball Description

 Table 5-1. Ball Description⁽¹⁾

TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
N23	VDDSDMMC0	HSIO	PA0	I/O	-	-	A	SDMMC0_CK	I/O	1	PIO, I, PU, ST
							B	FLEXCOM0_IO0	I/O	1	
							C	CANTX3	O	1	
							E	PWML0	O	3	
P25	VDDSDMMC0	HSIO	PA1	I/O	-	-	A	SDMMC0_CMD	I/O	1	PIO, I, PU, ST
							B	FLEXCOM0_IO1	I/O	1	
							C	CANRX3	I	1	
							D	D14	I/O	1,2	
							E	PWMH0	O	3	
R22	VDDSDMMC0	GPIO	PA2	I/O	-	-	A	SDMMC0_RSTN	O	1	PIO, I, PU, ST
							B	FLEXCOM0_IO2	I/O	1	
							C	PDMC1_CLK	O	1	
							D	D15	I/O	1,2	
							E	PWMH1	O	3	
							F	FLEXCOM1_IO0	I/O	3	
R24	VDDSDMMC0	HSIO	PA3	I/O	-	-	A	SDMMC0_DAT0	I/O	1	PIO, I, PU, ST
							B	FLEXCOM0_IO3	I/O	1	
							C	PDMC1_DS0	I	1	
							D	NWR1/NBS1	O	1,2	
							E	PWML3	O	3	
							F	FLEXCOM1_IO1	I/O	3	
N20	VDDSDMMC0	HSIO	PA4	I/O	-	-	A	SDMMC0_DAT1	I/O	1	PIO, I, PU, ST
							B	FLEXCOM0_IO4	I/O	1	
							C	PDMC1_DS1	I	1	
							D	NCS2	O	1,2	
							E	PWMH3	O	3	
							F	FLEXCOM2_IO0	I/O	3	

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
N24	VDDSDMMC0	HSIO	PA5	I/O	-	-	A	SDMMC0_DAT2	I/O	1	PIO, I, PU, ST
							B	FLEXCOM1_IO0	I/O	1	
							C	CANTX2	O	1	
							D	A23	O	1,2	
							E	PWMEXTRG0	I	3	
							F	FLEXCOM2_IO1	I/O	3	
N22	VDDSDMMC0	HSIO	PA6	I/O	-	-	A	SDMMC0_DAT3	I/O	1	PIO, I, PU, ST
							B	FLEXCOM1_IO1	I/O	1	
							C	CANRX2	I	1	
							D	A24	O	1,2	
							E	PWMEXTRG1	I	3	
							F	FLEXCOM3_IO0	I/O	3	
N21	VDDSDMMC0	HSIO	PA7	I/O	-	-	A	SDMMC0_DAT4	I/O	1	PIO, I, PU, ST
							B	FLEXCOM2_IO0	I/O	1	
							C	CANTX1	O	1	
							D	NWAIT	I	1,2	
							E	PWMFI0	I	3	
							F	FLEXCOM3_IO1	I/O	3	
M25	VDDSDMMC0	HSIO	PA8	I/O	-	-	A	SDMMC0_DAT5	I/O	1	PIO, I, PU, ST
							B	FLEXCOM2_IO1	I/O	1	
							C	CANRX1	I	1	
							D	NCS0	O	1,2	
							E	PWMFI1	I	3	
							F	FLEXCOM4_IO0	I/O	3	
L25	VDDSDMMC0	HSIO	PA9	I/O	-	-	A	SDMMC0_DAT6	I/O	1	PIO, I, PU, ST
							B	FLEXCOM2_IO2	I/O	1	
							C	CANTX0	O	1	
							D	SMCK	O	1,2	
							E	SPDIF_RX	I	1	
							F	FLEXCOM4_IO1	I/O	3	

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
M19	VDDSDMMC0	HSIO	PA10	I/O	-	-	A	SDMMC0_DAT7	I/O	1	PIO, I, PU, ST
							B	FLEXCOM2_IO3	I/O	1	
							C	CANRX0	I	1	
							D	NCS1	O	1,2	
							E	SPDIF_TX	O	1	
							F	FLEXCOM5_IO0	I/O	3	
N25	VDDSDMMC0	HSIO	PA11	I/O	-	-	A	SDMMC0_DS	I	1	PIO, I, PU, ST
							B	FLEXCOM2_IO4	I/O	1	
							D	A0/NBS0	O	1,2	
							E	TIOA0	I/O	1	
							F	FLEXCOM5_IO1	I/O	3	
P16	VDDIOP0	GPIO	PA12	I/O	-	-	A	SDMMC0_WP	I	1	PIO, I, PU, ST
							B	FLEXCOM1_IO3	I/O	1	
							D	FLEXCOM3_IO5	I/O	1	
							E	PWML2	O	3	
							F	FLEXCOM6_IO0	I/O	3	
AA10	VDDIOP0	GPIO	PA13	I/O	-	-	A	SDMMC0_1V8SEL	O	1	PIO, I, PU, ST
							B	FLEXCOM1_IO2	I/O	1	
							D	FLEXCOM3_IO6	I/O	1	
							E	PWMH2	O	3	
							F	FLEXCOM6_IO1	I/O	3	
AA11	VDDIOP0	GPIO	PA14	I/O			A	SDMMC0_CD	I	1	PIO, I, PU, ST
							B	FLEXCOM1_IO4	I/O	1	
							D	A25	O	1,2	
							E	PWML1	O	3	
V15	VDDIOP0	GPIO	PA15	I/O	-	-	A	G0_TXEN	O	1	PIO, I, PU, ST
							B	FLEXCOM3_IO0	I/O	1	
							C	ISC_MCK	O	1	
							D	A1	O	1,2	
							E	TIOB0	I/O	1	

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
Y15	VDDIOP0	GPIO	PA16	I/O	-	-	A	G0_TX0	O	1	PIO, I, PU, ST
							B	FLEXCOM3_IO1	I/O	1	
							C	ISC_D0	I	1	
							D	A2	O	1,2	
							E	TCLK0	I	1	
W13	VDDIOP0	GPIO	PA17	I/O	-	-	A	G0_TX1	O	1	PIO, I, PU, ST
							B	FLEXCOM3_IO2	I/O	1	
							C	ISC_D1	I	1	
							D	A3	O	1,2	
							E	TIOA1	I/O	1	
Y13	VDDIOP0	GPIO	PA18	I/O	-	-	A	G0_RXDV	I	1	PIO, I, PU, ST
							B	FLEXCOM3_IO3	I/O	1	
							C	ISC_D2	I	1	
							D	A4	O	1,2	
							E	TIOB1	I/O	1	
U17	VDDIOP0	GPIO	PA19	I/O	-	-	A	G0_RX0	I	1	PIO, I, PU, ST
							B	FLEXCOM3_IO4	I/O	1	
							C	ISC_D3	I	1	
							D	A5	O	1,2	
							E	TCLK1	I	1	
AA12	VDDIOP0	GPIO	PA20	I/O	-	-	A	G0_RX1	I	1	PIO, I, PU, ST
							B	FLEXCOM4_IO0	I/O	1	
							C	ISC_D4	I	1	
							D	A6	O	1,2	
							E	TIOA2	I/O	1	
U15	VDDIOP0	GPIO	PA21	I/O	-	-	A	G0_RXER	I	1	PIO, I, PU, ST
							B	FLEXCOM4_IO1	I/O	1	
							C	ISC_D5	I	1	
							D	A7	O	1,2	
							E	TIOB2	I/O	1	

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
AA13	VDDIOP0	GPIO	PA22	I/O	-	-	A	G0_MDC	O	1	PIO, I, PU, ST
							B	FLEXCOM4_IO2	I/O	1	
							C	ISC_D6	I	1	
							D	A8	O	1,2	
							E	TCLK2	I	1	
W15	VDDIOP0	GPIO	PA23	I/O	-	-	A	G0_MDIO	I/O	1	PIO, I, PU, ST
							B	FLEXCOM4_IO3	I/O	1	
							C	ISC_D7	I	1	
							D	A9	O	1,2	
Y17	VDDIOP0	GPIO	PA24	I/O	-	-	A	G0_TXCK	I/O	1	PIO, I, PU, ST
							B	FLEXCOM4_IO4	I/O	1	
							C	ISC_HSYNC	I	1	
							D	A10	O	1,2	
							E	FLEXCOM0_IO5	I/O	1	
V17	VDDIOP0	GPIO	PA25	I/O	-	-	A	G0_125CK	I/O	1	PIO, I, PU, ST
							B	FLEXCOM5_IO4	I/O	1	
							C	ISC_VSYNC	I	1	
							D	A11	O	1,2	
							E	FLEXCOM0_IO6	I/O	1	
							F	FLEXCOM7_IO0	I/O	3	
AA14	VDDIOP0	GPIO	PA26	I/O	-	-	A	G0_TX2	O	1	PIO, I, PU, ST
							B	FLEXCOM5_IO2	I/O	1	
							C	ISC_FIELD	I	1	
							D	A12	O	1,2	
							E	TF0	I/O	1	
							F	FLEXCOM7_IO1	I/O	3	

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
AA15	VDDIOP0	GPIO	PA27	I/O	-	-	A	G0_TX3	O	1	PIO, I, PU, ST
							B	FLEXCOM5_IO3	I/O	1	
							C	ISC_PCK	I	1	
							D	A13	O	1,2	
							E	TK0	I/O	1	
							F	FLEXCOM8_IO0	I/O	3	
T17	VDDIOP0	GPIO	PA28	I/O	-	-	A	G0_RX2	I	1	PIO, I, PU, ST
							B	FLEXCOM5_IO0	I/O	1	
							C	ISC_D8	I	1	
							D	A14	O	1,2	
							E	RD0	I	1	
							F	FLEXCOM8_IO1	I/O	3	
AA16	VDDIOP0	GPIO	PA29	I/O	-	-	A	G0_RX3	I	1	PIO, I, PU, ST
							B	FLEXCOM5_IO1	I/O	1	
							C	ISC_D9	I	1	
							D	A15	O	1,2	
							E	RF0	I/O	1	
							F	FLEXCOM9_IO0	I/O	3	
Y14	VDDIOP0	GPIO	PA30	I/O	-	-	A	G0_RXCK	I	1	PIO, I, PU, ST
							B	FLEXCOM6_IO4	I/O	1	
							C	ISC_D10	I	1	
							D	A16	O	1,2	
							E	RK0	I/O	1	
							F	FLEXCOM9_IO1	I/O	3	
AA17	VDDIOP0	GPIO	PA31	I/O	-	-	A	G0_TXER	O	1	PIO, I, PU, ST
							B	FLEXCOM6_IO2	I/O	1	
							C	ISC_D11	I	1	
							D	A17	O	1,2	
							E	TD0	O	1	
							F	FLEXCOM10_IO0	I/O	3	

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
T18	VDDIOP0	GPIO	PB0	I/O	-	-	A	G0_COL	I	1	PIO, I, PU, ST
							B	FLEXCOM6_IO3	I/O	1	
							C	EXT_IRQ0	I	1	
							D	A18	O	1,2	
							E	SPDIF_RX	I	2	
							F	FLEXCOM10_IO1	I/O	3	
AA18	VDDIOP0	GPIO	PB1	I/O	-	-	A	G0_CRS	I	1	PIO, I, PU, ST
							B	FLEXCOM6_IO1	I/O	1	
							C	EXT_IRQ1	I	1	
							D	A19	O	1,2	
							E	SPDIF_TX	O	2	
							F	FLEXCOM11_IO0	I/O	3	
Y19	VDDIOP0	GPIO	PB2	I/O	-	-	A	G0_TSUCOMP	O	1	PIO, I, PU, ST
							B	FLEXCOM6_IO0	I/O	1	
							C	ADTRG	I	1	
							D	A20	O	1,2	
							F	FLEXCOM11_IO1	I/O	3	
AA19	VDDIOP0	GPIO	PB3	I/O	-	-	A	RF1	I/O	1	PIO, I, PU, ST
							B	FLEXCOM11_IO0	I/O	1	
							C	PCK2	O	2	
							D	D8	I/O	1,2	
U19	VDDIOP0	GPIO	PB4	I/O	-	-	A	TF1	I/O	1	PIO, I, PU, ST
							B	FLEXCOM11_IO1	I/O	1	
							C	PCK3	O	2	
							D	D9	I/O	1,2	
W19	VDDIOP0	GPIO	PB5	I/O	-	-	A	TK1	I/O	1	PIO, I, PU, ST
							B	FLEXCOM11_IO2	I/O	1,2,3,4,5	
							C	PCK4	O	2	
							D	D10	I/O	1,2	

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
W20	VDDIOP0	GPIO	PB6	I/O	-	-	A	RK1	I/O	1	PIO, I, PU, ST
							B	FLEXCOM11_IO3	I/O	1,2,3,4,5	
							C	PCK5	O	2	
							D	D11	I/O	1,2	
W17	VDDIOP0	GPIO	PB7	I/O	-	-	A	TD1	O	1	PIO, I, PU, ST
							B	FLEXCOM11_IO4	I/O	1,2,3,4,5	
							C	FLEXCOM3_IO5	I/O	2,3,4,5	
							D	D12	I/O	1,2	
W21	VDDIOP0	GPIO	PB8	I/O	-	-	A	RD1	I	1	PIO, I, PU, ST
							B	FLEXCOM8_IO0	I/O	1	
							C	FLEXCOM3_IO6	I/O	2,3,4,5	
							D	D13	I/O	1,2	
Y25	VDDQSPI0	HSIO	PB9	I/O	-	-	A	QSPI0_IO3	I/O	1	PIO, I, PU, ST
							B	FLEXCOM8_IO1	I/O	1	
							C	PDMC0_CLK	O	1	
							D	NCS3/NANDCS	O	1	
							E	PWML0	O	2	
R20	VDDQSPI0	HSIO	PB10	I/O	-	-	A	QSPI0_IO2	I/O	1	PIO, I, PU, ST
							B	FLEXCOM8_IO2	I/O	1	
							C	PDMC0_DS0	I	1	
							D	NWE/NWR0/NANDWE	O	1	
							E	PWMH0	O	2	
U25	VDDQSPI0	HSIO	PB11	I/O	-	-	A	QSPI0_IO1	I/O	1	PIO, I, PU, ST
							B	FLEXCOM8_IO3	I/O	1	
							C	PDMC0_DS1	I	1	
							D	NRD/NANDOE	O	1	
							E	PWML1	O	2	

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
V25	VDDQSPI0	HSIO	PB12	I/O	-	-	A	QSPI0_IO0	I/O	1	PIO, I, PU, ST
							B	FLEXCOM8_IO4	I/O	1	
							C	FLEXCOM6_IO5	I/O	1	
							D	A21/NANDALE	O	1	
							E	PWMH1	O	2	
U22	VDDQSPI0	GPIO	PB13	I/O	-	-	A	QSPI0_CS	O	1	PIO, I, PU, ST
							B	FLEXCOM9_IO0	I/O	1	
							C	FLEXCOM6_IO6	I/O	1	
							D	A22/NANDCLE	O	1	
							E	PWML2	O	2	
W25	VDDQSPI0	HSIO	PB14	I/O	-	-	A	QSPI0_SCK	I/O	1	PIO, I, PU, ST
							B	FLEXCOM9_IO1	I/O	1	
							D	D0	I/O	1	
							E	PWMH2	O	2	
W24	VDDQSPI0	HSIO	PB15	I/O	-	-	A	QSPI0_SCKN	I/O	1	PIO, I, PU, ST
							B	FLEXCOM9_IO2	I/O	1	
							D	D1	I/O	1	
							E	PWML3	O	2	
U23	VDDQSPI0	HSIO	PB16	I/O	-	-	A	QSPI0_IO4	I/O	1	PIO, I, PU, ST
							B	FLEXCOM9_IO3	I/O	1	
							C	PCK0	O	1	
							D	D2	I/O	1	
							E	PWMH3	O	2	
							F	EXT_IRQ0	I	2	
T25	VDDQSPI0	HSIO	PB17	I/O	-	-	A	QSPI0_IO5	I/O	1	PIO, I, PU, ST
							B	FLEXCOM9_IO4	I/O	1	
							C	PCK1	O	1	
							D	D3	I/O	1	
							E	PWMEXTRG0	I	2	
							F	EXT_IRQ1	I	2	

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
R23	VDDQSPI0	HSIO	PB18	I/O	-	-	A	QSPI0_IO6	I/O	1	PIO, I, PU, ST
							B	FLEXCOM10_IO0	I/O	1	
							C	PCK2	O	1	
							D	D4	I/O	1	
							E	PWMEXTRG1	I	2	
R21	VDDQSPI0	HSIO	PB19	I/O	-	-	A	QSPI0_IO7	I/O	1	PIO, I, PU, ST
							B	FLEXCOM10_IO1	I/O	1	
							C	PCK3	O	1	
							D	D5	I/O	1	
							E	PWMFI0	I	2	
U24	VDDQSPI0	HSIO	PB20	I/O	-	-	A	QSPI0_DQS	I	1	PIO, I, PU, ST
							B	FLEXCOM10_IO2	I/O	1,2,3,4,5	
							D	D6	I/O	1	
							E	PWMFI1	I	2	
R25	VDDQSPI0	GPIO	PB21	I/O	-	-	A	QSPI0_INT	I	1	PIO, I, PU, ST
							B	FLEXCOM10_IO3	I/O	1,2,3,4,5	
							C	FLEXCOM9_IO5	I/O	1	
							D	D7	I/O	1	
L20	VDDQSPI1	GPIO	PB22	I/O	-	-	A	QSPI1_IO3	I/O	1	PIO, I, PU, ST
							B	FLEXCOM10_IO4	I/O	1,2,3,4,5	
							C	FLEXCOM9_IO6	I/O	1	
							D	NANDRDY	I	1	
K25	VDDQSPI1	GPIO	PB23	I/O	-	-	A	QSPI1_IO2	I/O	1	PIO, I, PU, ST
							B	FLEXCOM7_IO0	I/O	1	
							C	I2SMCC0_CK	I/O	1	
							F	PCK4	O	1	
L23	VDDQSPI1	GPIO	PB24	I/O	-	-	A	QSPI1_IO1	I/O	1	PIO, I, PU, ST
							B	FLEXCOM7_IO1	I/O	1	
							C	I2SMCC0_WS	I/O	1	
							F	PCK5	O	1	

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
L22	VDDQSPI1	GPIO	PB25	I/O	-	-	A	QSPI1_IO0	I/O	1	PIO, I, PU, ST
							B	FLEXCOM7_IO2	I/O	1	
							C	I2SMCC0_DOUT1	O	1	
							F	PCK6	O	1	
L24	VDDQSPI1	GPIO	PB26	I/O	-	-	A	QSPI1_CS	O	1	PIO, I, PU, ST
							B	FLEXCOM7_IO3	I/O	1	
							C	I2SMCC0_DOUT0	O	1	
							E	PWMEXTRG0	I	1	
							F	PCK7	O	1	
L21	VDDQSPI1	GPIO	PB27	I/O	-	-	A	QSPI1_SCK	I/O	1	PIO, I, PU, ST
							B	FLEXCOM7_IO4	I/O	1	
							C	I2SMCC0_MCK	O	1	
							E	PWMEXTRG1	I	1	
C17	VDDSDMMC1	GPIO	PB28	I/O	-	-	A	SDMMC1_RSTN	O	1	PIO, I, PU, ST
							B	ADTRG	I	2	
							E	PWMFI0	I	1	
							F	FLEXCOM7_IO0	I/O	4	
A19	VDDSDMMC1	HSIO	PB29	I/O	-	-	A	SDMMC1_CMD	I/O	1	PIO, I, PU, ST
							B	FLEXCOM3_IO2	I/O	2,3,4,5	
							C	FLEXCOM0_IO5	I/O	2	
							D	TIOA3	I/O	1	
							E	PWMFI1	I	1	
							F	FLEXCOM7_IO1	I/O	4	
A16	VDDSDMMC1	HSIO	PB30	I/O	-	-	A	SDMMC1_CK	I/O	1	PIO, I, PU, ST
							B	FLEXCOM3_IO3	I/O	2,3,4,5	
							C	FLEXCOM0_IO6	I/O	2	
							D	TIOB3	I/O	1	
							E	PWMH0	O	1	
							F	FLEXCOM8_IO0	I/O	4	

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
B19	VDDSDMMC1	HSIO	PB31	I/O	-	-	A	SDMMC1_DAT0	I/O	1	PIO, I, PU, ST
							B	FLEXCOM3_IO4	I/O	2,3,4,5	
							C	FLEXCOM9_IO5	I/O	2,3,4,5	
							D	TCLK3	I	1	
							E	PWML0	O	1	
							F	FLEXCOM8_IO1	I/O	4	
A18	VDDSDMMC1	HSIO	PC0	I/O	-	-	A	SDMMC1_DAT1	I/O	1	PIO, I, PU, ST
							B	FLEXCOM3_IO0	I/O	2	
							D	TIOA4	I/O	1	
							E	PWML1	O	1	
							F	FLEXCOM9_IO0	I/O	4	
A17	VDDSDMMC1	HSIO	PC1	I/O	-	-	A	SDMMC1_DAT2	I/O	1	PIO, I, PU, ST
							B	FLEXCOM3_IO1	I/O	2	
							D	TIOB4	I/O	1	
							E	PWMH1	O	1	
							F	FLEXCOM9_IO1	I/O	4	
B17	VDDSDMMC1	HSIO	PC2	I/O	-	-	A	SDMMC1_DAT3	I/O	1	PIO, I, PU, ST
							B	FLEXCOM4_IO0	I/O	2	
							D	TCLK4	I	1	
							E	PWML2	O	1	
							F	FLEXCOM10_IO0	I/O	4	
D2	VDDIN33	GPIO	PC3	I/O	-	-	A	SDMMC1_WP	I	1	PIO, I, PU, ST
							B	FLEXCOM4_IO1	I/O	2	
							D	TIOA5	I/O	1	
							E	PWMH2	O	1	
							F	FLEXCOM10_IO1	I/O	4	

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TFBGA427	Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
				Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
H13	VDDIN33	GPIO	PC4	I/O	-	-		A	SDMMC1_CD	I	1	PIO, I, PU, ST
								B	FLEXCOM4_IO2	I/O	2,3,4,5	
								C	FLEXCOM9_IO6	I/O	2,3,4,5	
								D	TIOB5	I/O	1	
								E	PWML3	O	1	
								F	FLEXCOM11_IO0	I/O	4	
C7	VDDIN33	GPIO	PC5	I/O	-	-		A	SDMMC1_1V8SEL	O	1	PIO, I, PU, ST
								B	FLEXCOM4_IO3	I/O	2,3,4,5	
								C	FLEXCOM6_IO5	I/O	2,3,4,5	
								D	TCLK5	I	1	
								E	PWMH3	O	1	
								F	FLEXCOM11_IO1	I/O	4	
H11	VDDIN33	GPIO	PC6	I/O	ACC_INP0	-		A	-	-	-	PIO, I, PU, ST
								B	FLEXCOM4_IO4	I/O	2,3,4,5	
								C	FLEXCOM6_IO6	I/O	2,3,4,5	
J13	VDDIN33	GPIO	PC7	I/O	ACC_INN1	-		A	I2SMCC0_DIN0	I	1	PIO, I, PU, ST
								B	FLEXCOM7_IO0	I/O	2	
D1	VDDIN33	GPIO	PC8	I/O	ACC_INP1	-		A	I2SMCC0_DIN1	I	1	PIO, I, PU, ST
								B	FLEXCOM7_IO1	I/O	2	
C5	VDDIN33	GPIO	PC9	I/O	ACC_INN2	-		A	I2SMCC0_DOUT3	O	1	PIO, I, PU, ST
								B	FLEXCOM7_IO2	I/O	2,3,4,5	
								F	FLEXCOM1_IO0	I/O	4	
J14	VDDIN33	GPIO	PC10	I/O	ACC_INP2	-		A	I2SMCC0_DOUT2	O	1	PIO, I, PU, ST
								B	FLEXCOM7_IO3	I/O	2,3,4,5	
								F	FLEXCOM1_IO1	I/O	4	
F11	VDDIN33	GPIO	PC11	I/O	ACC_INN3	-		A	I2SMCC1_CK	I/O	1	PIO, I, PU, ST
								B	FLEXCOM7_IO4	I/O	2,3,4,5	
								F	FLEXCOM2_IO0	I/O	4	
B4	VDDIN33	GPIO	PC12	I/O	ACC_INP3	-		A	I2SMCC1_WS	I/O	1	PIO, I, PU, ST
								B	FLEXCOM8_IO2	I/O	2,3,4,5	
								F	FLEXCOM2_IO1	I/O	4	

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
D13	VDDIN33	GPIO	PC13	I/O	AD0	-	A	I2SMCC1_MCK	O	1	PIO, I, PU, ST
							B	FLEXCOM8_IO1	I/O	2	
							F	FLEXCOM3_IO0	I/O	4	
E15	VDDIN33	GPIO	PC14	I/O	AD1	-	A	I2SMCC1_DOUT0	O	1	PIO, I, PU, ST
							B	FLEXCOM8_IO0	I/O	2	
							F	FLEXCOM3_IO1	I/O	4	
G15	VDDIN33	GPIO	PC15	I/O	AD2	-	A	I2SMCC1_DOUT1	O	1	PIO, I, PU, ST
							B	FLEXCOM8_IO3	I/O	2,3,4,5	
							F	FLEXCOM4_IO0	I/O	4	
A9	VDDIN33	GPIO	PC16	I/O	AD3	-	A	I2SMCC1_DOUT2	O	1	PIO, I, PU, ST
							B	FLEXCOM8_IO4	I/O	2,3,4,5	
							F	FLEXCOM4_IO1	I/O	4	
F15	VDDIN33	GPIO	PC17	I/O	AD4	-	A	I2SMCC1_DOUT3	O	1	PIO, I, PU, ST
							B	EXT_IRQ0	I	3	
							F	FLEXCOM5_IO0	I/O	4	
A8	VDDIN33	GPIO	PC18	I/O	AD5	-	A	I2SMCC1_DIN0	I	1	PIO, I, PU, ST
							B	FLEXCOM9_IO0	I/O	2	
							F	FLEXCOM5_IO1	I/O	4	
E13	VDDIN33	GPIO	PC19	I/O	AD6	-	A	I2SMCC1_DIN1	I	1	PIO, I, PU, ST
							B	FLEXCOM9_IO1	I/O	2	
							F	FLEXCOM6_IO0	I/O	4	
A7	VDDIN33	GPIO	PC20	I/O	AD7	-	A	I2SMCC1_DIN2	I	1	PIO, I, PU, ST
							B	FLEXCOM9_IO4	I/O	2,3,4,5	
							F	FLEXCOM6_IO1	I/O	4	
C9	VDDIN33	GPIO	PC21	I/O	AD8	-	A	I2SMCC1_DIN3	I	1	PIO, I, PU, ST
							B	FLEXCOM9_IO2	I/O	2,3,4,5	
							D	D3	I/O	2	
							F	FLEXCOM6_IO0	I/O	5	

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
A6	VDDIN33	GPIO	PC22	I/O	AD9	-	A	I2SMCC0_DIN2	I	1	PIO, I, PU, ST
							B	FLEXCOM9_IO3	I/O	2,3,4,5	
							D	D4	I/O	2	
							F	FLEXCOM6_IO1	I/O	5	
A5	VDDIN33	GPIO	PC23	I/O	AD10	-	A	I2SMCC0_DIN3	I	1	PIO, I, PU, ST
							B	FLEXCOM0_IO5	I/O	3	
							D	D5	I/O	2	
							F	FLEXCOM7_IO0	I/O	5	
C11	VDDIN33	GPIO	PC24	I/O	AD11	-	A	-	-	-	PIO, I, PU, ST
							B	FLEXCOM0_IO6	I/O	3	
							C	EXT_IRQ1	I	3	
							D	D6	I/O	2	
							F	FLEXCOM7_IO1	I/O	5	
D7	VDDIN33	GPIO	PC25	I/O	-	-	A	NTRST	I	1	NTRST, PU, ST
E11	VDDIN33	GPIO	PC26	I/O	-	-	A	TCK_SWCLK	I	1	TCK_SWCLK, ST
B5	VDDIN33	GPIO	PC27	I/O	-	-	A	TMS_SWDIO	I/O	1	TMS_SWDIO, PU, ST
H15	VDDIN33	GPIO	PC28	I/O	-	-	A	TDI	I	1	TDI, PU, ST
B7	VDDIN33	GPIO	PC29	I/O	-	-	A	TDO	O	1	TDO, ST
A3	VDDIN33	GPIO	PC30	I/O	AD12	-	A	-	-	-	PIO, I, PD, ST
							B	FLEXCOM10_IO0	I/O	2	
D11	VDDIN33	GPIO	PC31	I/O	AD13	-	A	-	-	-	PIO, I, PD, ST
							B	FLEXCOM10_IO1	I/O	2	
B1	VDDIN33	GPIO	PD0	I/O	AD14	-	A	-	-	-	PIO, I, PD, ST
							B	FLEXCOM11_IO0	I/O	2	
F13	VDDIN33	GPIO	PD1	I/O	AD15	-	A	-	-	-	PIO, I, PD, ST
							B	FLEXCOM11_IO1	I/O	2	

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
E19	VDDSDMMC2	GPIO	PD2	I/O	-	-	A	SDMMC2_RSTN	O	1	PIO, I, PU, ST
							B	PCK0	O	2	
							C	CANTX4	O	1	
							D	D7	I/O	2	
							E	TIOA0	I/O	2	
							F	FLEXCOM8_IO0	I/O	5	
A20	VDDSDMMC2	HSIO	PD3	I/O	-	-	A	SDMMC2_CMD	I/O	1	PIO, I, PU, ST
							B	FLEXCOM0_IO0	I/O	2	
							C	CANRX4	I	1	
							D	NANDRDY	I	2	
							E	TIOB0	I/O	2	
							F	FLEXCOM8_IO1	I/O	5	
D19	VDDSDMMC2	HSIO	PD4	I/O	-	-	A	SDMMC2_CK	I/O	1	PIO, I, PU, ST
							B	FLEXCOM0_IO1	I/O	2	
							C	CANTX5	O	1	
							D	NCS3/NANDCS	O	2	
							E	TCLK0	I	2	
							F	FLEXCOM9_IO0	I/O	5	
C19	VDDSDMMC2	HSIO	PD5	I/O	-	-	A	SDMMC2_DAT0	I/O	1	PIO, I, PU, ST
							B	FLEXCOM0_IO2	I/O	2,3	
							C	CANRX5	I	1	
							D	NWE/NWR0/NANDWE	O	2	
							E	TIOA1	I/O	2	
							F	FLEXCOM9_IO1	I/O	5	
G17	VDDSDMMC2	HSIO	PD6	I/O	-	-	A	SDMMC2_DAT1	I/O	1	PIO, I, PU, ST
							B	FLEXCOM0_IO3	I/O	2,3	
							C	SPDIF_RX	I	3	
							D	NRD/NANDOE	O	2	
							E	TIOB1	I/O	2	
							F	FLEXCOM10_IO0	I/O	5	

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
F17	VDDSDMMC2	HSIO	PD7	I/O	-	-	A	SDMMC2_DAT2	I/O	1	PIO, I, PU, ST
							B	FLEXCOM0_IO4	I/O	2,3	
							C	SPDIF_TX	O	3	
							D	A21/NANDALE	O	2	
							E	TCLK1	I	2	
							F	FLEXCOM10_IO1	I/O	5	
E17	VDDSDMMC2	HSIO	PD8	I/O	-	-	A	SDMMC2_DAT3	I/O	1	PIO, I, PU, ST
							C	I2SMCC0_DIN0	I	2	
							D	A22/NANDCLE	O	2	
							E	TIOA2	I/O	2	
							F	FLEXCOM11_IO0	I/O	5	
J25	VDDIOP1	GPIO	PD9	I/O	-	-	A	SDMMC2_WP	I	1	PIO, I, PU, ST
							C	I2SMCC0_DIN1	I	2	
							D	D0	I/O	2	
							E	TIOB2	I/O	2	
							F	FLEXCOM11_IO1	I/O	5	
J24	VDDIOP1	GPIO	PD10	I/O	-	-	A	SDMMC2_CD	I	1	PIO, I, PU, ST
							B	PCK6	O	2	
							C	I2SMCC0_DIN2	I	2	
							D	D1	I/O	2	
							E	TCLK2	I	2	
							F	FLEXCOM0_IO0	I/O	3	
H25	VDDIOP1	GPIO	PD11	I/O	-	-	A	SDMMC2_1V8SEL	O	1	PIO, I, PU, ST
							B	PCK7	O	2	
							C	I2SMCC0_DIN3	I	2	
							D	D2	I/O	2	
							E	TIOA3	I/O	2	
							F	FLEXCOM0_IO1	I/O	3	

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
L19	VDDIOP1	GPIO	PD12	I/O	-	-	A	PCK1	O	2	PIO, I, PU, ST
							B	FLEXCOM1_IO0	I/O	2	
							D	CANTX0	O	2	
							E	TIOB3	I/O	2	
K19	VDDIOP1	GPIO	PD13	I/O	-	-	A	I2SMCC0_CK	I/O	2	PIO, I, PU, ST
							B	FLEXCOM1_IO1	I/O	2	
							C	PWML0	O	4	
							D	CANRX0	I	2	
							E	TCLK3	I	2	
J23	VDDIOP1	GPIO	PD14	I/O	-	-	A	I2SMCC0_MCK	O	2	PIO, I, PU, ST
							B	FLEXCOM1_IO2	I/O	2,3,4	
							C	PWMH0	O	4	
							D	CANTX1	O	2	
							E	TIOA4	I/O	2	
							F	FLEXCOM2_IO0	I/O	5	
J18	VDDIOP1	GPIO	PD15	I/O	-	-	A	I2SMCC0_WS	I/O	2	PIO, I, PU, ST
							B	FLEXCOM1_IO3	I/O	2,3,4	
							C	PWML1	O	4	
							D	CANRX1	I	2	
							E	TIOB4	I/O	2	
							F	FLEXCOM2_IO1	I/O	5	
G25	VDDIOP1	GPIO	PD16	I/O	-	-	A	I2SMCC0_DOUT0	O	2	PIO, I, PU, ST
							B	FLEXCOM1_IO4	I/O	2,3,4	
							C	PWMH1	O	4	
							D	CANTX2	O	2	
							E	TCLK4	I	2	
							F	FLEXCOM3_IO0	I/O	5	

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
J20	VDDIOP1	GPIO	PD17	I/O	-	-	A	I2SMCC0_DOUT1	O	2	PIO, I, PU, ST
							B	FLEXCOM2_IO0	I/O	2	
							C	PWML2	O	4	
							D	CANRX2	I	2	
							E	TIOA5	I/O	2	
							F	FLEXCOM3_IO1	I/O	5	
F25	VDDIOP1	GPIO	PD18	I/O	-	-	A	I2SMCC0_DOUT2	O	2	PIO, I, PU, ST
							B	FLEXCOM2_IO1	I/O	2	
							C	PWMH2	O	4	
							D	CANTX3	O	2	
							E	TIOB5	I/O	2	
							F	FLEXCOM4_IO0	I/O	5	
J21	VDDIOP1	GPIO	PD19	I/O	-	-	A	I2SMCC0_DOUT3	O	2	PIO, I, PU, ST
							B	FLEXCOM2_IO2	I/O	2,3,4,5	
							C	PWML3	O	4	
							D	CANRX3	I	2	
							E	TCLK5	I	2	
							F	FLEXCOM4_IO1	I/O	5	
E25	VDDIOP1	GPIO	PD20	I/O	-	-	A	PCK0	O	3	PIO, I, PU, ST
							B	FLEXCOM2_IO3	I/O	2,3,4,5	
							C	PWMH3	O	4	
							D	CANTX4	O	2	
							F	FLEXCOM5_IO0	I/O	5	
J22	VDDIOP1	GPIO	PD21	I/O	-	-	A	PCK1	O	3	PIO, I, PU, ST
							B	FLEXCOM2_IO4	I/O	2,3,4,5	
							D	CANRX4	I	2	
							F	FLEXCOM5_IO1	I/O	5	
							G	G1_TXEN	O	1	

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
G24	VDDIOP1	GPIO	PD22	I/O	-	-	A	PDMC0_CLK	O	2	PIO, I, PU, ST
							C	PWMEXTRG0	I	4	
							D	RD1	I	2	
							F	CANTX5	O	2	
							G	G1_TX0	O	1	
G22	VDDIOP1	GPIO	PD23	I/O	-	-	A	PDMC0_DS0	I	2	PIO, I, PU, ST
							C	PWMEXTRG1	I	4	
							D	RF1	I/O	2	
							E	ISC_MCK	O	2	
							F	CANRX5	I	2	
							G	G1_TX1	O	1	
C25	VDDIOP1	GPIO	PD24	I/O	-	-	A	PDMC0_DS1	I	2	PIO, I, PU, ST
							C	PWMFI0	I	4	
							D	RK1	I/O	2	
							E	ISC_D0	I	2	
							G	G1_RXDV	I	1	
G23	VDDIOP1	GPIO	PD25	I/O	-	-	A	PDMC1_CLK	O	2	PIO, I, PU, ST
							B	FLEXCOM5_IO0	I/O	2	
							C	PWMFI1	I	4	
							D	TD1	O	2	
							E	ISC_D1	I	2	
							G	G1_RX0	I	1	
E23	VDDIOP1	GPIO	PD26	I/O	-	-	A	PDMC1_DS0	I	2	PIO, I, PU, ST
							B	FLEXCOM5_IO1	I/O	2	
							C	ADTRG	I	3	
							D	TF1	I/O	2	
							E	ISC_D2	I	2	
							G	G1_RX1	I	1	

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
B25	VDDIOP1	GPIO	PD27	I/O	-	-	A	PDMC1_DS1	I	2	PIO, I, PU, ST
							B	FLEXCOM5_IO2	I/O	2,3,4,5	
							C	TIOA0	I/O	3	
							D	TK1	I/O	2	
							E	ISC_D3	I	2	
							G	G1_RXER	I	1	
C21	VDDIOP1	GPIO	PD28	I/O	-	-	A	RD0	I	2	PIO, I, PU, ST
							B	FLEXCOM5_IO3	I/O	2,3,4,5	
							C	TIOB0	I/O	3	
							D	I2SMCC1_CK	I/O	2	
							E	ISC_D4	I	2	
							F	PWML3	O	5	
C24	VDDIOP1	GPIO	PD29	I/O	-	-	G	G1_MDC	O	1	PIO, I, PU, ST
							A	RF0	I/O	2	
							B	FLEXCOM5_IO4	I/O	2,3,4,5	
							C	TCLK0	I	3	
							D	I2SMCC1_WS	I/O	2	
							E	ISC_D5	I	2	
E22	VDDIOP1	GPIO	PD30	I/O	-	-	F	PWMH3	O	5	PIO, I, PU, ST
							G	G1_MDIO	I/O	1	
							A	RK0	I/O	2	
							B	FLEXCOM6_IO0	I/O	2	
							C	TIOA1	I/O	3	
							D	I2SMCC1_MCK	O	2	
							E	ISC_D6	I	2	
							F	PWMEXTRG0	I	5	
							G	G1_TXCK	I/O	1	

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
E24	VDDIOP1	GPIO	PD31	I/O	-	-	A	TD0	O	2	PIO, I, PU, ST
							B	FLEXCOM6_IO1	I/O	2	
							C	TIOB1	I/O	3	
							D	I2SMCC1_DOUT0	O	2	
							E	ISC_D7	I	2	
							F	PWMEXTRG1	I	5	
							G	G1_TX2	O	1	
D25	VDDIOP1	GPIO	PE0	I/O	-	-	A	TF0	I/O	2	PIO, I, PU, ST
							B	FLEXCOM6_IO2	I/O	2,3,4,5	
							C	TCLK1	I	3	
							D	I2SMCC1_DOUT1	O	2	
							E	ISC_HSYNC	I	2	
							F	PWMFI0	I	5	
							G	G1_TX3	O	1	
G21	VDDIOP1	GPIO	PE1	I/O	-	-	A	TK0	I/O	2	PIO, I, PU, ST
							B	FLEXCOM6_IO3	I/O	2,3,4,5	
							C	TIOA2	I/O	3	
							D	I2SMCC1_DOUT2	O	2	
							E	ISC_VSYNC	I	2	
							F	PWMFI1	I	5	
							G	G1_RX2	I	1	
A23	VDDIOP1	GPIO	PE2	I/O	-	-	A	PWML0	O	5	PIO, I, PU, ST
							B	FLEXCOM6_IO4	I/O	2,3,4,5	
							C	TIOB2	I/O	3	
							D	I2SMCC1_DOUT3	O	2	
							E	ISC_FIELD	I	2	
							G	G1_RX3	I	1	

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TFBGA427	Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
				Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
B22	VDDIOP1	GPIO	PE3	I/O	-	-		A	PWMH0	O	5	PIO, I, PU, ST
								B	FLEXCOM0_IO0	I/O	4	
								C	TCLK2	I	3	
								D	I2SMCC1_DIN0	I	2	
								E	ISC_PCK	I	2	
								G	G1_RXCK	I	1	
B21	VDDIOP1	GPIO	PE4	I/O	-	-		A	PWML1	O	5	PIO, I, PU, ST
								B	FLEXCOM0_IO1	I/O	4	
								C	TIOA3	I/O	3	
								D	I2SMCC1_DIN1	I	2	
								E	ISC_D8	I	2	
								G	G1_TXER	O	1	
A22	VDDIOP1	GPIO	PE5	I/O	-	-		A	PWMH1	O	5	PIO, I, PU, ST
								B	FLEXCOM0_IO2	I/O	4	
								C	TIOB3	I/O	3	
								D	I2SMCC1_DIN2	I	2	
								E	ISC_D9	I	2	
								G	G1_COL	I	1	
A21	VDDIOP1	GPIO	PE6	I/O	-	-		A	PWML2	O	5	PIO, I, PU, ST
								B	FLEXCOM0_IO3	I/O	4	
								C	TCLK3	I	3	
								D	I2SMCC1_DIN3	I	2	
								E	ISC_D10	I	2	
								G	G1_CRS	I	1	
G20	VDDIOP1	GPIO	PE7	I/O	-	-		A	PWMH2	O	5	PIO, I, PU, ST
								B	FLEXCOM0_IO4	I/O	4	
								C	TIOA4	I/O	3	
								E	ISC_D11	I	2	
								G	G1_TSUCOMP	O	1	
D9	VREFP	analog input	VREFP	-	-	-	-	-	-	-	-	-

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
F14	VDDIN33	power	VDDIN33	I	-	-	-	-	-	-	-
H16	GNDIN33	ground	GNDIN33	I	-	-	-	-	-	-	-
E16	GNDANA	ground	GNDANA	I	-	-	-	-	-	-	-
H10	GNDANA	ground	GNDANA	I	-	-	-	-	-	-	-
H14	GNDANA	ground	GNDANA	I	-	-	-	-	-	-	-
Y16	VDDIOP0	power	VDDIOP0	I	-	-	-	-	-	-	-
Y18	VDDIOP0	power	VDDIOP0	I	-	-	-	-	-	-	-
F24	VDDIOP1	power	VDDIOP1	I	-	-	-	-	-	-	-
H24	VDDIOP1	power	VDDIOP1	I	-	-	-	-	-	-	-
A1	GND	ground	GND	I	-	-	-	-	-	-	-
A25	GND	ground	GND	I	-	-	-	-	-	-	-
AA1	GND	ground	GND	I	-	-	-	-	-	-	-
AA4	GND	ground	GND	I	-	-	-	-	-	-	-
AA6	GND	ground	GND	I	-	-	-	-	-	-	-
AA8	GND	ground	GND	I	-	-	-	-	-	-	-
AA25	GND	ground	GND	I	-	-	-	-	-	-	-
B2	GND	ground	GND	I	-	-	-	-	-	-	-
B16	GND	ground	GND	I	-	-	-	-	-	-	-
B24	GND	ground	GND	I	-	-	-	-	-	-	-
C3	GND	ground	GND	I	-	-	-	-	-	-	-
C23	GND	ground	GND	I	-	-	-	-	-	-	-
D4	GND	ground	GND	I	-	-	-	-	-	-	-
D20	GND	ground	GND	I	-	-	-	-	-	-	-
D22	GND	ground	GND	I	-	-	-	-	-	-	-
E2	GND	ground	GND	I	-	-	-	-	-	-	-
E5	GND	ground	GND	I	-	-	-	-	-	-	-
E18	GND	ground	GND	I	-	-	-	-	-	-	-
E21	GND	ground	GND	I	-	-	-	-	-	-	-
F1	GND	ground	GND	I	-	-	-	-	-	-	-
F9	GND	ground	GND	I	-	-	-	-	-	-	-
F20	GND	ground	GND	I	-	-	-	-	-	-	-

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
G2	GND	ground	GND	I	-	-	-	-	-	-	-
G3	GND	ground	GND	I	-	-	-	-	-	-	-
G5	GND	ground	GND	I	-	-	-	-	-	-	-
G7	GND	ground	GND	I	-	-	-	-	-	-	-
G9	GND	ground	GND	I	-	-	-	-	-	-	-
H1	GND	ground	GND	I	-	-	-	-	-	-	-
H5	GND	ground	GND	I	-	-	-	-	-	-	-
H8	GND	ground	GND	I	-	-	-	-	-	-	-
H21	GND	ground	GND	I	-	-	-	-	-	-	-
J1	GND	ground	GND	I	-	-	-	-	-	-	-
J3	GND	ground	GND	I	-	-	-	-	-	-	-
J5	GND	ground	GND	I	-	-	-	-	-	-	-
J7	GND	ground	GND	I	-	-	-	-	-	-	-
J9	GND	ground	GND	I	-	-	-	-	-	-	-
J10	GND	ground	GND	I	-	-	-	-	-	-	-
J16	GND	ground	GND	I	-	-	-	-	-	-	-
K2	GND	ground	GND	I	-	-	-	-	-	-	-
K8	GND	ground	GND	I	-	-	-	-	-	-	-
K10	GND	ground	GND	I	-	-	-	-	-	-	-
K11	GND	ground	GND	I	-	-	-	-	-	-	-
K13	GND	ground	GND	I	-	-	-	-	-	-	-
K15	GND	ground	GND	I	-	-	-	-	-	-	-
K21	GND	ground	GND	I	-	-	-	-	-	-	-
L1	GND	ground	GND	I	-	-	-	-	-	-	-
L3	GND	ground	GND	I	-	-	-	-	-	-	-
L5	GND	ground	GND	I	-	-	-	-	-	-	-
L7	GND	ground	GND	I	-	-	-	-	-	-	-
L8	GND	ground	GND	I	-	-	-	-	-	-	-
L12	GND	ground	GND	I	-	-	-	-	-	-	-
L14	GND	ground	GND	I	-	-	-	-	-	-	-
L16	GND	ground	GND	I	-	-	-	-	-	-	-

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
L17	GND	ground	GND	I	-	-	-	-	-	-	-
L18	GND	ground	GND	I	-	-	-	-	-	-	-
M2	GND	ground	GND	I	-	-	-	-	-	-	-
M5	GND	ground	GND	I	-	-	-	-	-	-	-
M6	GND	ground	GND	I	-	-	-	-	-	-	-
M8	GND	ground	GND	I	-	-	-	-	-	-	-
M11	GND	ground	GND	I	-	-	-	-	-	-	-
M13	GND	ground	GND	I	-	-	-	-	-	-	-
M15	GND	ground	GND	I	-	-	-	-	-	-	-
M17	GND	ground	GND	I	-	-	-	-	-	-	-
M18	GND	ground	GND	I	-	-	-	-	-	-	-
M21	GND	ground	GND	I	-	-	-	-	-	-	-
N1	GND	ground	GND	I	-	-	-	-	-	-	-
N2	GND	ground	GND	I	-	-	-	-	-	-	-
N4	GND	ground	GND	I	-	-	-	-	-	-	-
N7	GND	ground	GND	I	-	-	-	-	-	-	-
N9	GND	ground	GND	I	-	-	-	-	-	-	-
N10	GND	ground	GND	I	-	-	-	-	-	-	-
N12	GND	ground	GND	I	-	-	-	-	-	-	-
N14	GND	ground	GND	I	-	-	-	-	-	-	-
N18	GND	ground	GND	I	-	-	-	-	-	-	-
P2	GND	ground	GND	I	-	-	-	-	-	-	-
P5	GND	ground	GND	I	-	-	-	-	-	-	-
P8	GND	ground	GND	I	-	-	-	-	-	-	-
P11	GND	ground	GND	I	-	-	-	-	-	-	-
P13	GND	ground	GND	I	-	-	-	-	-	-	-
P18	GND	ground	GND	I	-	-	-	-	-	-	-
P24	GND	ground	GND	I	-	-	-	-	-	-	-
R1	GND	ground	GND	I	-	-	-	-	-	-	-
R3	GND	ground	GND	I	-	-	-	-	-	-	-
R6	GND	ground	GND	I	-	-	-	-	-	-	-

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
R7	GND	ground	GND	I	-	-	-	-	-	-	-
R10	GND	ground	GND	I	-	-	-	-	-	-	-
R11	GND	ground	GND	I	-	-	-	-	-	-	-
R19	GND	ground	GND	I	-	-	-	-	-	-	-
T2	GND	ground	GND	I	-	-	-	-	-	-	-
T5	GND	ground	GND	I	-	-	-	-	-	-	-
T9	GND	ground	GND	I	-	-	-	-	-	-	-
T11	GND	ground	GND	I	-	-	-	-	-	-	-
T12	GND	ground	GND	I	-	-	-	-	-	-	-
T21	GND	ground	GND	I	-	-	-	-	-	-	-
U1	GND	ground	GND	I	-	-	-	-	-	-	-
U3	GND	ground	GND	I	-	-	-	-	-	-	-
U8	GND	ground	GND	I	-	-	-	-	-	-	-
U10	GND	ground	GND	I	-	-	-	-	-	-	-
U12	GND	ground	GND	I	-	-	-	-	-	-	-
U14	GND	ground	GND	I	-	-	-	-	-	-	-
U16	GND	ground	GND	I	-	-	-	-	-	-	-
U18	GND	ground	GND	I	-	-	-	-	-	-	-
V2	GND	ground	GND	I	-	-	-	-	-	-	-
V4	GND	ground	GND	I	-	-	-	-	-	-	-
V7	GND	ground	GND	I	-	-	-	-	-	-	-
V9	GND	ground	GND	I	-	-	-	-	-	-	-
V24	GND	ground	GND	I	-	-	-	-	-	-	-
W1	GND	ground	GND	I	-	-	-	-	-	-	-
W3	GND	ground	GND	I	-	-	-	-	-	-	-
W5	GND	ground	GND	I	-	-	-	-	-	-	-
W11	GND	ground	GND	I	-	-	-	-	-	-	-
W23	GND	ground	GND	I	-	-	-	-	-	-	-
Y2	GND	ground	GND	I	-	-	-	-	-	-	-
Y5	GND	ground	GND	I	-	-	-	-	-	-	-
Y7	GND	ground	GND	I	-	-	-	-	-	-	-

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TFBGA427	Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
				Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
	Y10	GND	ground	GND	I	-	-	-	-	-	-	-
	Y12	GND	ground	GND	I	-	-	-	-	-	-	-
	Y24	GND	ground	GND	I	-	-	-	-	-	-	-
	F10	VDDANA	power	VDDANA	I	-	-	-	-	-	-	-
	F12	VDDANA	power	VDDANA	I	-	-	-	-	-	-	-
	J15	VDDANAOUT	analog output	VDDOUT25	I	-	-	-	-	-	-	-
	G11	VDDCORE	power	VDDCORE	I	-	-	-	-	-	-	-
	H12	VDDCORE	power	VDDCORE	I	-	-	-	-	-	-	-
	J17	VDDCORE	power	VDDCORE	I	-	-	-	-	-	-	-
	K17	VDDCORE	power	VDDCORE	I	-	-	-	-	-	-	-
	K20	VDDCORE	power	VDDCORE	I	-	-	-	-	-	-	-
	L13	VDDCORE	power	VDDCORE	I	-	-	-	-	-	-	-
	M12	VDDCORE	power	VDDCORE	I	-	-	-	-	-	-	-
	N17	VDDCORE	power	VDDCORE	I	-	-	-	-	-	-	-
	N19	VDDCORE	power	VDDCORE	I	-	-	-	-	-	-	-
	P21	VDDCORE	power	VDDCORE	I	-	-	-	-	-	-	-
	T14	VDDCORE	power	VDDCORE	I	-	-	-	-	-	-	-
	T16	VDDCORE	power	VDDCORE	I	-	-	-	-	-	-	-
	T24	VDDCORE	power	VDDCORE	I	-	-	-	-	-	-	-
	V19	VDDCORE	power	VDDCORE	I	-	-	-	-	-	-	-
	F21	VDDCPU	power	VDDCPU	I	-	-	-	-	-	-	-
	G19	VDDCPU	power	VDDCPU	I	-	-	-	-	-	-	-
	H20	VDDCPU	power	VDDCPU	I	-	-	-	-	-	-	-
	J19	VDDCPU	power	VDDCPU	I	-	-	-	-	-	-	-
	K18	VDDCPU	power	VDDCPU	I	-	-	-	-	-	-	-
	E8	GNDUTMI	ground	GNDUTMI	I	-	-	-	-	-	-	-
	E10	GNDUTMI	ground	GNDUTMI	I	-	-	-	-	-	-	-
	E12	GNDUTMI	ground	GNDUTMI	I	-	-	-	-	-	-	-
	E14	GNDUTMI	ground	GNDUTMI	I	-	-	-	-	-	-	-
	H18	GNDUTMI	ground	GNDUTMI	I	-	-	-	-	-	-	-

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
B8	VDDUTMI	power	VDDUTMI	I	-	-	-	-	-	-	-
B10	VDDUTMI	power	VDDUTMI	I	-	-	-	-	-	-	-
B12	VDDUTMI	power	VDDUTMI	I	-	-	-	-	-	-	-
B14	VDDUTMI	power	VDDUTMI	I	-	-	-	-	-	-	-
F16	VDDUTMI	power	VDDUTMI	I	-	-	-	-	-	-	-
A11	VDDUTMI	-	HHS_A_DP	I/O	-	-	-	-	-	-	-
B11	VDDUTMI	-	HHS_A_DM	I/O	-	-	-	-	-	-	-
C13	VDDUTMI	-	HHS_A_CC1	I/O	-	-	-	-	-	-	-
D15	VDDUTMI	-	HHS_A_CC2	I/O	-	-	-	-	-	-	-
A10	VDDUTMI	analog input	HHS_A_RTUNE	I	-	-	-	-	-	-	-
A13	VDDUTMI	-	HHS_B_DP	I/O	-	-	-	-	-	-	-
B13	VDDUTMI	-	HHS_B_DM	I/O	-	-	-	-	-	-	-
C15	VDDUTMI	-	HHS_B_CC1	I/O	-	-	-	-	-	-	-
D17	VDDUTMI	-	HHS_B_CC2	I/O	-	-	-	-	-	-	-
A12	VDDUTMI	analog input	HHS_B_RTUNE	I	-	-	-	-	-	-	-
A15	VDDUTMI	-	HHSC_DP	I/O	-	-	-	-	-	-	-
B15	VDDUTMI	-	HHSC_DM	I/O	-	-	-	-	-	-	-
A14	VDDUTMI	analog input	HHSC_RTUNE	I	-	-	-	-	-	-	-
K12	VDDIODDR	power	VDDIODDR	I	-	-	-	-	-	-	-
K14	VDDIODDR	power	VDDIODDR	I	-	-	-	-	-	-	-
L9	VDDIODDR	power	VDDIODDR	I	-	-	-	-	-	-	-
L10	VDDIODDR	power	VDDIODDR	I	-	-	-	-	-	-	-
L11	VDDIODDR	power	VDDIODDR	I	-	-	-	-	-	-	-
L15	VDDIODDR	power	VDDIODDR	I	-	-	-	-	-	-	-
M9	VDDIODDR	power	VDDIODDR	I	-	-	-	-	-	-	-
M10	VDDIODDR	power	VDDIODDR	I	-	-	-	-	-	-	-
M14	VDDIODDR	power	VDDIODDR	I	-	-	-	-	-	-	-
M16	VDDIODDR	power	VDDIODDR	I	-	-	-	-	-	-	-

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
N11	VDDIODDR	power	VDDIODDR	I	-	-	-	-	-	-	-
N13	VDDIODDR	power	VDDIODDR	I	-	-	-	-	-	-	-
N15	VDDIODDR	power	VDDIODDR	I	-	-	-	-	-	-	-
P10	VDDIODDR	power	VDDIODDR	I	-	-	-	-	-	-	-
P12	VDDIODDR	power	VDDIODDR	I	-	-	-	-	-	-	-
P14	VDDIODDR	power	VDDIODDR	I	-	-	-	-	-	-	-
R13	VDDIODDR	power	VDDIODDR	I	-	-	-	-	-	-	-
E4	VDDIODDR	analog input	DDR_VREF	-	-	-	-	-	-	-	-
R12	VDDIODDR	analog input	DDR_VREF	-	-	-	-	-	-	-	-
G4	VDDIODDR	analog input	DDRM_ZQ	-	-	-	-	-	-	-	-
J12	VDDIODDR	analog input	DDR_ZQ	-	-	-	-	-	-	-	-
A4	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
AA3	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
AA5	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
AA7	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
B6	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
E1	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
E3	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
E7	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
E9	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
F2	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
F5	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
F6	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
F8	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
G1	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
G6	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
H2	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
H6	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
J2	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
J4	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
J6	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
K1	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
K5	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
K6	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
K7	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
K9	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
L2	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
L4	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
L6	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
M1	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
M7	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
N3	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
N5	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
N6	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
N8	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
P1	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
P6	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
R2	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
R4	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
R5	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
R9	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
T1	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
T6	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
T8	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
T10	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
U2	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
U4	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
U5	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
U7	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
U9	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
V1	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
V6	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
W2	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
W6	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
W7	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
W9	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
Y1	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
Y4	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
Y6	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
Y8	DDRM_VDD	power	DDRM_VDD	-	-	-	-	-	-	-	-
T20	VDDDPHY	power	VDDDPHY	I	-	-	-	-	-	-	-
U21	VDDDPHY	power	VDDDPHY	I	-	-	-	-	-	-	-
V20	GNDDPHY	ground	GNDDPHY	I	-	-	-	-	-	-	-
V22	GNDDPHY	ground	GNDDPHY	I	-	-	-	-	-	-	-
Y21	VDDDPHY	-	MIPI_CLKN	-	-	-	-	-	-	-	-
AA21	VDDDPHY	-	MIPI_CLKP	-	-	-	-	-	-	-	-
Y22	VDDDPHY	analog input	MIPI_DN0	-	-	-	-	-	-	-	-
Y20	VDDDPHY	analog input	MIPI_DP0	-	-	-	-	-	-	-	-
Y20	VDDDPHY	analog input	MIPI_DN1	-	-	-	-	-	-	-	-
AA20	VDDDPHY	analog input	MIPI_DP1	-	-	-	-	-	-	-	-
AA23	VDDDPHY	analog input	MIPI_REXT	-	-	-	-	-	-	-	-
M24	VDDSDMMC0	power	VDDSDMMC0	I	-	-	-	-	-	-	-
B18	VDDSDMMC1	power	VDDSDMMC1	I	-	-	-	-	-	-	-
D24	VDDSDMMC2	power	VDDSDMMC2	I	-	-	-	-	-	-	-

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TFBGA427 Pins	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral				Reset State
			Signal	Dir	Signal	Dir	Func	Signal	Dir	I/O Set	Signal, Dir, PU, PD, HiZ, ST, SEC, FILTER
M20	VDDSDMMC0	analog input	SDMMC0_CAL	-	-	-	-	-	-	-	-
F18	VDDSDMMC1	analog input	SDMMC1_CAL	-	-	-	-	-	-	-	-
B20	VDDSDMMC2	analog input	SDMMC2_CAL	-	-	-	-	-	-	-	-
N16	GNDBAT	ground	GNDBAT	I	-	-	-	-	-	-	-
K16	VBAT	power	VBAT	I	-	-	-	-	-	-	-
V13	VBAT	PIOBU	PIOBU0	-	-	-	-	-	-	-	-
T15	VBAT	PIOBU	PIOBU1	-	-	-	-	-	-	-	-
V11	VBAT	PIOBU	PIOBU2	-	-	-	-	-	-	-	-
U13	VBAT	PIOBU	PIOBU3	-	-	-	-	-	-	-	-
C2	VDDIN33	-	XIN	-	-	-	-	-	-	-	-
C1	VDDIN33	-	XOUT	-	-	-	-	-	-	-	-
Y9	VBAT	-	XIN32	-	-	-	-	-	-	-	-
AA9	VBAT	-	XOUT32	-	-	-	-	-	-	-	-
U11	VBAT	-	TST	-	-	-	-	-	-	-	-
T13	VBAT	-	JTAGSEL	-	-	-	-	-	-	-	-
Y11	VBAT	-	WKUP0	-	-	-	-	-	-	-	-
R15	VBAT	-	SHDN	-	-	-	-	-	-	-	-
G13	VDDIN33	-	NRST	-	-	-	-	-	-	-	-
B9	VDDIN33	-	NRST_OUT	-	-	-	-	-	-	-	-
J11	VDDIN33	GPIO	AUDIOCLK	-	-	-	-	-	-	-	-
P15	VBAT	-	LPM	-	-	-	-	-	-	-	-
P20	VDDQSPI0	-	VDDQSPI0	-	-	-	-	-	-	-	-
R17	VDDQSPI0	analog input	QSPI0_CAL	-	-	-	-	-	-	-	-
K24	VDDQSPI1	-	VDDQSPI1	-	-	-	-	-	-	-	-
Y12	GND	-	GND	-	-	-	-	-	-	-	-

Note:

1. DDRM_VDD and VDDIODDR must be connected to one single power plane of the application PCB.

6. Electrical Characteristics

The Electrical Characteristics sections in the SAMA7G5 Series and DDR3L SDRAM data sheets (see [Reference Documents](#)) apply to this device. Complementary information is provided in the following sections.

The VDDQ and VDD power inputs described in the DDR3L SDRAM data sheets are connected to the SAMA7G5 SIP balls called “DDRM_VDD”. Therefore, the requirements placed on VDDQ and VDD power inputs in the “Absolute Maximum Ratings” and “Recommended DC Operating Conditions” sections of these data sheets apply to the DDRM_VDD power inputs.

6.1 Recommended Thermal Operating Conditions

Table 6-1. Recommended Thermal Operating Conditions

Symbol	Parameter	Min	Max	Unit
T _{J_MPU}	Junction temperature range	-40	105	°C
T _{J_DDR3L}	Junction temperature range	-40	105	°C

Table 6-2. BGA343 Package Thermal Characteristics⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Typ	Unit
R _{JA}	Junction-to-ambient thermal resistance	21	°C/W

Notes:

1. $R_{JA} = (T_{J_MPU} - T_A) / P_{MPU}$, where T_A is the ambient temperature and P_{MPU} is the processor power consumption. The DDR3L SDRAM junction temperature is always lower than the MPU junction temperature.
2. According to the JEDEC JESD51-2 standard, with 2s2p board and 0 m/s air flow.
3. These values are not directly applicable to the board where the device is mounted. As per JEDEC standards, these parameters do not characterize the package itself but rather the package together with the PCB (4-layer or more) and other environmental factors (still air, etc.). For example, in still-air JEDEC-defined R_{JA} measurements, almost 70% of the power generated by the chip is dissipated from the test board, not from the package surfaces.

6.2 Power Sequences

The DDR3L SDRAM power rail (DDRM_VDD) must be connected to VDDIODDR (1.35V) on the PCB. Refer to Recommended Power Supply Sequencing in section Electrical Characteristics of the SAMA7G5 Series data sheet.

6.3 Device Power Consumption in Applicative Use Cases

[Table 6-4](#) provides the device power consumption in the following conditions:

- f_{CPU_CLK}: 1 GHz
- f_{MCK1}: 200 MHz
- f_{MCK2}: 533 MHz
- f_{MCK3}: 266 MHz
- f_{MCK4}: 400 MHz
- I & D caches enabled
- Use cases run on Linux®
- Ambient temperature: 25°C
- Current consumptions are measured as shown in [Figure 6-1](#). Note that the external component current consumptions are not counted.

The measurements are provided for typical SAMA7G54D1G, SAMA7G54D2G and SAMA7G54D4G devices.

Table 6-3. Use Case Definition

Use Case	Description
1	Audio MP3 decoding and playback on I ² S; MP3 file on USB mass storage
2	SAMA7G5 running as iPerf server
3	Run Bonnie++ on USB mass storage
4	SAMA7G5 downloads a file from GMAC0 and copies this file to USB mass storage
5	Streaming camera on Ethernet (image format: RAW8, 1080p @ 30 fps)

Figure 6-1. Current Measurement for Applicative Use Cases

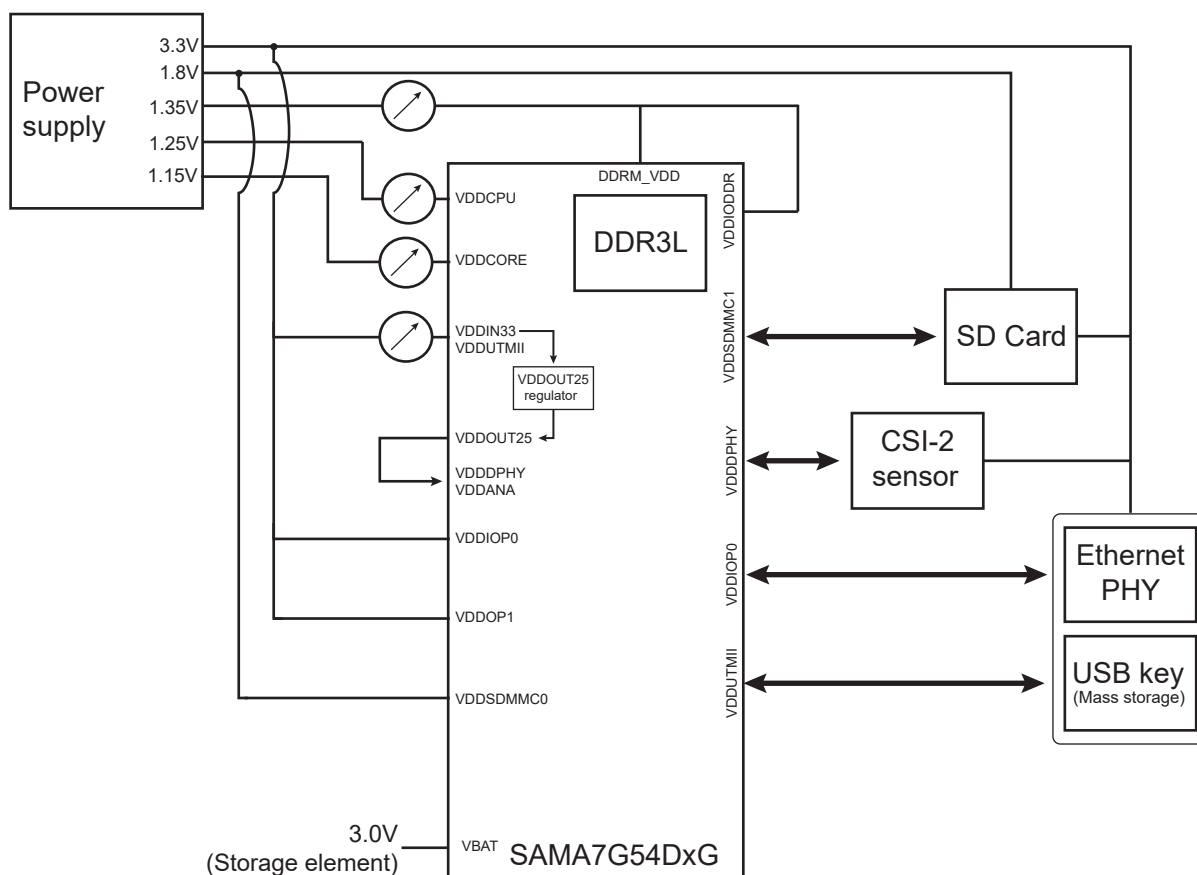


Table 6-4. Power Consumption in Applicative Use Cases

Use Case	Power Consumption (mW)				Total
	VDDCORE 1.15V	VDDCPU 1.25V	VDDIODDR DDR3L DDR4L 1.35V	VDDIN33 VDDUTMI 3.3V	
1	250	85	91	127	553
2	281	215	190	157	843
3	274	253	113	123	762
4	278	216	168	121	784

.....continued

Use Case	Power Consumption (mW)				
	VDDCORE 1.15V	VDDCPU 1.25V	VDDIODDR DDRM_VDD 1.35V	VDDIN33 VDDUTMI 3.3V	Total
5	283	183	140	138	744

6.4 SDRAM Power Consumption in Idle and Ultra-Low Power (ULP0, ULP1, ULP2) Modes with SDRAM in Self-Refresh

For a complete description of how to enter and exit ULP0, ULP1 or ULP2 mode, refer to the SAMA7G5 Series data sheet (see [Reference Documents](#)).

Table 6-5. Typical Current Consumption in Idle, ULP0, ULP1 or ULP2 Mode on VDDIODDR and DDRM_VDD

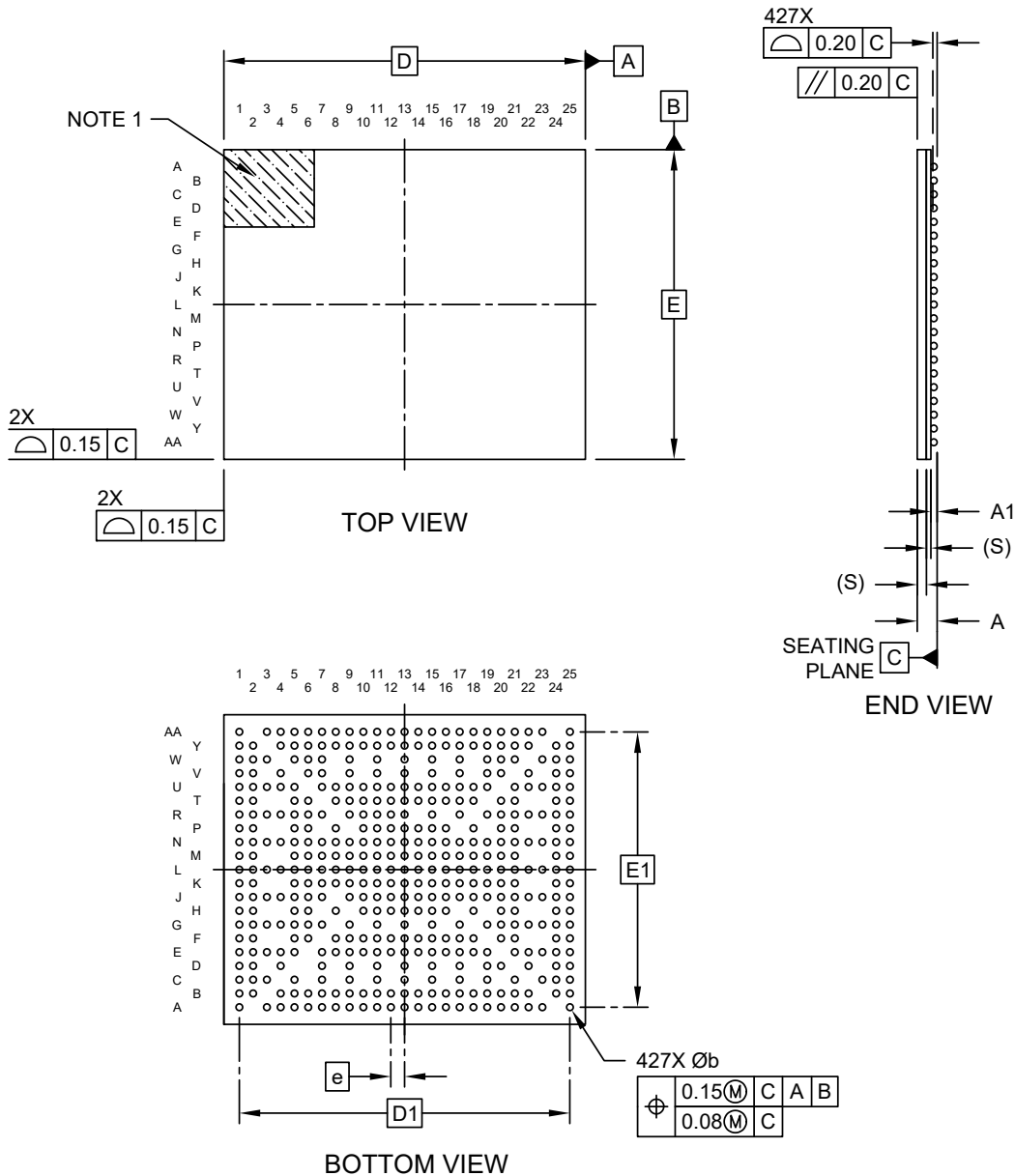
VDDIODDR DDRM_VDD (V)	T _A = -40°C	T _A = 25°C	T _A = 50°C	T _A = 70°C	T _A =85°C	Unit
1.35	6	6	6	7	7	mA

7. Mechanical Characteristics

7.1 427-Ball TFBGA Mechanical Characteristics

427-Ball Thin Fine-Pitch Ball Grid Array (4UB) - 21x18x1.2 mm Body [TFBGA]

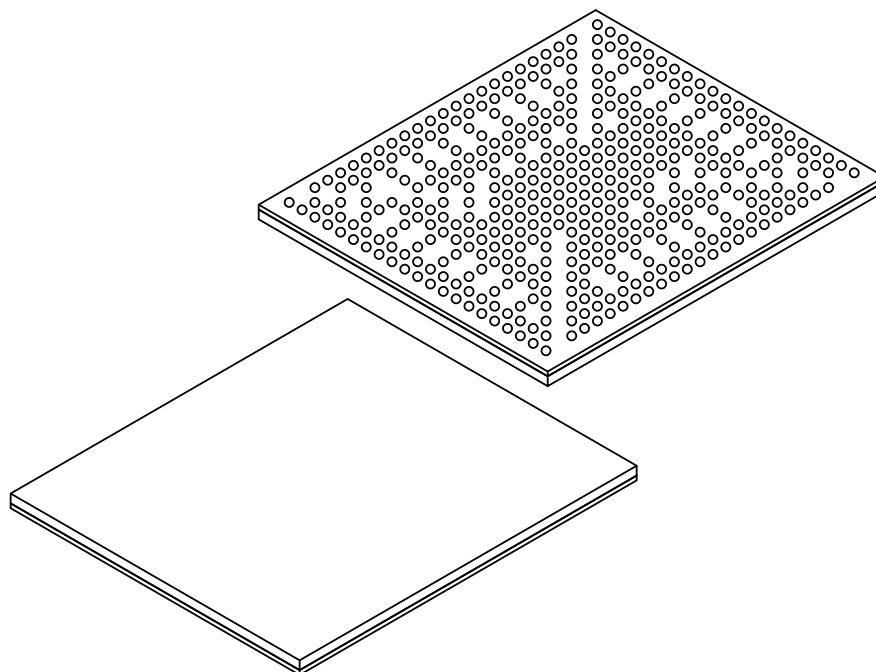
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-21537 Rev A Sheet 1 of 2

427-Ball Thin Fine-Pitch Ball Grid Array (4UB) - 21x18x1.2 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	427		
Pitch	e	0.80 BSC		
Overall Height	A	–	–	1.20
Ball Height	A1	0.27	–	0.37
Mold Thickness	M	0.53 REF		
Substrate Thickness	S	0.26 REF		
Overall Length	D	21.00 BSC		
Ball Array Length	D2	19.20 BSC		
Overall Width	E	18.00 BSC		
Ball Array Width	E2	16.00 BSC		
Ball Width	b	0.38	–	0.45

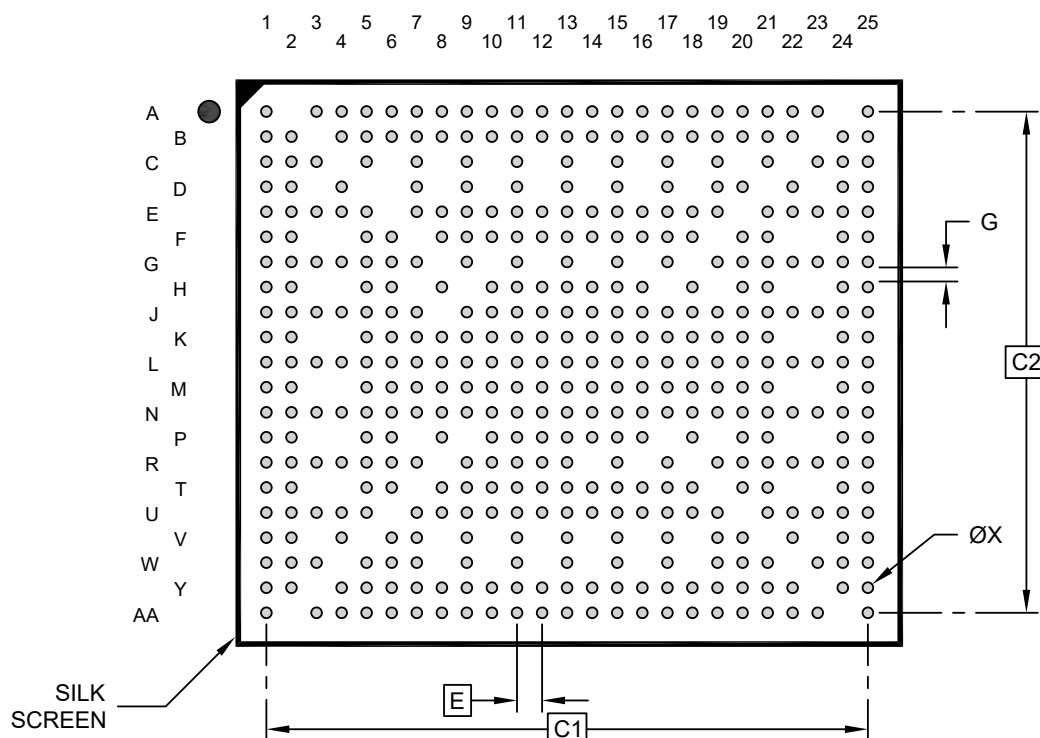
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21537 Rev A Sheet 2 of 2

427-Ball Thin Fine-Pitch Ball Grid Array (4UB) - 21x18x1.2 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.80 BSC		
Contact Pad Spacing	C1	19.20 BSC		
Contact Pad Spacing	C2	16.00 BSC		
Contact Pad Width (Xnn)	X			0.35
Contact Pad to Contact Pad (Xnn)	G	0.45		

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-23537 Rev A

Table 7-1. 427-ball TFBGA Package Characteristics

Moisture sensitivity level	MSL3
----------------------------	------

Table 7-2. Device and 427-ball TFBGA Package Weight

980	mg
-----	----

Table 7-3. Package Reference

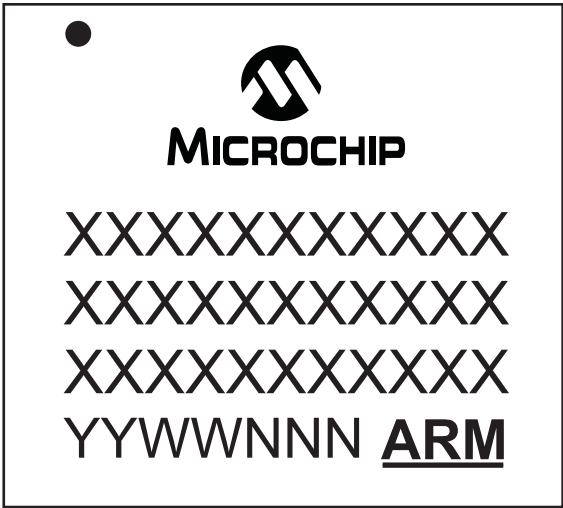
JEDEC drawing reference	NA
J-STD-609 classification	e8

Table 7-4. 427-ball TFBGA Package Information

Ball land	0.450 mm
Nominal ball diameter	0.400 mm
Solder mask opening	0.350 mm
Solder mask definition	Solder Mask Defined (SMD)
Solder	SAC105

8. Marking

Top marking follows the scheme below:



with possible values:

Line	Description	Values
1	Company logo	Microchip logo
2	Company name	Microchip
3	Device name	SAMA7G54-DxG
4	Temperature code/Package	I\4UB
5	Not used	-
6	Lot traceability, Arm logo	YYWWNNN ARM

9. Ordering Information

For details on ordering codes, see [Product Identification System](#).

Ordering Code	Memory Type	Memory Size	Package	Carrier Type	Junction Temperature Range ⁽¹⁾
SAMA7G54D1G-I4UB	DDR3L SDRAM	1 Gbit	TFBGA427	Tray	-40°C to +105°C
SAMA7G54D1GT-I4UB		1 Gbit		Tape and Reel	
SAMA7G54D2G-I4UB		2 Gbits		Tray	
SAMA7G54D2GT-I4UB		2 Gbits		Tape and Reel	
SAMA7G54D4G-I4UB ⁽²⁾		4 Gbits		Tray	
SAMA7G54D4GT-I4UB ⁽²⁾		4 Gbits		Tape and Reel	

Notes:

1. Applies to both the MPU and the DDR3L memory junction temperatures.
2. To order this device, contact your local Microchip sales representative.

10. Revision History

10.1 DS50003577A - 09/2023

Changes
First issue

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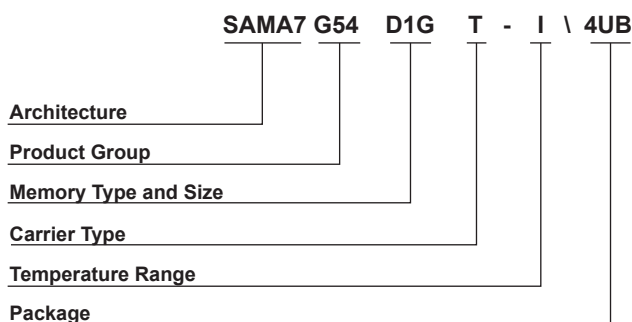
- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

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Product Identification System

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Architecture:	SAMA7	= Arm Cortex-A7 CPU
Product Group:	G54	= 427-ball general-purpose microprocessors
Memory Type and Size:	D1G	= 1-Gbit DDR3L SDRAM
	D2G	= 2-Gbit DDR3L SDRAM
	D4G	= 4-Gbit DDR3L SDRAM
Carrier Type:	Blank	= Standard packaging (tray)
	T	= Tape and Reel
Ambient Temperature Range ⁽¹⁾ :	I	= -40°C to +85°C (industrial)
Package:	4UB	= 427-ball TFBGA
Note:		
1. Indicative Ambient Temperature Range. The user must not exceed the maximum Junction Temperature (T _J) defined in the section Electrical Characteristics .		

Example:

- SAMA7G54D1GT-IV4UB = Arm Cortex-A7 general-purpose microprocessor, 1-Gbit DDR3L SDRAM, tape and reel packaging, industrial temperature, 427-ball TFBGA

Note: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package.

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