




<b>PCN Number:</b>	20231219026.2		<b>PCN Date:</b>	December 19, 2023																			
<b>Title:</b>	Qualification of LFAB as an additional Wafer Fab site option for select devices																						
<b>Customer Contact:</b>	Change Management team		<b>Dept:</b>	Quality Services																			
<b>Proposed 1<sup>st</sup> Ship Date:</b>	Jun 19, 2024		<b>Sample Requests accepted until:</b>	Jan 19, 2024*																			
<b>*Sample requests received after January 19, 2024 will not be supported.</b>																							
<b>Change Type:</b>																							
<input type="checkbox"/>	Assembly Site	<input type="checkbox"/>	Design	<input type="checkbox"/>	Wafer Bump Material																		
<input type="checkbox"/>	Assembly Process	<input type="checkbox"/>	Data Sheet	<input type="checkbox"/>	Wafer Bump Process																		
<input type="checkbox"/>	Assembly Materials	<input type="checkbox"/>	Part number change	<input checked="" type="checkbox"/>	Wafer Fab Site																		
<input type="checkbox"/>	Mechanical Specification	<input type="checkbox"/>	Test Site	<input type="checkbox"/>	Wafer Fab Material																		
<input checked="" type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>	Test Process	<input type="checkbox"/>	Wafer Fab Process																		
<b>PCN Details</b>																							
<b>Description of Change:</b>																							
Texas Instruments is pleased to announce the addition of LFAB as an additional Wafer Fab site option for the products listed in the "Product Affected" section of this document.																							
<table border="1"> <thead> <tr> <th colspan="3">Current Fab Site</th> <th colspan="3">Additional Fab Site</th> </tr> <tr> <th>Current Fab Site</th> <th>Process</th> <th>Wafer Diameter</th> <th>New Fab Site</th> <th>Process</th> <th>Wafer Diameter</th> </tr> </thead> <tbody> <tr> <td>UMC12i</td> <td>F65</td> <td>300mm</td> <td>LFAB</td> <td>F65</td> <td>300mm</td> </tr> </tbody> </table>			Current Fab Site			Additional Fab Site			Current Fab Site	Process	Wafer Diameter	New Fab Site	Process	Wafer Diameter	UMC12i	F65	300mm	LFAB	F65	300mm			
Current Fab Site			Additional Fab Site																				
Current Fab Site	Process	Wafer Diameter	New Fab Site	Process	Wafer Diameter																		
UMC12i	F65	300mm	LFAB	F65	300mm																		
Qual details are provided in the Qual Data Section.																							
<b>Reason for Change:</b>																							
Continuity of supply																							
<b>Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):</b>																							
None																							
<b>Changes to product identification resulting from this PCN:</b>																							
<b>Device Symbol:</b> <div style="display: flex; align-items: center; margin-top: 20px;"> <div style="border: 1px solid black; padding: 10px; text-align: center; margin-right: 20px;">  <p><b>F28388DPTPS</b> <b>\$\$-YMLLLLS</b> <b>G4</b></p> </div> <div> <p><b>YMLLLLS = Lot Trace Code</b></p> <p>YM = 2-Digit Year/Month Code  LLLL = Assembly Lot  S = Assembly Site Code  \$\$ = Wafer Fab Code as applicable  # = Silicon Revision Code</p> </div> </div> <div style="margin-top: 10px;">  <p>Package Pin 1</p> </div>																							
<b>Original Fab Field:</b> \$\$ = \$7 → UMC 12i																							
<b>Updated Fab Field:</b> \$\$ = 3L → LFAB																							
<b>Current Fab Site Information:</b>																							
<b>Chip Site</b>	<b>Chip Site Origin Code (20L)</b>	<b>Chip Site Country Code (21L)</b>	<b>Chip Site City</b>																				
UMC12i	UMI	SGP	Singapore																				

**Additional Fab Site Information:**

New Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City
<b>LFAB</b>	<b>LHI</b>	<b>USA</b>	<b>Lehi</b>

Sample product shipping label (not actual product label)

 **TEXAS INSTRUMENTS**  
 MADE IN: Malaysia  
 2DC: 20:  
 MSL '2 /260C/1 YEAR SEAL DT  
 MSL 1 /235C/UNLIM 03/29/04  
 OPT:  
 ITEM:  
**LBL: 5A (L)T0:1750**



(1P) **SN74LS07NSR**  
 (Q) **2000** (D) **0336**  
 (31T) LOT: 3959047MLA  
 (4W) TKY (1T) 7523483SI2  
 (P)  
 (2P) REV: (V) 0033317  
 (20L) CSO: SHE (21L) CCO: USA  
 (22L) ASO: MLA (23L) ACO: MYS

**Product Affected:**

F28384DPTPQR	F28384SPTPQR	F28386DPTPQR	F28386DZWTQR
F28384DZWTQR	F28386DPTPQ	F28386DZWTQ	F28386SPTPQR

**Automotive New Product Qualification Summary**  
 (As per AEC-Q100 Rev. H and JEDEC Guidelines)
**Qualification Results**

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: F28388DZWS	Qual Device: F28388SPTPS	QBS Wafer fab Process qualification TMS320F28379SPTPQ
<b>Test Group A - Accelerated Environment Stress Tests</b>										
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL3 260C	-	1/77/0	QBS	3/462/0
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST	110C/85%RH	264 Hours	QBS	QBS	3/231/0
AC/UHAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Unbiased HAST	130C/85%RH	96 Hours	QBS	QBS	3/231/0
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	1/77/0	QBS	3/231/0
TC-BP	A4	MIL-STD883 Method 2011	1	5	Post Temp Cycle Bond Pull	-	-	1/5/0	QBS	1/5/0
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	150C	1000 Hours	QBS	QBS	3/135/0
<b>Test Group B - Accelerated Lifetime Simulation Tests</b>										
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	125C	1000 Hours	3/231/0	QBS	3/231/0 [1]
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate	125C	48 Hours	QBS	QBS	3/2400/0
EDR	B3	AEC Q100-005	3	77	NVM Endurance, Data Retention and Operational Life	150C	1000 hours	QBS	QBS	3/231/0 [1]
<b>Test Group C - Package Assembly Integrity Tests</b>										
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	1/30/0	3/90/0

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: <a href="#">F28388DZWTS</a>	Qual Device: <a href="#">F28388SPTPS</a>	QBS Wafer fab Process qualification <a href="#">TMS320F28379SPTPQ</a>
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	1/30/0	3/90/0
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	Package family data	Package family data	-
<b>Test Group D - Die Fabrication Reliability Tests</b>										
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDDb	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
BTI	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
<b>Test Group E - Electrical Verification Tests</b>										
ESD	E2	AEC Q100-002	1	3	ESD HBM	-	2000 Volts	1/3/0	1/3/0	
ESD	E3	AEC Q100-011	1	3	ESD CDM	-	500 Volts	1/3/0	1/3/0	
LU	E4	AEC Q100-004	1	6	Latch-Up	Per AEC Q100-004	-	1/6/0	1/6/0	
Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: <a href="#">F28388DZWTS</a>	Qual Device: <a href="#">F28388SPTPS</a>	QBS Wafer fab Process qualification <a href="#">TMS320F28379SPTPQ</a>
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	3/90/0	1/30/0	
<b>Additional Tests</b>										

- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
- The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
- The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
- The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles
- [1] HTOL and EDR were preconditioned with Write and Erase of the flash memory.

- QBS: Qual By Similarity

**Ambient Operating Temperature by Automotive Grade Level:**

- Grade 0 (or E): -40C to +150C
- Grade 1 (or Q): -40C to +125C
- Grade 2 (or T): -40C to +105C
- Grade 3 (or J): -40C to +85C

**E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):**

- Room/Hot/Cold : HTOL, ED
- Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
- Room : AC/uHAST

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

TI Qualification ID: R-CHG-2206-073

ZVEI ID: SEM-PW-13

For questions regarding this notice, e-mails can be sent to the Change Management team or your local Field Sales Representative.

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