PCN	Number:	202	3082	9004.2				PCN	Date:		August 30, 2023	
<b>Title:</b> Qualification of LFAB as an additional Fab site and CD-PR as an additional Probe Site fo select devices											nal Probe Site for	
Customer Contact: Change Management team Dept: Quality Services												
Proposed 1 <sup>st</sup> Ship Date: Feb 29, 2024  Sample requests accepted until: Sep 29, 2023*									29, 2023*			
*Sar	nple reque	sts re	ceive	d afte	r Sep	tember 29,	2023 will n	ot be	suppo	rte	d.	
Char	nge Type:											
	Assembly S	te				Design			Wafer	Wafer Bump Material		
	Assembly P	ocess				Data Sheet			☐ Wafer Bump Process			
	Assembly M	ateria	S			Part numbe	r change		Wafer	· Fal	b Site	
☐ Mechanical Specification						Test Site		Wafer Fab Material				
☐ Packing/Shipping/Labeling						Test Proces	SS		Wafer	· Fal	b Process	

## **Description of Change:**

Texas Instruments is pleased to announce the qualification of its LFAB fabrication facility as an additional Wafer Fab source and CD-PR as additional probe site options for the selected devices listed in the "Product Affected" section.

	Current Fa	b/Probe Sit	:e	Additional Fab/Probe Sites				
Current Fab Site	Fab Process	Probe Site	Wafer Diameter	Additional Fab Site	Fab Process	Probe Site	Wafer Diameter	
UMC12i	F65	CLARK-PR	300mm	LFAB	F65	CD-PR	300mm	

Test coverage, insertions, conditions will remain consistent with current testing.

## **Reason for Change:**

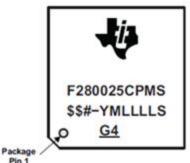
Continuity of supply

## Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):

None

# **Changes to product identification resulting from this PCN:**

# **Device Symbol:**



YMLLLLS = Lot Trace Code

YM = 2-Digit Year/Month Code

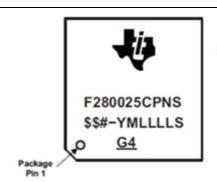
LLLL = Assembly Lot

S = Assembly Site Code

\$\$ = Wafer Fab Code (one or two characters) as applicable

# = Silicon Revision Code

G4 = Green (Low Halogen and RoHS-compliant)



YMLLLLS = Lot Trace Code

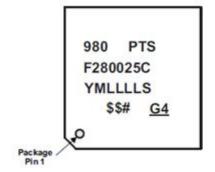
YM = 2-Digit Year/Month Code

LLLL = Assembly Lot S = Assembly Site Code

\$\$ = Wafer Fab Code (one or two characters) as applicable

# = Silicon Revision Code

G4 = Green (Low Halogen and RoHS-compliant)



YMLLLLS = Lot Trace Code

YM = 2-Digit Year/Month Code

LLLL = Assembly Lot S = Assembly Site Code 980 = TI E.I.A. Code

\$\$ = Wafer Fab Code (one or two characters) as applicable

# = Silicon Revision Code

G4 = Green (Low Halogen and RoHS-compliant)

## Original Fab Field:

 $$$ = $7 \rightarrow UMC 12i$ 

#### Updated Fab Field:

 $$$ = $7 \rightarrow UMC 12i$ 

Or

 $$$ = 3L \rightarrow LFAB$ 

#### **Current Fab Site Information:**

Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City
UMC 12i	UMI	SGP	Singapore

## **Additional Fab Site Information:**

	•	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	
ı	LFAB	LHI	USA	Lehi

Sample product shipping label (not actual product label)





(1P) SN74LS07NSR

(D) 0336 (31T)LOT: 3959047MLA (4W) TKY(1T) 7523483SI2

(2P) REV: (V) 0033317 (20L) 650: SHE (21L) CCO-USA (22L) ASO: MLA 23L) ACO: MYS

#### **Product Affected:**

F280021PTQR	F280023PTQR	F280025CPTQR	F280025PTQR
F280023PMQR	F280025CPMQR	F280025PMQR	SB280025PNQR
F280023PNQR	F280025CPNQR	F280025PNQR	

## Qualification Results

# Data Displayed as: Number of lots / Total sample size / Total failed

Туре	#	Test Spec	Min Lot Qty	SS/ Lot	Test Name	Condition	Duration	Qual Device: <u>F280025CPNQR</u>	QBS Reference: TMS320F28379SPTPQ		
Test Group	Test Group A - Accelerated Environment Stress Tests										
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL3 260C	-	-QBS	3/363/0		
HAST	A2	JEDEC JESD22- A110	3	77	Biased HAST	110C/85%RH	264 Hours	-QBS	3/231/0		
AC/UHAST	A3	JEDEC JESD22- A102/JEDEC JESD22-A118	3	77	Unbiased HAST	130C/85%RH	96 Hours	-QBS	3/231/0		
тс	A4	JEDEC JESD22- A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	-QBS	3/231/0		
TC-BP	A4	MIL-STD883 Method 2011	1	5	Post Temp Cycle Bond Pull	-	-	-QBS	1/5/0		
HTSL	A6	JEDEC JESD22- A103	1	45	High Temperature Storage Life	150C	1000 Hours	-QBS	3/135/0		
Test Group	B - Acce	elerated Lifetime Simula	tion Test	s							
HTOL	B1	JEDEC JESD22- A108	3	77	Life Test	125C	1000 Hours	1/77/0	3/231/0		
ELFR	B2	AEC Q100-008	3	77	Early Life Failure Rate	125C	48 Hours	-QBS	3/2400/0		
EDR B3	В3	AEC Q100-005	3	77	NVM Endurance, Data Retention, and Operational Life	150C	1000 hours	-QBS	3/231/0		
Test Group	C - Pack	cage Assembly Integrity	Tests								
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	-QBS	3/90/0		

Туре	#	Test Spec	Min Lot Qty	SS/ Lot	Test Name	Condition	Duration	Qual Device: F280025CPNQR	QBS Reference: TMS320F28379SPTPQ	
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	-QBS	3/90/0	
Test Group D - Die Fabrication Reliability Tests										
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	
TDDB	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	
NBTI	D4	-	-	-	Negative Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	
Test Group	E - Elect	rical Verification Tests								
ESD	E2	AEC Q100-002	1	3	ESD HBM	-	2000 Volts	1/3/0	1/3/0	
ESD	E3	AEC Q100-011	1	3	ESD CDM	-	750 Volts	1/3/0	1/3/0	
LU	E4	AEC Q100-004	1	6	Latch-Up	Per AEC Q100-004	-	1/6/0	1/6/0	
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	3/90/0	3/90/0	
Additional	Tests									

- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
- The following are equivalent HTOL options based on an activation energy of 0.7eV: 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
- The following are equivalent HTSL options based on an activation energy of 0.7eV: 150C/1k Hours, and 170C/420 Hours
- The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles
- Flash memory was programmed and Erased to 20,000 times for B1 and B2 tests

Ambient Operating Temperature by Automotive Grade Level:

- Grade 0 (or E): -40C to +150C
- Grade 1 (or Q): -40C to +125C
- Grade 2 (or T): -40C to +105C
- Grade 3 (or I) : -40C to +85C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

- Room/Hot/Cold : HTOL, ED
- Room/Hot: THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
- Room : AC/uHAST

Quality and Environmental data is available at TI's external Web site: http://www.ti.com/

TI Qualification ID: R-CHG-2206-089

[1]-1 unit passed 25C (Q100 requirement) marginal failure at 125C. Appears to be tester repeatability and unrelated to stress test. Refer to QEM-EVAL-2211-00276

#### **ZVEI ID:** SEM-PW-13, SEM-TF-01

For questions regarding this notice, e-mails can be sent to the Change Management team or your local Field Sales Representative.

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