

17052469 EFM8 BB3 and EFM8 LB1 datasheet update bulletin

Bulletin Issue Date: 5/24/2017 Effective Date: 5/24/2017

Description of Change

Silicon Labs is pleased to announce the release of version 1.1 of the EFM8 Busy Bee 3 or BB3 and EFM8 Laser Bee 1 or LB1 datasheets.

The changes to the EFM8 BB3 datasheet are as follows:

- -Added table 4.12 for the 1.8V LDO Internal Regulator specifying the min, max, and typical values.
- -Added a note to table 4.9 ADC indicating that product test uses a 2.4 V external reference and external ground.
- -Added Output Voltage and Output Current specifications to DAC table 4.13.
- -Updated the wording in the feature list paragraph on page 1 to clarify which packages are offered in commercial grade, industrial grade, and automotive grade.
- -Added a note in the introduction pointing to the reference manual where specific block level information can be found.
- -The typo which incorrectly stated the application note number on page 34, section 5.2 has been corrected.
- -Adjusted the Data Hold Time in table 4.17 for the SMBus peripheral in standard master mode from 0 µs to 275 ns.
- -Adjusted the Data Hold Time in table 4.17 for the SMBus peripheral in fast master mode from 0 µs to 275 ns.
- -Adjusted the Data Setup Time in table 4.17 for the SMBus peripheral in standard master mode from 4.7 µs to 300 ns.
- -Adjusted the Data Setup Time in table 4.17 for the SMBus peripheral in fast master mode from 1.3 µs to 300 ns.
- -Added a note outlining the use of the DLYEXT bit which can be used to adjust the SMBus Data Setup and Data Hold times.
- -Updated the minimum Vio labeled in Figure 5.2 to match the recommended operating conditions.

The changes to the EFM8 LB1 datasheet are as follows

- -Removed a note that AEC-Q100 qualification was pending for these devices.
- -Added table 4.12 for the 1.8V LDO Internal Regulator specifying the min, max, and typical values.
- -Added a note to table 4.9 ADC indicating that product test uses a 2.4 V external reference and external ground.
- -Added Output Voltage and Output Current specifications to DAC table 4.13.
- -Adjusted the Data Hold Time in table 4.17 for the SMBus peripheral in standard master mode from 0 μs to 275 ns.
- -Adjusted the Data Hold Time in table 4.17 for the SMBus peripheral in fast master mode from 0 µs to 275 ns.
- -Adjusted the Data Setup Time in table 4.17 for the SMBus peripheral in standard master mode from 4.7 µs to 300 ns.
- -Adjusted the Data Setup Time in table 4.17 for the SMBus peripheral in fast master mode from 1.3 us to 300 ns.
- -Added a note outlining the use of the DLYEXT bit which can be used to adjust the SMBus Data Setup and Data Hold times.
- -Updated the minimum Vio labeled in Figure 5.2 to match the recommended operating conditions.
- -Added a note in the introduction pointing to the reference manual where specific block level information can be found.
- -The typo which incorrectly stated the application note number on page 33, section 5.2 has been corrected.

Reason for Change

Release of version 1.1 of the EFM8 BB3 and EFM8 LB1 datasheets.

Product Identification

Existing Part #
EFM8LB10F16E-B-QFN24
EFM8LB10F16E-B-QFN24R
EFM8LB10F16E-B-QFN32
EFM8LB10F16E-B-QFN32R

EFM8LB10F16E-B-QFP32 EFM8LB10F16E-B-QFP32R

EFM8LB10F16ES0-B-QFN24 EFM8LB10F16ES0-B-QFN24R

EFM8LB10F16ES0-B-QFN24R EFM8LB10F16ES0-B-QFN32

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EFM8LB10F16E-B-QSOP24

EFM8LB10F16E-B-QSOP24R

EFM8LB11F16E-B-QFN24

EFM8LB11F16E-B-QFN24R

EFM8LB11F16E-B-QFN32

EFM8LB11F16E-B-QFN32R

EFM8LB11F16E-B-QFP32

EFM8LB11F16E-B-QFP32R

EFM8LB11F16ES0-B-QFN24

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EFM8LB11F16ES0-B-QFN32R

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EFM8LB12F32E-B-QSOP24

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EFM8LB12F64ES0-B-QFN32R

EFM8LB12F64E-B-QSOP24

EFM8LB12F64E-B-OSOP24R

EFM8BB31F16G-B-QFN24 EFM8BB31F16G-B-QFN24R

EFM8BB31F16G-B-QFN32

EFM8BB31F16G-B-QFN32R

EFM8BB31F16G-B-QFP32

EFM8BB31F16G-B-QFP32R

EFM8BB31F16G-B-QSOP24

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EFM8BB31F16I-B-QFN24

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This change is considered a minor change which does not affect form, fit, function, quality, or reliability. The information is being provided as a cusomer courtesy.

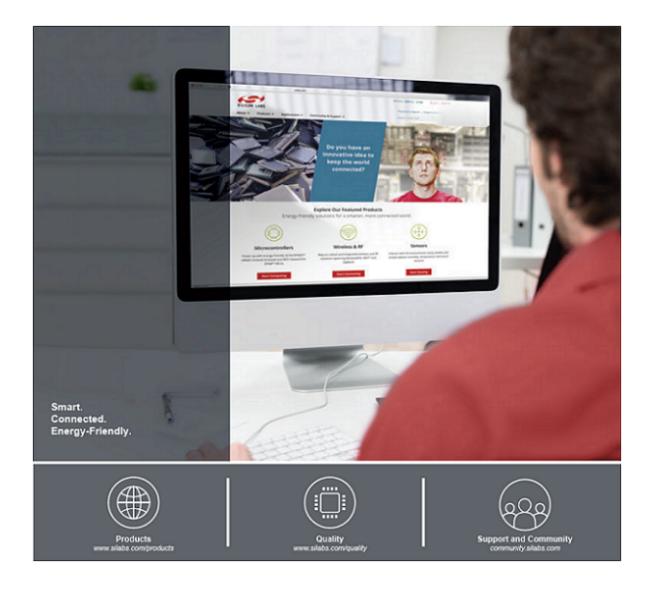
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