PIC32MZ Graphics (DA) Family
Silicon Errata and Data Sheet Clarification

The PIC32MZ Graphics (DA) family of devices that you have received conform functionally to the current Device Data Sheet (DS60001361**H**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. If applicable, any silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC32MZ Graphics (DA) family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table (if applicable) apply to the current silicon revision (**A1**).

Data Sheet clarifications and corrections (if applicable) start on page 20.

The silicon revision level can be identified using the current version of MPLAB® X IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB X IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB X IDE project.
3. Configure the MPLAB X IDE project for the appropriate device and hardware debugger.
4. Select *Window* > *Dashboard*, and then click the **Refresh Debug Tool Status** icon ( ).
5. The part number and the Device and Revision ID values appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various PIC32MZ Graphics (DA) family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)
		A1
PIC32MZ1025DAA169	0x05F0C053	0x1
PIC32MZ1025DAB169	0x05F0D053	
PIC32MZ1064DAA169	0x05F0F053	
PIC32MZ1064DAB169	0x05F10053	
PIC32MZ2025DAA169	0x05F15053	
PIC32MZ2025DAB169	0x05F16053	
PIC32MZ2064DAA169	0x05F18053	
PIC32MZ2064DAB169	0x05F19053	
PIC32MZ1025DAG169	0x05F42053	
PIC32MZ1025DAH169	0x05F43053	
PIC32MZ1064DAG169	0x05F45053	
PIC32MZ1064DAH169	0x05F46053	
PIC32MZ2025DAG169	0x05F4B053	
PIC32MZ2025DAH169	0x05F4C053	
PIC32MZ2064DAG169	0x05F4E053	
PIC32MZ2064DAH169	0x05F4F053	

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001361**H**) for detailed information on Device and Revision IDs for your specific device.

TABLE 1: SILICON DEVREV VALUES (CONTINUED)

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)
		A1
PIC32MZ1025DAA176	0x05F78053	0x1
PIC32MZ1025DAB176	0x05F79053	
PIC32MZ1064DAA176	0x05F7B053	
PIC32MZ1064DAB176	0x05F7C053	
PIC32MZ2025DAA176	0x05F81053	
PIC32MZ2025DAB176	0x05F82053	
PIC32MZ2064DAA176	0x05F84053	
PIC32MZ2064DAB176	0x05F85053	
PIC32MZ1025DAG176	0x05FAE053	
PIC32MZ1025DAH176	0x05FAF053	
PIC32MZ1064DAG176	0x05FB1053	
PIC32MZ1064DAH176	0x05FB2053	
PIC32MZ2025DAG176	0x05FB7053	
PIC32MZ2025DAH176	0x05FB8053	
PIC32MZ2064DAG176	0x05FBA053	
PIC32MZ2064DAH176	0x05FBB053	
PIC32MZ1025DAA288	0x05F5D053	0x1
PIC32MZ1025DAB288	0x05F5E053	
PIC32MZ1064DAA288	0x05F60053	
PIC32MZ1064DAB288	0x05F61053	
PIC32MZ2025DAA288	0x05F66053	
PIC32MZ2025DAB288	0x05F67053	
PIC32MZ2064DAA288	0x05F69053	
PIC32MZ2064DAB288	0x05F6A053	

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001361**H**) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item	Issue Summary	Affected Revisions(1)
				A1
Primary Oscillator	Primary Oscillator Crystal	1.	The Primary Oscillator (POSC) has been tested in a normal power-up sequence and supports specific crystal operation.	X
Secondary Oscillator	Secondary Oscillator Crystal	2.	The Secondary Oscillator (SOSC) does not support crystal operation.	X
Reset	BOR	3.	A system Reset is not generated on a BOR event (VPORIO < VDDIO < VBORIO). This will stop system clocks with all the I/O pin functions frozen in the present state until either VDDIO falls to VPORIO or VDDIO > VBORIO.	X
Reset	HVD Reset	4.	A BOR event also sets the HVD1V8R (RCON<29>) bit.	X
Power-Saving	PMD Bits	5.	Turning off the REFCLK modules through the PMD (PMD6<11:8>) bits causes unpredictable device behavior.	X
DMA	PMD Bits	6.	Setting the PMD bit for DMA (PMD7<4>) does not disable clocks to the DMA peripheral.	X
VBAT	—	7.	VBAT is not functional.	X
Deep Sleep	—	8.	Deep Sleep mode is not functional.	X
I^2C	—	9.	The I^2C module does not function reliably under certain conditions.	X
ADC	Interrupts	10.	ADC Group Early Interrupt is not functional (IRQ205).	X
ADC	Level Trigger	11.	ADC level trigger will not perform burst conversions in debug mode.	X
ADC	DNL	12.	In Differential mode, code 3072 is not within the specification.	X
ADC	Turbo Mode	13.	Turbo mode is not functional.	X
SDHC	Clock	14.	The SDHC module requires System PLL to be turned ON.	X
SDHC	Clock Stability	15.	The SDHC module may not function if the $\overline{SDCD}$ pin is not used.	X
SDHC	Card Detect Status	16.	Card detect status indication through the CDSLVL bit (SDHCSTAT1<18>) is inverted.	X
SDHC	Write Protect Status	17.	Write protect status indication through the WPSLVL bit (SDHCSTAT1<19>) is inverted.	X
SDHC	Stop at Block Gap	18.	The Stop at Block Gap feature of the SDHC module is not functional.	X
HLVD	—	19.	High/Low-Voltage Detect module is not functional.	X
DDR2C	—	20.	DDR2 is functional only between 0°C and 70°C.	X
DDR2C	Internal DDRVREF Circuit	21.	Internal DDRVREF circuit is not functional.	X
SQI	XIP Mode	22.	SQI XIP mode is not functional in cached memory space (KSEG2).	X
USB	Interrupt	23.	The USB General Event Interrupt (IRQ 132) is not persistent.	X
USB	Resume	24.	The USB module does not support remote wake-up.	X
System Bus	Writes	25.	The EERP bit (SBTxECON<24>) is not functional.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item	Issue Summary	Affected Revisions(1)
				A1
Crypto	Flash Data Access	26.	The Crypto module cannot access data from Flash.	X
UART	Overflow	27.	Clearing the OERR bit (UxSTA<1>) clears the receiver buffer.	X
EBI	Chip Select	28.	For Asynchronous NOR Flash, EBI internal clock specification, TEBICLK (EB10), is not met.	X
CTMU	Triggers	29.	Edge Sequencing mode (EDGSEQEN(CTMUCON<10>)) and Edge modes are not functional.	X
CTMU	TGEN	30.	When the TGEN bit is set, manual current sourcing from CTMU is not possible.	X
Temperature Sensor	—	31.	The temperature sensor does not function.	X
ICSP	TDO	32.	While programming on any ICSP PGECx/PGEDx pair, the TDO pin will toggle.	X
PORTS	VIH Electrical Specification	33.	The VIH specification of 0.65 * VDDIO is not met.	X
Primary Oscillator	Automatic Gain Control (AGC)	34.	The Primary Oscillator Automatic Gain Control (AGC) is not functional.	X
Primary Oscillator	Automatic Gain Control (AGC)	35.	The Primary Oscillator AGC Gain Search Step Settling Time Control bits are not functional.	X
Primary Oscillator	Primary Oscillator Fine Gain Control	36.	The Primary Oscillator Fine Gain Control bits are not functional.	X
GPU	GPURESET bit	37.	The GPU Run-time enable/Disable feature is not functional.	X
SDHC	SDWPPOL bit	38.	The SDHC Write-protect Polarity Inversion feature is not functional.	X
PMP	Status Flags	39.	The PMP input buffer full flag, IB0F, and the output buffer underflow, OBUF, are getting set as soon as the PMP module is enabled in Client mode (PMPTTL bit (PMCON<10>) is equal to '1').	X
I^2C	Start/Restart	40.	When the I^2C module is in Client mode, Start and Restart interrupts are not functional.	X
Crypto	Partial Packet	41.	The Crypto Engine does not support partial packet processing.	X
Crypto	Zero-length Packet	42.	The Crypto Engine does not support a Hash operation on an empty string.	X
CTMU	Idle	43.	CTMU current source is not enabled in Idle mode (CTMUSIDL bit in the CTMUCON register is equal to '1'), which prevents ADC if enabled in Idle mode from being able to measure the CTMU temperature sensor.	X
Timer1	Asynchronous Counter	44.	Timer1 in Asynchronous External Counter mode does not reflect the first count from an external T1CK input.	X
Timer1	TMR1 Register	45.	TMR1 register of Timer1 in Asynchronous mode remains at initial set value for five external clock pulses after wake-up from Sleep mode.	X
Timer1	Asynchronous Mode	46.	Timer1 counts beyond the period value in Asynchronous mode when the period is 0x01.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item	Issue Summary	Affected Revisions(1)
				A1
Timer1	Gated Mode	47.	Timer1 does not work properly in Gated mode with prescaler enabled.	X
Timer1	TMR1 Register Writes	48.	Back-to-back writes to the TMR1 register are not allowed for four PBCLK cycles.	X
Timer1	Asynchronous Timer1	49.	The Asynchronous Timer Write Disable bit, TWDIS (TxCON<12>), and the Asynchronous Timer Write in Progress bit, TWIP (TxCON<11>), are non-functional.	X
UART	High-Speed Mode	50.	The UART Stop bit duration is shorter than expected in High-Speed mode (UxMODE.BRGH =1) for baud rates less than 7.5 Mbps.	X
Sleep	IPD	51.	3 mA increase in sleep current when PB5DIV is disabled.	X
CFG	Unique ID	52.	Unique ID is not programmed on devices which are released earlier than trace code dated 1821xxx.	X
EBI	EBIRDYx pin as GPIO	53.	The EBIRDYEN1 bit (CFGEBIC<25>), EBIRDYEN2 bit (CFGEBIC<26>), EBIRDYEN3 bit(CFGEBIC<27>) are not functional and always set to '1'.	X
I^2C	I^2C Client	54.	The 7-bit address that matches the 10-bit upper address value (111_10xx) is not accepted regardless of the STRICT bit setting.	X
I^2C	Speed	55.	I^2C module does not meet low period of the SCL clock (tLOW) parameter from I^2C specification for clock frequency >= 400 kHz.	X
Input Capture	Debug	56.	Debug breakpoints are not supported when using Input Capture with DMA.	X
SDHC	MMC	57.	Data from the MMC card can not be read correctly when the block size is set smaller than 512 bytes.	X
Sleep	Wake-up	58.	Multiple sleep attempts which occur before the CPU has fully awakened, may stall the CPU until the next reset event.	X
SPI	Block Transmission	59.	At the end of a transmission, the SRMT bit can indicate the completion of the transmission for one PBCLK even though the transmission has one block remaining.	X
SQI	Special Functions Registers	60.	The CPU stalls if the SQI Special Function Registers are read before the REFCLKO2 clock is enabled.	X
Timer2-9	Match	61.	If timer match coincides with entry into sleep mode, timer event triggers and interrupt may not occur.	X
Timer2-9	Match	62.	If timer match coincides with entry into Idle mode, timer event triggers and interrupt may not occur.	X
Timer2-9	Debug	63.	On a debug breakpoint, TMRx register, x=2-9, may not be representative of the correct value.	X
USB	LPM	64.	The USB Link Power Management (LPM) feature is not functional.	X
USB	Host Resume	65.	The USB Host module does not send correct resume signal on the USB bus on subsequent suspend/resume sequences.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item	Issue Summary	Affected Revisions(1)
				A1
USB	Host Disconnect Detection	66.	The USB Host module does not wake up CPU from sleep when a USB device is disconnected.	X
USB	Suspend/ Resume IRQ	67.	USB Suspend/Resume Event through IRQ 103 is not functional.	X
System	Clock	68.	CPU can lockup when SYSCLK and PBCLK7 clock frequencies are different. SYSCLK and PBCLK7 must use same clock frequency (i.e., PBDIV (PB7DIV<6:0>) =0) to prevent system lockups.	X
ADC	External VREF-	69.	Excessive current flows through the VREF- pin when external voltage reference is used, and voltage on the VREF- pin is greater than AVSS.	X
USB	FIFO	70.	Writing '1' to the FLUSH bit (USBIENCSRx<19>, where x = 1-7) does not flush the TX FIFO and reset the TX FIFO pointer.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A1**).

1. Module: Primary Oscillator

The POSC has been tested in a normal power-up sequence and supports specific crystal operation.

Work around 1

The Primary Oscillator (POSC) has been characterized to operate at 8 MHz and 12 MHz when the circuit shown in Figure 1 is implemented, and the operating conditions listed in Table 3 are met.

Work around 2

Alternatively, use an external clock or Internal FRC Oscillator. Note that communication interfaces (DDR2, USB, etc.,) with tighter clock accuracy requirements will not function with the FRC as clock source.

FIGURE 1: POSC CRYSTAL CIRCUIT

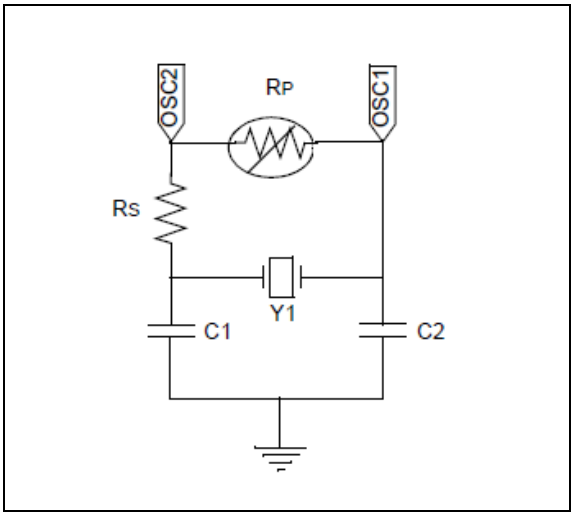

TABLE 3: CRYSTAL SPECIFICATION

Crystal Frequency (See Note 1)	Series Resistor RS	POSC Gain Setting POSCGAIN<1:0> (DEVCFG0<20:19>	POSC Boost Setting POSCBOOST (DEVCFG0<21>
8 MHz	2 kΩ	'0b00 (GAIN_0)	'0b1
12 MHz	1 kΩ	'0b00 (GAIN_0)	'0b1

Note 1: Using any other crystal frequency will require special component selection and characterization.

2: A parallel register (RP) should not be used to increase the gain of the POSC.

Affected Silicon Revisions

A1							
X							

2. Module: Secondary Oscillator

A crystal oscillator cannot be used as the input to the Secondary Oscillator (SOSC) pins: SOSCI and SOSCO.

Work around

Use an external clock source (32.768 Hz) applied to the SOSCO pin with the FSOSCEN bit (DEVCFG1<6>) set to '0' (i.e., the SOSC is disabled through the Configuration Word) for a real-time clock base; otherwise, use the internal LPRC for non-precision requirements.

Affected Silicon Revisions

A1							
X							

3. Module: Reset

A system Reset is not generated on a BOR event (V_{PORIO} < V_{DDIO} < V_{BORIO}). This will stop system clocks with all the I/O pin functions frozen in the present state until either V_{DDIO} falls to V_{PORIO} or V_{DDIO} > V_{BORIO}.

Work around

Reset device using a $\overline{MCLR}$ pin through an external reset supervisor/monitor is shown in Figure 2. Set the SMCLR (DEVCFG2<15>) configuration bit to '0', which makes the $\overline{MCLR}$ to act as a POR Reset instead of a normal system reset.

Table 4 and Table 5 provide a list of external Reset supervisor and regulators with built in Reset supervisors that can be used.

When selecting an external supervisor other than the ones provided in Table 4 and Table 5, the following requirements must be taken into consideration:

- Minimum Reset trip voltage of the external supervisor should be V_{BORIO} (Max)+0.5V.
- The external reset supervisor/LDO output going to $\overline{MCLR}$ should have an open drain output to not interfere with the MPLAB programming/debug tools.

When this work around is implemented, the minimum V_{DDIO} operating voltage of the application needs to be above the reset supervisor maximum trip voltage + 0.2V, where 0.2V compensates for variation in the external reset supervisor voltage.

FIGURE 2: EXTERNAL RESET CIRCUIT

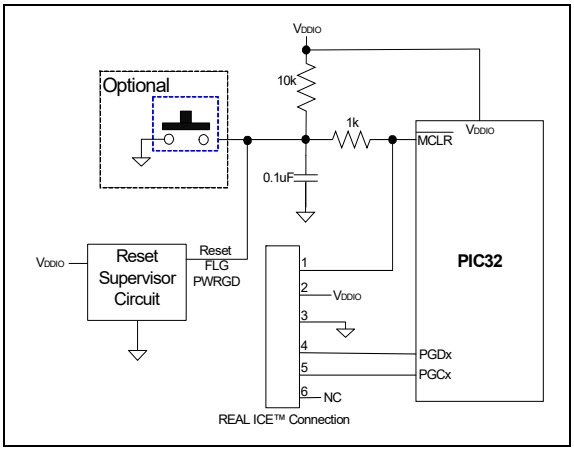

TABLE 4: RESET SUPERVISOR/ VOLTAGE MONITOR

Part Number	Reset Trip Voltage	$\overline{MCLR}$ Source
MIC803-26D2VC3	2.63V	Reset pin (Open Drain)

TABLE 5: LDOs WITH EMBEDDED RESET SUPERVISOR

Part Number	V_{IN} (Max)	V_{OUT}	I_{OUT}	Reset Trip Voltage	$\overline{MCLR}$ Source
MIC5239-3.3YM	30V	3.3V	500 ma	3.3V- 5%	FLG pin (Open Drain)
MIC5239-3.3YMM					
MCP1725-3302E/MC	6V	3.3V	500 ma	3.3V-10%	PWRGD pin (Open Drain)
MCP1727-3302E/MF	6V	3.3V	1500 ma	3.3V-10%	PWRGD pin (Open Drain)

Affected Silicon Revisions

A1							
X							

4. Module: Reset

A BOR event also sets the HVD1V8R bit (RCON<29>).

Work around

True high-voltage detect will set only the HVD1V8R (RCON<29>) bit. This bit should be ignored when it is set along with the BOR (RCON<1>) bit. Also, make sure to clear the HVD1V8R bit on exit from the BOR event, if set.

Affected Silicon Revisions

A1							
X							

5. Module: Power-Saving

Turning off the REFCLK modules through the PMD bits (PMD6<11:8>) causes unpredictable device behavior.

Work around

None. Do not disable the REFCLK modules through the PMD bits.

Affected Silicon Revisions

A1							
X							

6. Module: DMA

Setting the PMD bit for DMA (PMD7<4>) does not disable clocks to the DMA peripheral.

Work around

Use the ON bit (DMACON<15>) to enable/disable DMA globally, or use the CHEN bit (DCHxCON<7>) to enable/disable individual channels.

Affected Silicon Revisions

A1							
X							

7. Module: VBAT

The VBAT pin is not functional. Connect the VBAT pin to VDDIO.

Work around

None.

Affected Silicon Revisions

A1							
X							

8. Module: Deep Sleep

Deep Sleep mode is not functional.

Work around

None.

Affected Silicon Revisions

A1							
X							

9. Module: I^2C

Indeterminate I^2C module behavior may result when data rates greater than 100 kHz and/or continuous sequential data transfers greater than 500 bytes are used.

The potential false intermittent error signals can result in one of the following error conditions, which are listed in order of decreasing frequency:

- **False Error Condition 1:**
  False Host Bus Collision Detect (Host-mode only) – The error is indicated through the BCL bit (I2CxSTAT<10>).
- **False Error Condition 2:**
  Receive Overflow (Host or Client modes) – The error is indicated through the I2COV bit (I2CxSTAT<20>).
- **False Error Condition 3:**
  Suspended I^2C Module Operations (Host or Client modes) – I^2C transactions in progress are inadvertently suspended without error indications.

Note: All three false errors are recoverable in software.

Work around 1

- **False Error Condition 1:**
  Clear the Host Bus Collision Detect (BCL bit (I2CxSTAT<10>) after the bus returns to an Idle state. The software can monitor the S bit (I2CxSTAT<3>) and the P (I2CxSTAT<4>) bit to wait for an Idle bus. When the software services the bus collision Interrupt Service Routine and the I^2C bus is free, the software can resume communication by asserting a new Start condition.
- **False Error Condition 2:**
  Clear the Receive Overflow Status flag I2COV bit (I2CxSTAT<20>), and then resume normal operation.
- **False Error Condition 3:**
  Initialize a Timer to slightly greater than the worst case I^2C transaction cycle, (i.e., from Start-to-Stop, including the sum of all other application PC flow latencies, calls, interrupts, etc.). Exact timing is not required, rather just long enough so that a normal transaction is not interrupted. Prior to the beginning of each transaction, start the timer. Be sure to stop and reset the timer after completion of each successful I^2C transaction.
  During the Timer interrupt (i.e., the I^2C transaction has timed out), disable the I^2C module by setting the ON bit (I2CxCON<15>) = 0. After disabling the module, wait 4 instruction cycles, after which time the I2CxSTAT register will automatically be cleared. Re-enable the I^2C module by setting the ON bit = 1 and resume normal operation.

Work around 2

Instead of using the hardware I^2C module, use a software “bit-bang” implementation.

Affected Silicon Revisions

A1							
X							

10. Module: ADC

The ADC Group Early Interrupt (IRQ 205) feature is not functional.

Work around

Use individual ADC Early Interrupts (IRQ 119 through IRQ 203 and IRQ 206).

Affected Silicon Revisions

A1							
X							

11. Module: ADC

The ADC level trigger will not perform burst conversions in Debug mode.

Work around

Do not use Debug mode with the ADC level trigger.

Affected Silicon Revisions

A1							
X							

12. Module: ADC

In Differential mode, code 3072 has a DNL of +3.

Work around

None.

Affected Silicon Revisions

A1							
X							

13. Module: ADC

Turbo mode is not functional when two channels are linked for the purpose of increasing throughput.

Work around

None.

Affected Silicon Revisions

A1							
X							

14. Module: SDHC

The SDHC module requires the System PLL to be turned ON.

Work around

SPLL should be enabled before using the SD Host Controller (SDHC) module.

Affected Silicon Revisions

A1							
X							

15. Module: SDHC

The SDHC module may not function if the $\overline{\text{SDCD}}$ pin is not used.

Work around 1

Set CDSSEL (SDHCCON1<7>) to '1' and CDTLVL (SDHCCON1<6>) to '0'.

Work around 2

Ensure that the $\overline{\text{SDCD}}$ pin is used and driven to a low state externally.

Affected Silicon Revisions

A1							
X							

16. Module: SDHC

Card-detect status indication through the CDSLVL bit (SDHCSTAT1<18>) is inverted.

Work around 1

Use ACMD42 to detect the card's presence.

Work around 2

If $\overline{\text{SDCD}}$ is used for card detect, add a software work around to invert the CDSLVL (SDHCSTAT1<18>) state.

Affected Silicon Revisions

A1							
X							

17. Module: SDHC

Write-protect status indication through the WPSLVL bit (SDHCSTAT1<19>) is inverted.

Work around

If $\overline{\text{SDWP}}$ is used for Write-protect, add a software work around to invert WPSLVL (SDHCSTAT1<19>) state.

Affected Silicon Revisions

A1							
X							

18. Module: SDHC

The Stop at Block Gap feature of the SDHC module is not functional.

Work around

None.

Affected Silicon Revisions

A1							
X							

19. Module: HLVD

High/Low-Voltage Detect module is not functional.

Work around

None.

Affected Silicon Revisions

A1							
X							

20. Module: DDR2C

DDR2 is functional only between 0°C and 70°C.

Work around

None.

Affected Silicon Revisions

A1							
X							

21. Module: DDR2C

Internal DDRV$_{REF}$ circuit (voltage divider) is not functional.

Work around

Use external voltage divider circuit on the DDRV$_{REF}$ pin to track V$_{DDR1V8}$/2. Make sure to set INTVREFCON<1:0> (CFGMPLL<7:6>) to `0'b00` before initializing DDR2.

Affected Silicon Revisions

A1							
X							

22. Module: SQI

SQI eXecute-In-Place (XIP) mode is not functional in cached memory space (KSEG2).

Work around

Use KSEG3 (uncached starts at 0xF0000000) address space to access SQI Flash in XIP mode.

Affected Silicon Revisions

A1							
X							

23. Module: USB

The USB General Event Interrupt (IRQ 132) is not persistent as expected. The module is not guaranteed to generate interrupts for USB bus events when a USB interrupt is already being processed.

Work around

Upon entering the Interrupt Service Routine, continue to process all USB module events till the USBIF bit in the USBCRCON register (USBCRCON<26>) is cleared by the hardware.

Affected Silicon Revisions

A1							
X							

24. Module: USB

The USB module does not support remote wake-up through the USBRIE bit (USBCRCON<1>).

Work around

None.

Affected Silicon Revisions

A1							
X							

25. Module: System Bus

The ERRP (SBTxECON<24>) bit is not functional and should not be used.

Work around

None.

Affected Silicon Revisions

A1							
X							

26. Module: Crypto

The Crypto module cannot access data from Flash due to prefetch cache corruption. Both work arounds listed below do not impact CPU performance when L1 cache is used by CPU.

Work around 1

Disable predictive prefetching for all addresses except CPU instructions and data. This can be achieved by NOT setting PREFEN<1:0> (PRECON<5:4>) to `0'b11`.

Work around 2

Set Flash Wait states using the PFMWS<2:0> bits (PRECON<2:0>) to greater than four.

Affected Silicon Revisions

A1							
X							

27. Module: UART

Clearing the receive buffer overrun error through the OERR bit (UxSTA<1>) clears the receive buffer. This condition occurs when the RUNOVF bit (UxMODE<16>) is set, and an overflow condition occurs.

Work around

When a receive buffer overrun error occurs, read the entire receive FIFO through the UxRXREG register before clearing the OERR (UxSTA<1>) bit.

Affected Silicon Revisions

A1							
X							

28. Module: EBI

For Asynchronous NOR Flash, EBI internal clock specification, TEBICLK (EB10) is not met.

Work around

When asynchronous NOR is attached to EBI, the system frequency would have to be reduced to 180 MHz for it to properly function.

Affected Silicon Revisions

A1							
X							

29. Module: CTMU

Edge Sequencing mode (EDGSEQEN (CTMUCON<10>)) and Edge mode are not functional.

Work around

Use level modes.

Affected Silicon Revisions

A1							
X							

30. Module: CTMU

When the TGEN bit is set, manual current sourcing (i.e. setting the EDG1STAT bit) from CTMU is not possible.

Work around

None.

Affected Silicon Revisions

A1							
X							

31. Module: Temperature Sensor

The temperature sensor is not functional.

Work around

None.

Affected Silicon Revisions

A1							
X							

32. Module: ICSP

While programming/debugging the device through any PGECx/PGEDx pair, TDO will toggle.

Work around

None.

Affected Silicon Revisions

A1							
X							

33. Module: PORTS

VIH specification of 0.65 * VDDIO is not met. Use VIH specification of 0.8 * VDDIO.

Work around

None.

Affected Silicon Revisions

A1							
X							

34. Module: Primary Oscillator

The Primary Oscillator (POSC) does not support Automatic Gain Control (AGC). Therefore, the POSCAGC bit (DEVCFG0/ADEVCFG0<27>) is not functional.

Work around

None.

Affected Silicon Revisions

A1							
X							

35. Module: Primary Oscillator

The Primary Oscillator (POSC) does not support Automatic Gain Control (AGC). Therefore, the Primary Oscillator AGC Gain Search Step Settling Time Control bits, POSCAGCDLY<1:0> (DEVCFG0/ADEVCFG0<25:24>), are not functional.

Work around

None.

Affected Silicon Revisions

A1							
X							

36. Module: Primary Oscillator

The Fine Gain Control bits, POSCFGAIN<1:0> (DEVCFG0/ADEVCFG0<23-22>), are not functional.

Work around

None.

Affected Silicon Revisions

A1							
X							

37. Module: GPU

The GPU Run-time enable/disable feature is not functional. Therefore, the GPURESET bit (CFGCON2<0>) is not functional. The GPU is always enabled regardless of the value of the GPURESET bit.

Work around

None.

Affected Silicon Revisions

A1							
X							

38. Module: SDHC

The SDHC write-protect polarity inversion feature is not functional. Therefore, the SDWPPOL bit (CFGCON2<2>) is not functional and should not be used.

Work around

None.

Affected Silicon Revisions

A1							
X							

39. Module: PMP

The PMP Input Buffer 'x' Status Full bit, IB0F (PMSTAT<8>), and the Output Buffer Underflow Status bit, OBUF (PMSTAT<6>), are set as soon as the PMP is turned ON in Client mode (i.e., PMPTTL bit (PMCON<10>) is equal to '1').

Work around

During PMP slave mode initialization, and before PMP interrupts are enabled, clear the Input Buffer Full Flag (IB0F bit (PMSTAT<8>) and the Output Buffer Underflow Flag (OBUF bit (PMSTAT<6>) when clearing any pending IFSx interrupt flags.

Affected Silicon Revisions

A1							
X							

40. Module: I²C

When the I²C module is in Client mode, Start and Restart Interrupts are not occurring or properly reflected in the IFSx flag bits.

Work around

Use software polling to test the I²C Start/Restart Status bit, S (I2CxSTAT<3).

Affected Silicon Revisions

A1							
X							

41. Module: Crypto

The output digest of a partial message cannot be used as the initial vector for continuing the cryptographic operation on the remainder of the message. The full message must be processed in one operation.

Work around

None.

Affected Silicon Revisions

A1							
X							

42. Module: Crypto

The Crypto Engine does not support a Hash operation on an empty string (i.e., string with zero length). The Crypto Engine times out and does not return a valid hash.

Work around

Use the fixed known hash of the empty string.

Affected Silicon Revisions

A1							
X							

43. Module: CTMU

If the ADC module is enabled in Idle mode, it should override the setting of the CTMUSIDL bit (CTMUCON<13>) = 1, (i.e., discontinue CTMU module operation when the device enters Idle mode), and if the ADC module attempts to make a CTMU temperature sensor measurement. However, it cannot because CTMU current sources aren't enabled in Idle mode.

Work around

Set the CTMUSIDL bit to '0' to continue module operation when the device enters Idle mode.

Affected Silicon Revisions

A1							
X							

44. Module: Timer1

In Asynchronous external counter mode, (i.e., TCS bit (T1CON<1> = 1), TSYNC bit (T1CON<2> = 0), and TECS<1:0> (T1CON<9:8> = '0b01)), Timer1 does not reflect the first count from an external T1CLK input.

Work around

None.

Affected Silicon Revisions

A1							
X							

45. Module: Timer1

The Timer1 register (TMR1) in Asynchronous external counter mode, (i.e., TCS bit (T1CON<1> = 1), TSYNC bit (T1CON<2> = 0), and TECS<1:0> (T1CON<9:8> = '0b01)), remains at the initial set value for five external clock pulses after wake-up from Sleep mode.

Work around

None.

Affected Silicon Revisions

A1							
X							

46. Module: Timer1

Timer1 counts beyond the period value in Asynchronous mode when the period is 0x01.

Work around

Set the Timer1 period, PR1, to a value greater than 1.

Affected Silicon Revisions

A1							
X							

47. Module: Timer1

Timer1 does not work properly in Gated mode (i.e., TGATE bit (T1CON<7> = 1), TCS bit (T1CON<1> = 0) with the prescaler enabled (TCKPS<1:0> bits (T1CON<5:4>) = '0b00)).

Work around

None.

Affected Silicon Revisions

A1							
X							

48. Module: Timer1

Back-to-back CPU writes to the TMR1 register are not allowed for at least four PBCLK cycles.

Work around

None.

Affected Silicon Revisions

A1							
X							

49. Module: Timer1

The Asynchronous Timer Write Disable bits (TWDIS (TxCON<12>)) and the Asynchronous Timer Write In Progress bits (TWIP (TxCON<11>)) are not functional.

Work around

None.

Affected Silicon Revisions

A1							
X							

50. Module: UART

The UART TX Stop bit duration is shorter than the expected in High-Speed mode (BRGH bit (UxMODE<3>) = 1) for baud rates less than 7.5 Mbps.

Work around

For baud rates less than 7.5 Mbps, operate the UART in Standard-Speed mode, that is, BRGH bit (UxMODE<3> =0). For baud rates greater than 7.5 Mbps operate the UART in High-Speed mode, that is, BRGH bit (UxMODE<3> =1).

Affected Silicon Revisions

A1							
X							

51. Module: Sleep

If the ON bit (PB5DIV<15> = 0), and PBCLK5 is disabled, there is a 3 mA increase in Sleep IPD current.

Work around

Do not disable PBCLK5 before entering Sleep mode.

Affected Silicon Revisions

A1							
X							

52. Module: CFG

Unique ID, DEVSNx<31:0> is not programmed in the devices released earlier than trace code dated 1821xxx.

Work around

None.

Affected Silicon Revisions

A1							
X							

53. Module: EBI

The EBIRDYEN1 bit (CFGEBIC<25>), EBIRDYEN2 bit (CFGEBIC<26>), and EBIRDYEN3 bit (CFGEBIC<27>) are not functional and always set to '1'.

Work around

None.

Affected Silicon Revisions

A1							
X							

54. Module: I^2C

The 7-bit address that matches the 10-bit upper address value (111_10xx) is not accepted regardless of the STRICT bit setting.

Work around

None.

Affected Silicon Revisions

A1							
X							

55. Module: I^2C

I^2C module does not meet low period of the SCL clock (tLOW) parameter from I^2C specification for clock frequency >= 400 kHz.

Work around

None.

Affected Silicon Revisions

A1							
X							

56. Module: Input Capture

Debug breakpoints are not supported when using Input Capture with DMA.

Work around

None.

Affected Silicon Revisions

A1							
X							

57. Module: SDHC

Data from the MMC card can not be read correctly when the block size is set smaller than 512 bytes (i.e., the BSIZE<9:0> bits (SDHCBLKCON<9:0>) are smaller than 0x200).

Work around

None.

Affected Silicon Revisions

A1							
X							

58. Module: Sleep

Multiple sleep attempts (i.e., WAIT instruction with the SLPEN bit (OSCCON<4>) = 1) which occur within 20 µs of awake event, before the CPU has fully awakened, can cause the CPU to stall until a Power-on Reset (POR) event.

Work around

Ensure that at least 20 µs elapse before attempting to put the CPU to sleep (WAIT instruction with the SLPEN bit (OSCCON<4>) =1) after it awakens from a previous sleep.

Affected Silicon Revisions

A1							
X							

59. Module: SPI

Just before the last block of a transmission is shifted out to the SPI pins, the SRMT bit may incorrectly indicate that the transmission is done. However, this does not affect the Transmit Buffer Empty Interrupt (STXISEL<1:0> bits (SPIxCON<3:2>) = 0).

Work around

Use the interrupt notification rather than polling the SRMT bit to determine when a transmission has completed.

Affected Silicon Revisions

A1							
X							

60. Module: SQI

The CPU stalls if the SQI Special Function Registers are read before the REFCLKO2 clock is enabled.

Work around

None.

Affected Silicon Revisions

A1							
X							

61. Module: Timer2-9

If timer match coincides with entry into Sleep mode, timer event triggers and interrupt may not occur.

Work around

None.

Affected Silicon Revisions

A1							
X							

62. Module: Timer2-9

When timer operation is discontinued in Idle mode (i.e., the SIDL bit (TxCON <13>) is set), and timer match coincides with entry into Idle mode, timer event triggers and interrupt may not occur.

Work around

None.

Affected Silicon Revisions

A1							
X							

63. Module: Timer2-9

On a debug breakpoint, TMRx register, x=2-9, may not be representative of the correct value.

Work around

None.

Affected Silicon Revisions

A1							
X							

64. Module: USB

The USB Link Power Management (LPM) feature is not functional.

Work around

None.

Affected Silicon Revisions

A1							
X							

65. Module: USB

The USB Host module does not send the correct resume signal on the USB bus on subsequent suspend or resume sequences.

Work around

None.

Affected Silicon Revisions

A1							
X							

66. Module: USB

The USB Host module does not wake up CPU from sleep when a USB device is disconnected.

Work around

None.

Affected Silicon Revisions

A1							
X							

67. Module: USB

The USB Suspend/Resume Event through IRQ 103 is not functional.

Work around

Handle the USB Suspend/Resume event through the IRQ132 (USB General Event) and check the SUSPIF bit (USBCSR2<16>) and the RESUMEIF bit (USBCSR2 <17>) to identify the correct event.

Affected Silicon Revisions

A1							
X							

68. Module: System

CPU can lockup when SYSCLK and PBCLK7 clock frequencies are different. SYSCLK and PBCLK7 must use same clock frequency (i.e., PBDIV (PB7DIV<6:0>) must be '0') to prevent system lockups.

Work around

None.

Affected Silicon Revisions

A1							
X							

69. Module: ADC

Excessive current flows through the VREF- pin when the external voltage reference is used, and voltage on the VREF- pin is greater than AVSS.

Work around

Connect the VREF- pin to AVSS. Input dynamic range can be changed after varying voltage on the VREF+ pin.

Affected Silicon Revisions

A1							
X							

70. Module: USB

Writing '1' to the FLUSH bit (USBIENCSRx <19>, where x = 1-7) does not flush the TX FIFO and reset the TX FIFO pointer. As a result, the TXPKTRDY bit (USBIENCSRx <16>, where x = 1-7) is not cleared and the USB interrupt is not generated.

Work around

To clear the TX FIFO, repeat the following action twice in a row:

Simultaneously set the FLUSH bit (USBIENCSRx <19>, where x = 1-7) and clear the TXPKTRDY bit (USBIENCSRx <16>, where x = 1-7).

Affected Silicon Revisions

A1							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest revision of the device data sheet (DS60001361**H**).

Note: The corrected information is shown in **bold** type**.** Where possible, the original bold text formatting has been removed for clarity.

1. Module: Bitfields added to the SDHCCAP Register

The SLOTTYPE bit field and the ASYNCINT bit have been added in the SDHCCAP register.

2. Module: MPLL Maximum Output Frequency

Table 44-26 MPLL CLOCK TIMING REQUIREMENTS has been updated, and the corrected information is shown in **bold** type:

AC CHARACTERISTICS			**Standard Operating Conditions: VDDIO = 2.2V to 3.6V, VDDCORE = 1.7V to 1.9V (unless otherwise stated)** Operating temperature: -40°C ≤ TA ≤ +85°C for Industrial				
Parameter No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
MP10	MFIN	MPLL Input Frequency	8	—	64	MHz	—
MP11	MFVCO	MPLL Vco Frequency Range	400	—	1600	MHz	—
MP12	MFMPLL	MPLL Output Frequency	8	—	**200**	MHz	—
MP13	MLOCK	MPLL Start-up Time (Lock Time)	—	—	1500 x 1/MFIN	µs	—
MP14	MPJ	MPLL Period Jitter	—	—	0.015	%	—
MP15	MCJ	MPLL Cycle Jitter	—	—	0.02	%	—
MP16	MLTJ	MPLL Long-term Jitter	—	—	0.5	%	—

Note 1: These parameters are characterized, but not tested in manufacturing.

3. Module: EBI Timing Requirements

Table 44-54 EBI TIMING REQUIREMENTS has been updated, and the corrected information is shown in **bold** type:

TABLE 3-1: EBI TIMING REQUIREMENTS (1)

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature: -40°C ≤ TA ≤ +85°C for Industrial				
Parameter No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
EB10	TEBICLK	Internal EBI Clock Period (SYSCLK)	5	—	—	ns	—
EB11	TEBIRC	EBI Read Cycle Time (TRC<5:0>)	**30**	—	—	ns	—
EB12	TEBIPRC	EBI Page Read Cycle Time (TPRC<3:0>)	**30**	—	—	ns	—
EB13	TEBIAS	EBI Write Address Setup (TAS<1:0>)	**15**	—	—	ns	—
EB14	TEBIWP	EBI Write Pulse Width (TWP<5:0>)	**25**	—	—	ns	—
EB15	TEBIWR	EBI Write Recovery Time (TWR<1:0>)	**15**	—	—	ns	—
EB16	TEBICO	EBI Output Control Signal Delay	**4**	—	**13**	ns	See **Note 2**
EB17	TEBIDO	EBI Output Data Signal Delay	**4**	—	**13**	ns	See **Note 2**
EB18	TEBIDS	EBI Input Data Setup	**10**	—	—	ns	See **Note 2**
EB19	TEBIDH	EBI Input Data Hold	**3**	—	—	ns	See **Note 2, 3**

Note 1: EBI Timings Requirements data are from simulation.

2: Maximum pin capacitance = 10 pF.

3: Hold time from EBI Address change is 0 ns.

4. Module: INTERNAL DDR2 SDRAM TIMING SPECIFICATIONS

A new Note 5 has been added to Table 44-56, INTERNAL DDR2 SDRAM TIMING SPECIFICATIONS, and the note content is shown below in **bold**:

Note: When DRAM is operated at 85°C < Tj ≤ 125°C, the extended Self Refresh rate must be enabled by setting the bit A7 to '1' in the Extended Mode Register (2) EMR(2) before the Self Refresh mode can be entered. Note: For a detailed information about the EMR(2) check the DDR2 SDRAM Specification JESD79-2F.

APPENDIX A: REVISION HISTORY

Rev A Document (3/2017)

Initial release of this document, which includes the following silicon issues: 1. (Primary Oscillator), 2. (Secondary Oscillator), 3. (Reset), 4. (Reset), 5. (Power-Saving), 6. (DMA), 7. (VBAT), 8. (Deep Sleep), 9. (I^2C), 10. (ADC), 11. (ADC), 12. (ADC), 13. (ADC), 14. (SDHC), 15. (SDHC), 16. (SDHC), 17. (SDHC), 18. (SDHC), 19. (HLVD), 20. (DDR2C), 21. (DDR2C), 22. (SQI), 23. (USB), 24. (USB), 25. (System Bus), 26. (Crypto), 27. (UART), 28. (EBI), 29. (CTMU), 30. (CTMU), 31. (Temperature Sensor), 32. (ICSP), 33. (PORTS).

Rev B Document (12/2017)

Silicon issue 25. (System Bus) was updated.

Added silicon issues 34. (Primary Oscillator), 35. (Primary Oscillator), 36. (Primary Oscillator), 37. (GPU), 38. (SDHC), 39. (PMP), 40. (I^2C), 41. (Crypto), 42. (Crypto), 43. (CTMU), 44. (Timer1), 45. (Timer1), 46. (Timer1), 47. (Timer1), 48. (Timer1), and 49. (Timer1).

Added data sheet clarifications, 1. (Comparator), 3. (Device Configuration Word 0 Registers (DEVCFG0/ ADEVCFG0)), and 4. (Device Configuration Word 1 Registers (DEVCFG1/ADEVCFG1)).

Rev C Document (9/2018)

Added Silicon Issues 50. (UART), 51. (Sleep), and 52. (CFG).

Removed Previous Data Sheet Clarifications 1, 2, 3, and 4.

Added Data Sheet Clarification 1. (Comparator).

Rev D Document 6/2019

Added Silicon Issues 53. (EBI), 54. (I^2C), 55. (I^2C), 56. (Input Capture), 57. (SDHC), 58. (Sleep), 59. (SPI), 60. (SQI), 61. (Timer2-9), 62. (Timer2-9), 63. (Timer2-9), 64. (USB), 65. (USB), and 66. (USB).

Removed previous Data Sheet Clarifications for Module 1 Comparator.

Revision E Document 09/2019

The following silicon issue was updated with new verbiage: 23. Module: “USB”.

Added Silicon Issue 67. Module: “USB”.

Added Data Sheet Clarification: 1. Module: “Bitfields added to the SDHCCAP Register”

Revision F Document 10/2020

The following Silicon Issues were added:

- 68. Module: “System”
- 69. Module: “ADC”
- 70. Module: “USB”

Revision G Document 05/2021

The I^2C, SPI, and I^2S standards use the terminology "Master" and "Slave". The equivalent Microchip terminology used in this document is "Host" and "Client" respectively.

The following Silicon Issues were updated:

- 70. Module: “USB”

The following Data Sheet Clarifications were added:

- 1. Module: “Bitfields added to the SDHCCAP Register”
- 2. Module: “MPLL Maximum Output Frequency”
- 3. Module: “EBI Timing Requirements”
- 4. Module: “INTERNAL DDR2 SDRAM TIMING SPECIFICATIONS”

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