PIC32MX330/350/370/430/450/470

PIC32MX330/350/370/430/450/470 Family Silicon Errata and Data Sheet Clarification

The PIC32MX330/350/370/430/450/470 family of devices that you have received conform functionally to the current Device Data Sheet (DS60001185**G**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1 through Table 4. The silicon issues are summarized in Table 5.

The errata described in this document will be addressed in future revisions of the PIC32MX330/350/370/430/450/470 family silicon.

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 5 apply to the current silicon revision (**A1**).

Data Sheet clarifications and corrections (if applicable) start on page 14, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® X IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

For example, to identify the silicon revision level using MPLAB X IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB X IDE project.
3. Configure the MPLAB X IDE project for the appropriate device and hardware debugger.
4. Select *Window > Dashboard*, and then click the **Refresh Debug Tool Status** icon (🔄).
5. The part number and the Device and Revision ID values appear in the **Output** window.

> **Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various PIC32MX330/350/370/430/450/470 silicon revisions are shown in Table 1 and Table 4.

TABLE 1: SILICON DEVREV VALUES FOR DEVICES WITH 64 KB FLASH MEMORY

Part Number	Flash Memory Size (KB)	Device ID$^{(1)}$	Revision ID for Silicon Revision$^{(1)}$		
			A0	A1	B0
PIC32MX330F064H	64	0x05600053	0x0	0x1	0xB
PIC32MX330F064L	64	0x05601053			
PIC32MX430F064H	64	0x05602053			
PIC32MX430F064L	64	0x05603053			

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001185**G**) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON DEVREV VALUES FOR DEVICES WITH 128 KB FLASH MEMORY

Part Number	Flash Memory Size (KB)	Device ID(1)	Revision ID for Silicon Revision(1)		
			A0	A1	B0
PIC32MX350F128H	128	0x0570C053	0x0	0x1	0x8
PIC32MX350F128L	128	0x0570D053			
PIC32MX450F128H	128	0x0570E053			
PIC32MX450F128L	128	0x0570F053			

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001185**G**) for detailed information on Device and Revision IDs for your specific device.

TABLE 3: SILICON DEVREV VALUES FOR DEVICES WITH 256 KB FLASH MEMORY

Part Number	Flash Memory Size (KB)	Device ID(1)	Revision ID for Silicon Revision(1)		
			A0	A1	B1
PIC32MX350F256H	256	0x05704053	0x0	0x1	0xA
PIC32MX350F256L	256	0x05705053			
PIC32MX450F256H	256	0x05706053			
PIC32MX450F256L	256	0x05707053			

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001185**G**) for detailed information on Device and Revision IDs for your specific device.

TABLE 4: SILICON DEVREV VALUES FOR DEVICES WITH 512 KB FLASH MEMORY

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)	
		A0	B0
PIC32MX370F512H	0x05808053	0x0	0xC
PIC32MX370F512L	0x05809053		
PIC32MX470F512H	0x0580A053		
PIC32MX470F512L	0x0580B053		

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001185**G**) for detailed information on Device and Revision IDs for your specific device.

TABLE 5: SILICON ISSUE SUMMARY

Module	Feature	Item #	Issue Summary	Affected Revisions				
				Flash Memory (KB)	A0	A1	B0	B1
ADC	Differential Nonlinearity	1.	The ADC module is not within the published data sheet specification when operating at a conversion rate above 500 ksps.	64	X	X	X	—
				128	X	X	X	—
				256	X	X	—	X
				512	X	—	X	—
Clock	Clock Out	2.	A clock signal is present on the CLKO pin, regardless of the clock source and setting of the CLKO Enable Configuration bit, during a Power-on Reset (POR) condition.	64	X	X	X	—
				128	X	X	X	—
				256	X	X	—	X
				512	X	—	X	—
Reserved	—	3.	—	—	—	—	—	—
I/O	I/O	4.	Port pin RF6 is not 5V tolerant. Use RF6 as a non-5V tolerant pin only.	64	X	X	X	—
				128	X	X	X	—
				256	X	X	—	X
				512	X	—	X	—
5V Tolerant I/O Pins	Pull-ups	5.	Internal pull-up resistors may not guarantee a logical '`1`' on digital inputs on 5V tolerant pins.	64	X	X	X	—
				128	X	X	X	—
				256	X	X	—	X
				512	X	—	X	—
Non-5V Tolerant I/O Pins	Pull-ups	6.	Internal pull-up resistors may not guarantee a logical '`1`' on digital inputs on non-5V tolerant pins.	64	X			—
				128	X			—
				256	X		—	
				512		—		—
I^{2}C	Slave Mode	7.	When the I^{2}C slave receives any of the reserve address with STRICT = `1`, an ACK will be generated, but an interrupt will not be generated.	64	X	X	X	—
				128	X	X	X	—
				256	X	X	—	X
				512	X	—	X	—
JTAG	Boundary Scan	8.	Boundary Scan is not supported.	64	X	X	X	—
				128	X	X	X	—
				256	X	X	—	X
				512	X	—	X	—

Legend: An 'X' indicates the issue is present in this revision of the silicon.
Shaded cells with an Em dash ('—') indicate that this silicon revision does not exist for this issue.
Blank cells indicate an issue has been corrected or does not exist in this revision of the silicon.

TABLE 5: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item #	Issue Summary	Affected Revisions				
				Flash Memory (KB)	A0	A1	B0	B1
Watchdog Timer	Windowed Watchdog	9.	Clearing the Watchdog Timer inside the window when in Window mode may cause a reset.	64	X	X	X	—
				128	X	X	X	—
				256	X	X	—	X
				512	X	—	X	—
Debug	Debug Pins	10.	On-chip debug pins require special consideration.	64				—
				128	X	X	X	—
				256	X	X	—	X
				512		—		—
USB	Idle Interrupt	11.	USB Idle interrupts cease if the IDLEIF flag is cleared and the bus is left idle for more than 3 ms.	64	X	X	X	—
				128	X	X	X	—
				256	X	X	—	X
				512	X	—	X	—
I/O Port	Open Drain	12.	The Open Drain selection (ODCx) on I/O port pins is not available when the pin is configured for anything other than a standard port output.	64	X	X	X	—
				128	X	X	X	—
				256	X	X	—	X
				512	X	—	X	—
Flash Memory	Flash Memory	13.	The Program Write Protection (PWP) bits are not able to protect all 512 KB of Flash memory on PIC32MX370/470 devices.	64				—
				128				—
				256			—	
				512	X	—	X	—
Timer1	Interrupts	14.	Under specific conditions, Timer1 will not generate interrupts.	64	X	X	X	—
				128	X	X	X	—
				256	X	X	—	X
				512	X	—	X	—
UART	Auto-baud	15.	The Automatic Baud Rate feature does not function to set the baud rate.	64	X	X	X	—
				128	X	X	X	—
				256	X	X	—	X
				512	X	—	X	—

Legend: An 'X' indicates the issue is present in this revision of the silicon.
Shaded cells with an Em dash ('—') indicate that this silicon revision does not exist for this issue.
Blank cells indicate an issue has been corrected or does not exist in this revision of the silicon.

TABLE 5: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item #	Issue Summary	Affected Revisions				
				Flash Memory (KB)	A0	A1	B0	B1
UART	Synchronization	16.	On a RX FIFO overflow, shift registers stop receiving data, which causes the UART to lose synchronization.	64	X	X	X	—
				128	X	X	X	—
				256	X	X	—	X
				512	X	—	X	—
CTMU	Module Operation	17.	The CTMU module is not functional	64	X	X	X	—
				128	X	X	X	—
				256	X	X	—	X
				512	X	—	X	—
ADC	IVREF Sensing	18.	Testing the IVREF setting with the ADC module does not function as intended.	64	X	X	X	—
				128	X	X	X	—
				256	X	X	—	X
				512	X	—	X	—
HVD	HVDR	19.	On power-up, the High-Voltage Detect Reset event flag, RCON<HVDR> is being set.	64	X	X	X	—
				128	X	X	X	—
				256	X	X	—	X
				512	X	—	X	—
Power-Saving Modes	Idle	20.	On exit from Sleep mode, the SLEEP and IDLE status bits in the RCON register are being set.	64	X	X	X	—
				128	X	X	X	—
				256	X	X	—	X
				512	X	—	X	—
Flash Memory	Write Protection	21.	When enabled, the Boot Write Protect (BWP) bit also protects and overlaps the first page of user program space below 0x1000 in addition to the boot segment	64	X	X	X	—
				128	X	X	X	—
				256	X	X	—	X
				512	X	—	X	—
Flash Memory	Write Protection	22.	The Program Write Protection (PWP) bit field is off by one page relative to the definition in the data sheet.	64	X	X	X	—
				128	X	X	X	—
				256	X	X	—	X
				512	X	—	X	—

Legend: An ‘X’ indicates the issue is present in this revision of the silicon.
Shaded cells with an Em dash (‘—’) indicate that this silicon revision does not exist for this issue.
Blank cells indicate an issue has been corrected or does not exist in this revision of the silicon.

TABLE 5: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item #	Issue Summary	Affected Revisions				
				Flash Memory (KB)	A0	A1	B0	B1
Flash Memory	Write Protection	23.	The Program Write Protection (PWP) bits are not enabled unless the Boot Write Protect (BWP) bit is also enabled.	64	X	X	X	—
				128	X	X	X	—
				256	X	X	—	X
				512	X	—	X	—
I/O Pins	Peripheral Pin Select (PPS)	24.	The RPF3 pin is not available for PPS functions on USB devices.	64	X	X	X	—
				128	X	X	X	—
				256	X	X	—	X
				512	X	—	X	—
USB Low-Speed Mode	Low-Speed Mode	25.	The USB Low-Speed mode is not supported.	64	X	X	X	—
				128	X	X	X	—
				256	X	X	—	X
				512	X	—	X	—

Legend: An ‘X’ indicates the issue is present in this revision of the silicon.
Shaded cells with an Em dash (‘—’) indicate that this silicon revision does not exist for this issue.
Blank cells indicate an issue has been corrected or does not exist in this revision of the silicon.

Silicon Errata Issues

Note 1: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. The table provided in each issue indicates which issues exist for a particular revision of silicon based on Flash memory size.

2: The following applies to the Affected Silicon Revision tables in each silicon issue:

- An ‘X’ indicates the issue is present in this revision of silicon
- Shaded cells with an Em dash (‘—’) indicate that this silicon revision does not exist for this issue
- Blank cells indicate an issue has been corrected or does not exist in this revision of silicon.

1. Module: ADC

When the ADC is configured for 10-bit operation, the specifications in the data sheet are not met for operation above 500 ksps.

Work around

For 600 ksps operation, RIN = 500 ohms, TSAMP = 2 TAD. The module specifications are shown in Table 6. For 1000 ksps operation, RIN = 200 ohms, TSAMP = 2 TAD. The module specifications are shown in Table 7.

TABLE 6: 600 KSPS OPERATION

Parameter No.	Symbol	Minimum	Typical	Maximum	Units
AD17	RIN	—	—	200	Ohm
ADC Accuracy – Measurements taken with External VREF+/VREF-					
AD21c	INL	-1.5	—	1.5	LSB
AD22c	DNL	-1.4	—	2.1	LSB
AD23c	GERR	-1.2	—	1.2	LSB
ADC Accuracy – Measurements taken with Internal VREF+/VREF-					
AD21d	INL	-1.5	—	1.5	LSB
AD22d	DNL	-1.4	—	2.1	LSB

TABLE 7: 1000 KSPS OPERATION

Parameter No.	Symbol	Minimum	Typical	Maximum	Units
AD17	RIN	—	—	200	Ohm
ADC Accuracy – Measurements taken with External VREF+/VREF-					
AD21c	INL	-5.2	—	6.5	LSB
AD22c	DNL	-3.4	—	7	LSB
AD23c	GERR	-1.5	—	1.5	LSB
ADC Accuracy – Measurements taken with Internal VREF+/VREF-					
AD21d	INL	-5.2	—	6.5	LSB
AD22d	DNL	-3.4	—	7	LSB

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1	B0	B1		
64	X	X	X	—		
128	X	X	X	—		
256	X	X	—	X		
512	X	—	X	—		

2. Module: Clock

A clock signal is present on the CLKO pin, regardless of the clock source and setting of the CLKO Enable Configuration bit, OSCIOFNC (DEVCFG1<10>), during a Power-on Reset (POR) condition.

Work around

Do not connect the CLKO pin to a device that would be adversely affected by rapid pin toggling or a frequency other than that defined by the oscillator configuration. Do not use the CLKO pin as an input if the device connected to the CLKO pin would be adversely affected by the pin driving a signal out.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1	B0	B1		
64	X	X	X	—		
128	X	X	X	—		
256	X	X	—	X		
512	X	—	X	—		

3. Module: Reserved

The issue, previously reported in a prior revision of this errata, is no longer relevant and was removed.

4. Module: I/O

The port pin, RF6, is not 5V tolerant. Use RF6 as a non-5V tolerant pin only.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1	B0	B1		
64	X	X	X	—		
128	X	X	X	—		
256	X	X	—	X		
512	X	—	X	—		

5. Module: 5V Tolerant I/O Pins

When internal pull-ups are enabled on 5V tolerant pins, the level as measured on the pin and available to external device inputs may not exceed the minimum value of V_{IH}, and therefore qualify as a logic “high”. However, with respect to the PIC32 device, as long as $V_{DD} \geq 3V$ and the load doesn't exceed -50 µA, the internal pull-ups are guaranteed to be recognized as a logic “high” internally to the device.

Work around

It is recommend to use only external pull ups:

- To guarantee a logic “high” for external logic input circuits outside of the PIC32 device
- For PIC32 device inputs, if the external load exceeds -50 µA or $V_{DD} < 3V$

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1	B0	B1		
64	X	X	X	—		
128	X	X	X	—		
256	X	X	—	X		
512	X	—	X	—		

6. Module: Non-5V Tolerant I/O Pins

When internal pull-ups are enabled on non-5V tolerant pins, the level as measured on the pin and available to external device inputs may not exceed the minimum value of V_{IH}, and therefore qualify as a logic “high”. However, with respect to the PIC32 device, as long as $V_{DD} \geq 3V$ and the load doesn't exceed -50 µA, the internal pull ups are guaranteed to be recognized as a logic “high” internally to the device.

Work around

It is recommend to only use external pull ups:

- To guarantee a logic “high” for external logic input circuits outside of the PIC32 device
- For PIC32 device inputs, if the external load exceeds -50 µA or $V_{DD} < 3V$

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1	B0	B1		
64	X			—		
128	X			—		
256	X		—			
512		—		—		

7. Module: I^2C

The slave address, 0x78, is one of a group of reserved addresses. It is used as the upper byte of a 10-bit address when 10-bit addressing is enabled. The I^2C module control register allows the programmer to enable both 10-bit addressing and strict enforcement of reserved addressing, with the A10M and STRICT bits, respectively. When both bits are cleared, the device should respond to the reserved address 0x78, but it does not.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1	B0	B1		
64	X	X	X	—		
128	X	X	X	—		
256	X	X	—	X		
512	X	—	X	—		

8. Module: JTAG

Boundary Scan is not supported.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1	B0	B1		
64	X	X	X	—		
128	X	X	X	—		
256	X	X	—	X		
512	X	—	X	—		

9. Module: Watchdog Timer

When the Watchdog Timer module is used in Windowed mode, the module may issue a reset even if the user tries to clear the module within the allowed window.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1	B0	B1		
64	X	X	X	—		
128	X	X	X	—		
256	X	X	—	X		
512	X	—	X	—		

10. Module: Debug

For PIC32MX350/450 devices, the programming pin pairs at PGEC2/PGED2 and PGEC3/PGED3 may not function for on-chip debugging if PGEC1 is open or is a logical “high”.

Work arounds

- Use the PGEC1/PGED1 pins for debugging
  OR
- Hold PGEC1 to V_{SS} with an external resistor with a value of 150k or less while debugging on another pair.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1	B0	B1		
64				—		
128	X	X	X	—		
256	X	X	—	X		
512		—		—		

11. Module: USB

If the bus has been idle for more than 3 ms, the IDLEIF interrupt flag is set. If software clears the interrupt flag and the bus remains idle, the IDLEIF interrupt flag will not be set again.

Work around

Software can leave the IDLEIF bit set until it has received some indication of bus resumption (i.e., Resume, Reset, SOF, or Error).

> **Note:** Resume and Reset are the only interrupts that should be following IDLEIF assertion. If the IDLEIF bit is set, it should be okay to suspend the USB module (as long as this code is protected by the GUARD and/or ACTPEND logic). This will require software to clear the IDLEIF interrupt enable bit to exit the USB ISR (if using interrupt driven code).

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1	B0	B1		
64	X	X	X	—		
128	X	X	X	—		
256	X	X	—	X		
512	X	—	X	—		

12. Module: I/O Port

The Open Drain selection (ODCx) on I/O port pins is not available when the pin is configured for anything other than a standard port output. In addition, the Open Drain feature is not available for dedicated or remappable Peripheral Pin Select (PPS) output features.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1	B0	B1		
64	X	X	X	—		
128	X	X	X	—		
256	X	X	—	X		
512	X	—	X	—		

13. Module: Flash Memory

The Program Write Protection (PWP) bits are not able to protect all 512 KB of Flash memory on PIC32MX370/470 devices.

Work around

The PWP<7:0> bits in the DEVCFG0 Configuration register can protect a maximum of 508 KB of Flash memory.

Use a PWP<7:0> value of 0x10000000 for a maximum of 508 KB (memory location 0xBD07EFFF).

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1	B0	B1		
64				—		
128				—		
256			—			
512	X	—	X	—		

14. Module: Timer1

Timer1 fails to generate interrupts when configured as follows:

- External Clock Input and
- Asynchronous Clock and
- Prescaler other than 1:1

Work around

Any other combination of the timer will generate interrupts as expected. For example, Synchronous mode or leaving the prescaler at 1:1.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1	B0	B1		
64	X	X	X	—		
128	X	X	X	—		
256	X	X	—	X		
512	X	—	X	—		

15. Module: UART

The UART Automatic baud rate feature is intended to set the baud rate during run-time based on external data input. However, this feature does not function.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1	B0	B1		
64	X	X	X	—		
128	X	X	X	—		
256	X	X	—	X		
512	X	—	X	—		

16. Module: UART

During a RX FIFO overflow condition, the shift register stops receiving data. This causes the UART to lose synchronization with the serial data stream. The only way to recover from this is to turn the UART OFF and ON until it synchronizes. This could require several OFF/ON sequences.

Work arounds

Work around 1:

Avoid the RX overrun condition by ensuring that the UARTx module has a high enough interrupt priority such that other peripheral interrupt processing latencies do not exceed the time to overrun the UART RX buffer based on the application baud rate. Alternately or in addition to, set the URXISEL bits in the UxSTA register to generate an earlier RX interrupt based on RX FIFO fill status to buy more time for interrupt latency processing requirements.

Work around 2:

If avoiding RX FIFO overruns is not possible, implement a ACK/NAK software handshake protocol to repeat lost packet transfers after restoring UART synchronization.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1	B0	B1		
64	X	X	X	—		
128	X	X	X	—		
256	X	X	—	X		
512	X	—	X	—		

17. Module: CTMU

The CTMU module is not functional.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1	B0	B1		
64	X	X	X	—		
128	X	X	X	—		
256	X	X	—	X		
512	X	—	X	—		

18. Module: ADC

Converting the Internal Band Gap (IVREF) voltage source generates a High-Voltage Detect (HVD) event and aborts the conversion; therefore, this feature is not functional.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1	B0	B1		
64	X	X	X	—		
128	X	X	X	—		
256	X	X	—	X		
512	X	—	X	—		

19. Module: HVD

On power-up, the High-Voltage Detect Reset, event flag, RCON<HVDR>, is set incorrectly.

On a power-up, only the POR, BOR, and EXTR bits should be set with the proper VCAP bypass capacitor value, as stated in the current data sheet.

Work around

Check the status of the POR bit in the RCON register when checking the HVDR bit. If the POR bit is set, both bits can be cleared as the HVDR bit is a false detection. If the POR bit is clear, the HVDR bit has been correctly detected and can be handled according to the requirements of the application.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1	B0	B1		
64	X	X	X	—		
128	X	X	X	—		
256	X	X	—	X		
512	X	—	X	—		

20. Module: Power-Saving Modes

On exit from Sleep mode, both the SLEEP and IDLE status bits in the RCON register are set.

Work around

Add the following code to the user application at the point it wakes from Sleep mode:

```
rcon_var1 = RCON;
// ... enter Sleep mode
if (rcon_var1 & 0x4) Nop();
// If IDLE bit already set previously
// before sleep do nothing
else RCONbits.IDLE = 0x0;
// If IDLE bit is not set previously
// and is after Sleep mode then clear
```

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1	B0	B1		
64	X	X	X	—		
128	X	X	X	—		
256	X	X	—	X		
512	X	—	X	—		

21. Module: Flash Memory

When enabled, the Boot Write Protect (BWP) bit inadvertently also protects and overlaps the first page of PWP user program space below 0x1000, (i.e., PWP<7:0> = 0xFE), in addition to the boot segment, regardless of the state of the Program Write Protection (PWP) bits (DEVCFG0<19:12>). If BWP is enabled by setting the BWP bit (DEVCFG0<24>) = 0, users cannot Page Erase or program the first page of the PWP user program space. Only user run-time Page Erase or Program operations are affected, which does not include a Bulk erase of the entire Flash.

Work around

None. Refer to silicon issues 22 and 23 for related information

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1	B0	B1		
64	X	X	X	—		
128	X	X	X	—		
256	X	X	—	X		
512	X	—	X	—		

22. Module: Flash Memory

The Program Write Protection (PWP) bit field is off by one page relative to the data sheet definition. In silicon, PWP<7:0> = (n + 1), where 'n' is the DEVCFG0<19:12> value as defined in the data sheet.

TABLE 8: PWP BITS (DEVCFG0<19:12>)

Value	Expected	Actual
`11111111`	Disabled	Disabled
`11111110`	Memory below 0x01000 is write protected	Disabled
`11111101`	Memory below 0x02000 is write protected	Memory below 0x01000 is write protected
...		
`01111111`	Memory below 0x80000 is write protected	Memory below 0x7F000 is write protected

Work around

Set the PWP<7:0> bits (DEVCFG0<19:12>) = (DEVCFG0<PWP> - 1) to correct for the first page protection offset. Please refer to silicon issues 21 and 23 for related information.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1	B0	B1		
64	X	X	X	—		
128	X	X	X	—		
256	X	X	—	X		
512	X	—	X	—		

23. Module: Flash Memory

The Program Write Protection (PWP) bits (DEVCFG0<19:12>) are not enabled unless the Boot Write Protect (BWP) bit (DEVCFG0<24> is also enabled (i.e., = 0).

Work around

None. Please refer to silicon issues 21 and 22 for related information.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1	B0	B1		
64	X	X	X	—		
128	X	X	X	—		
256	X	X	—	X		
512	X	—	X	—		

24. Module: I/O Pins

The RPF3 Peripheral Pin Select (PPS) functions are not available on PIN32MX4xx USB device variants. The PIC32MX3xx General Purpose devices are not affected.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1	B0	B1		
64	X	X	X	—		
128	X	X	X	—		
256	X	X	—	X		
512	X	—	X	—		

25. Module: USB Low-Speed Mode

The USB Low-Speed mode is not supported.

Work around

None.

Affected Silicon Revisions

Device Flash Memory (KB)	Device Silicon Revision					
	A0	A1	B0	B1		
64	X	X	X	—		
128	X	X	X	—		
256	X	X	—	X		
512	X	—	X	—		

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001185**G**):

No clarifications to report at this time.

APPENDIX A: REVISION HISTORY

Rev A Document (4/2013)

Initial release of this document; issued for revision A0 silicon.

Includes silicon issues 1 (ADC), 2 (Clock), 3 (Reserved), 4 (I/O), 5 (5V Tolerant I/O Pins), 6 (Non-5V Tolerant I/O Pins), 7 (I^2C), 8 (JTAG), and 9 (Watchdog Timer).

Rev B Document (6/2013)

Updated the silicon revision to Rev. A1 and added the PIC32MX350/430/450 devices.

Added silicon issues 10 (Debug), 11 (USB), and 12 (I/O Port). Updated silicon issue 3 (Reserved).

Rev C Document (10/2013)

Added the 512 KB Flash memory devices (PIC32MX370/470).

Updated silicon issue 1 (ADC).

Added silicon issues 13 (Flash Memory) and 14 (Timer1).

Rev D Document (6/2014)

Added Data Sheet Clarification 1 (Packaging) and 2 (Power-Down Current (IPD)).

Rev E Document (2/2015)

The document was updated for silicon revision B0 devices:

- 128 KB devices were moved from Table 1 to Table 2.
- Added separate 128 KB row to Affected Silicon Revisions tables.

Added silicon issues 15 (UART), 16 (UART), 17 (CTMU), 18 (ADC), 19 (HVD), and 20 (Power-Saving Modes), 21 (Flash Memory), 22 (Flash Memory), and 23 (Flash Memory).

Deleted silicon issue 3 (CTMU).

Rev F Document (6/2015)

Deleted Data Sheet Clarification 1 (Packaging).

Added Data Sheet Clarification 1 (Power-Down Current (IPD)).

Updated Table 31-7.

Rev G Document (6/2018)

Added issue 24 (I/O Pins).

Removed Data Sheet Clarification 1 (Power-Down Current IPD).

Added **TABLE 3: “Silicon DEVREV Values For Devices With 256 KB Flash Memory”** to reflect updates for the 256 Flash Memory.

Rev H Document (01/2020

Updated B0 data for all errata.

Added a new silicon issue **25. Module: “USB Low-Speed Mode”**.

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