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Chip Errata for the MB90880/910/920/930/950/990 Series, F^{2}MC-16LX Family, 16-Bit Microcontroller

This document describes the chip errata for the MB90880/910/920/930/950/990 Series, F^{2}MC-16LX Family, 16-Bit Microcontroller. Compare this document to the device's data sheet for a complete functional description.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number
MB90880/910/920/930/950/990 Series

Problem Description

The functional limitation of PLL stop mode was found. It is rare problem that CPU does not return to PLL clock mode normally when it returns from PLL stop mode by external interrupt. Details of the functional limitation and workaround are provided in this errata.

No limitation occurs, if one of the following conditions met:

- PLL stop mode is not used
- PLL stop mode is released by external reset or power on reset
- PLL clock multiplication rate: 1 or 2 or 3 or 4

Affected Devices

Table 1. Affected Devices

Series	Part Number
MB90880 series	MB90882/S, MB90F882A/S, MB90F883B/S, MB90F883BH/S,MB90F883C/S, MB90F884B/S, MB90F884BH/S, MB90F884C/S
MB90910 series	MB90911AS, MB90F912BS
MB90920 series	MB90922NCS, MB90F922NC/S, MB90F923NC/S, MB90F924NC/S
MB90930 series	MB90931/S, MB90F931/S
MB90950 series	MB90F952JDS/MDS
MB90990 series	MB90F997JBS/MBS

Details of the Limitation

When CPU returns from PLL stop mode by external interrupt, it usually starts to execute program in PLL clock mode after the oscillation stable waiting time progress set up in CKSCR:WS1,0 bit.
However, Table 1 Affected devices may perform operation (1) or (2) or (3) immediately after external interrupt input.

1. Reset start without reset source

2. Start in Main clock mode, then change to PLL clock mode after PLL clock oscillation stabilization wait time (2^{14}/Main clock) progress

3. Start in PLL clock mode without clock oscillation stabilization wait time

4. In (3) case, CPU may execute incorrect instruction because it operates by unstable PLL clocks.As a result, user system may malfunction.

No limitation occurs, if one of the following conditions met:

■ PLL stop mode is not used

■ PLL stop mode is released by external reset or power on reset

■ PLL clock multiplication rate: 1 or 2 or 3 or 4

Workaround

Use on the conditions of 1) or 2) or 3)

1. Use Main stop mode instead of PLL STOP mode

2. Use by the following state transiton

3. PLL clock mode => Main clock mode => Main stop mode => Main clock mode => PLL clock mode

4. PLL stop mode is released by external reset or power on reset

5. PLL clock multiplication rate: 1 or 2 or 3 or 4

Corrective Action by Spansion

We will release errata sheet of each Hardware manuals to prohibit PLL stop mode.

Document History Page

Document Title: MB90880/900 Series - Chip Errata for the MB90880/910/920/930/950/990 Series, F^{2}MC-16LX Family, 16-Bit Microcontroller **Document Number: 002-04398**			
Rev.	**ECN No.**	**Orig. of Change**	**Description of Change**
**	_	YUIS	Initial Release
*A	5233073	YUIS	Migrated to Cypress format