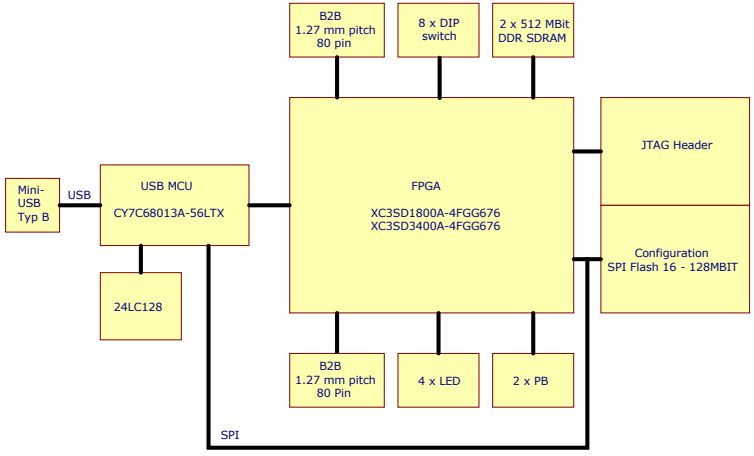

U_01
01.SchDoc

U_01
03.SchDoc

U_01
05.SchDoc

U_01
07.SchDoc

U_01
02.SchDoc

U_01
04.SchDoc

U_01
06.SchDoc

MHole2.2mm
FGND

MHole2.2mm
FGND

MHole2.2mm
FGND

MHole2.2mm
FGND

WEEE1
WEEE TOP

PM1

PM2

PM3

PM4

PM5

PM6

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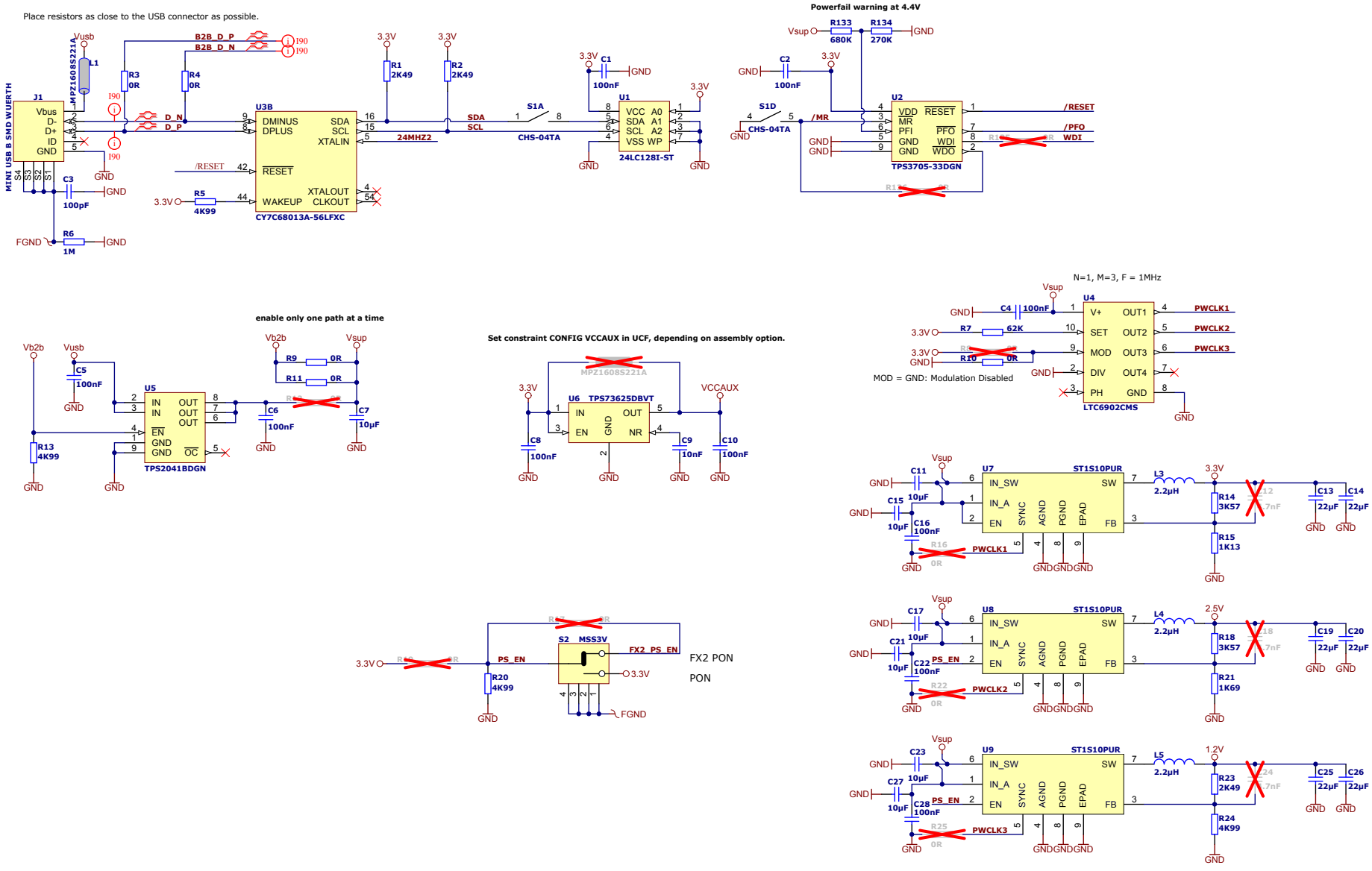
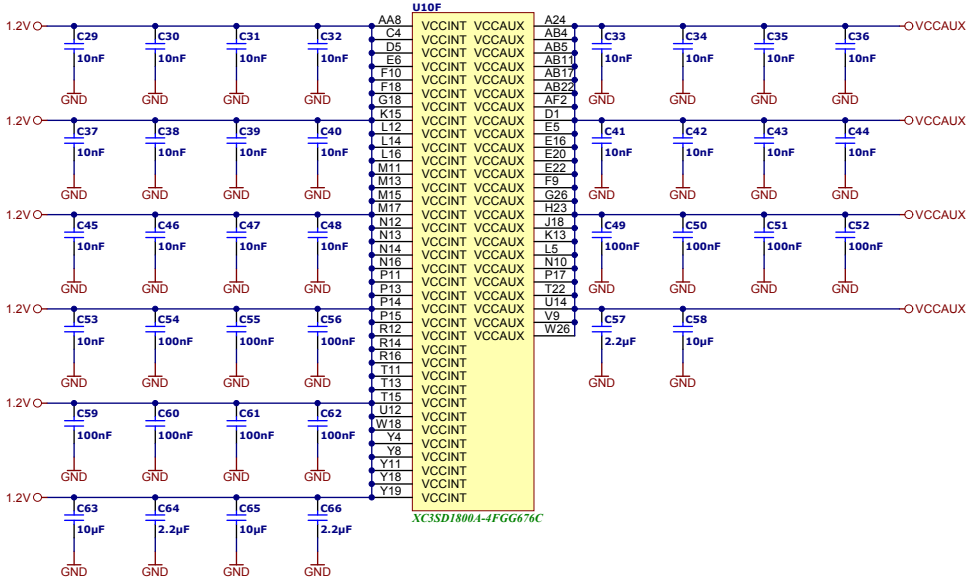
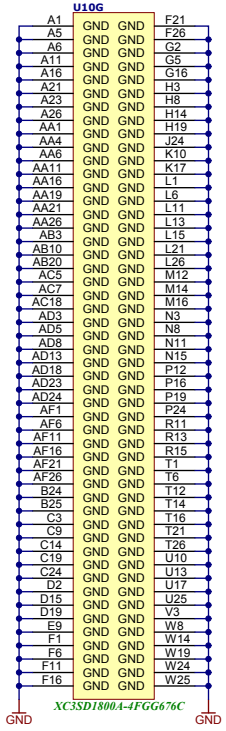
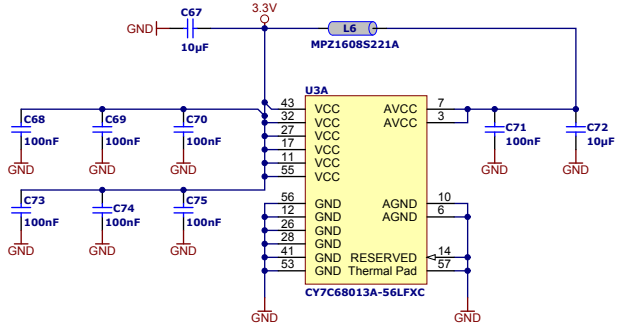
Title: Overview			
A4	Nummer: TE0320		Rev. 00
Datum: 2009-09-21	Zeichner:		Blatt 1 von 8
Filename: 00.SchDoc			

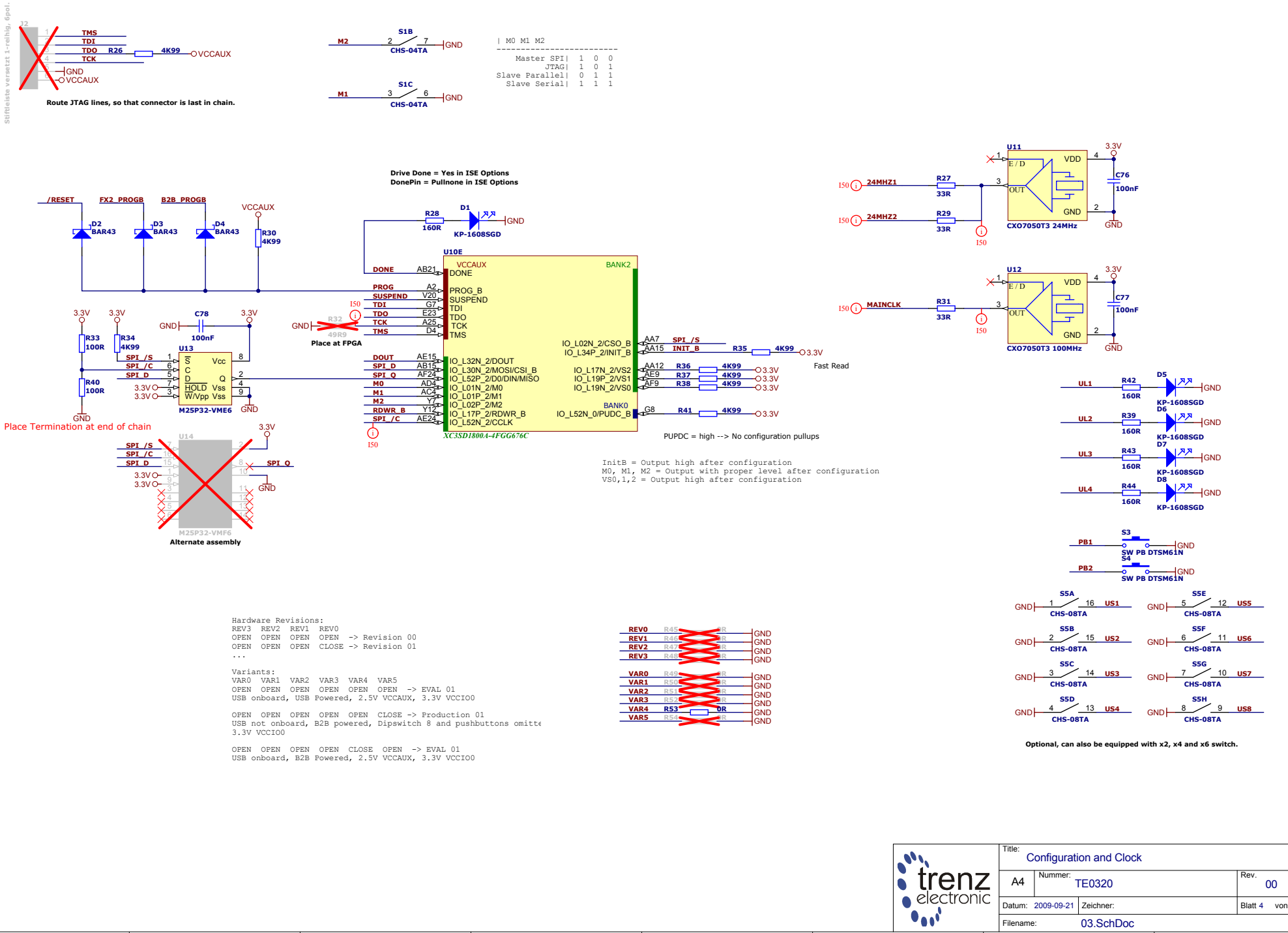

Place resistors as close to the USB connector as possible.
MINI USB B SMD WUERTH
J1
MPZ1608S221A
L1
R3 0R
R4 0R
B2B_D_P
B2B_D_N
I90
D_N
D_P
U3B
CY7C68013A-56LFXC
DMINUS
DPLUS
SDA
SCL
XTALIN
RESET
WAKEUP
CLKOUT
XTALOUT
/RESET
R5 4K99
C3 100pF
R6 1M
R1 2K49
R2 2K49
24MHZ2
S1A
CHS-04TA
U1
24LC128I-ST
C1 100nF
C2 100nF
Powerfail warning at 4.4V
R133 680K
R134 270K
S1D
/MR
U2
TPS3705-33DGN
/RESET
/PFO
WDI
enable only one path at a time
U5
TPS2041BDGN
R9 0R
R11 0R
C5 100nF
C6 100nF
C7 10µF
R13 4K99
Set constraint CONFIG VCCAUX in UCF, depending on assembly option.
MPZ1608S221A
U6 TPS73625DBVT
C8 100nF
C9 10nF
C10 100nF
VCCAUX
N=1, M=3, F = 1MHz
U4
LTC6902CMS
R7 62K
R10 0R
MOD = GND: Modulation Disabled
PWCLK1
PWCLK2
PWCLK3
U7
U8
U9
ST1S10PUR
L3 2.2µH
L4 2.2µH
L5 2.2µH
R14 3K57
R15 1K13
R18 3K57
R21 1K69
R23 2K49
R24 4K99
C11 10µF
C15 10µF
C16 100nF
C17 10µF
C21 10µF
C22 100nF
C23 10µF
C27 10µF
C28 100nF
C13 22µF
C14 22µF
C19 22µF
C20 22µF
C25 22µF
C26 22µF
3.3V
2.5V
1.2V
S2 MSS3V
FX2_PS_EN
PS_EN
R20 4K99
FX2 PON
PON
Title: Powersupply
A4
Nummer: TE0320
Rev. 00
Datum: 2009-09-21
Zeichner:
Blatt 2 von 8
Filename: 01.SchDoc
trenz electronic







Title: Chip Powersupply		
A4	Nummer: TE0320	Rev. 00
Datum: 2009-09-21	Zeichner:	Blatt 3 von 8
Filename: 02.SchDoc		


Stiftleiste versetzt 1-reihig, 6pol.
J2
TMS
TDI
TDO
TCK
GND
VCCAUX
R26
4K99
Route JTAG lines, so that connector is last in chain.
S1B
M2
CHS-04TA
S1C
M1
| M0 M1 M2
Master SPI| 1 0 0
JTAG| 1 0 1
Slave Parallel| 0 1 1
Slave Serial| 1 1 1
Drive Done = Yes in ISE Options
DonePin = PullnOne in ISE Options
/RESET
FX2_PROGB
B2B_PROGB
D2 BAR43
D3 BAR43
D4 BAR43
R30 4K99
R28 160R
D1 KP-1608SGD
U10E
VCCAUX
DONE
PROG_B
SUSPEND
TDI
TDO
TCK
TMS
BANK2
BANK0
IO_L02N_2/CSO_B
IO_L34P_2/INIT_B
IO_L32N_2/DOUT
IO_L30N_2/MOSI/CSI_B
IO_L52P_2/D0/DIN/MISO
IO_L01N_2/M0
IO_L01P_2/M1
IO_L02P_2/M2
IO_L17P_2/RDWR_B
IO_L52N_2/CCLK
IO_L17N_2/VS2
IO_L19P_2/VS1
IO_L19N_2/VS0
IO_L52N_0/PUDC_B
XC3SD1800A-4FGG676C
R32 49R9
Place at FPGA
R33 100R
R34 4K99
R40 100R
C78 100nF
U13
M25P32-VME6
Place Termination at end of chain
U14
M25P32-VMF6
Alternate assembly
R35 4K99
R36 4K99
R37 4K99
R38 4K99
R41 4K99
Fast Read
PUPDC = high --> No configuration pullups
InitB = Output high after configuration
M0, M1, M2 = Output with proper level after configuration
VS0,1,2 = Output high after configuration
U11
CXO7050T3 24MHz
24MHZ1
24MHZ2
R27 33R
R29 33R
C76 100nF
U12
CXO7050T3 100MHz
MAINCLK
R31 33R
C77 100nF
UL1
UL2
UL3
UL4
R42 160R
R39 160R
R43 160R
R44 160R
D5 KP-1608SGD
D6 KP-1608SGD
D7 KP-1608SGD
D8 KP-1608SGD
S3
S4
PB1
PB2
SW PB DTSM61N
S5A
S5B
S5C
S5D
S5E
S5F
S5G
S5H
US1
US2
US3
US4
US5
US6
US7
US8
CHS-08TA
Optional, can also be equipped with x2, x4 and x6 switch.
Hardware Revisions:
REV3 REV2 REV1 REV0
OPEN OPEN OPEN OPEN -> Revision 00
OPEN OPEN OPEN CLOSE -> Revision 01
...
Variants:
VAR0 VAR1 VAR2 VAR3 VAR4 VAR5
OPEN OPEN OPEN OPEN OPEN OPEN -> EVAL 01
USB onboard, USB Powered, 2.5V VCCAUX, 3.3V VCCIO0
OPEN OPEN OPEN OPEN OPEN CLOSE -> Production 01
USB not onboard, B2B powered, Dipswitch 8 and pushbuttons omitte
3.3V VCCIO0
OPEN OPEN OPEN OPEN CLOSE OPEN -> EVAL 01
USB onboard, B2B Powered, 2.5V VCCAUX, 3.3V VCCIO0
REV0
REV1
REV2
REV3
VAR0
VAR1
VAR2
VAR3
VAR4
VAR5
0R
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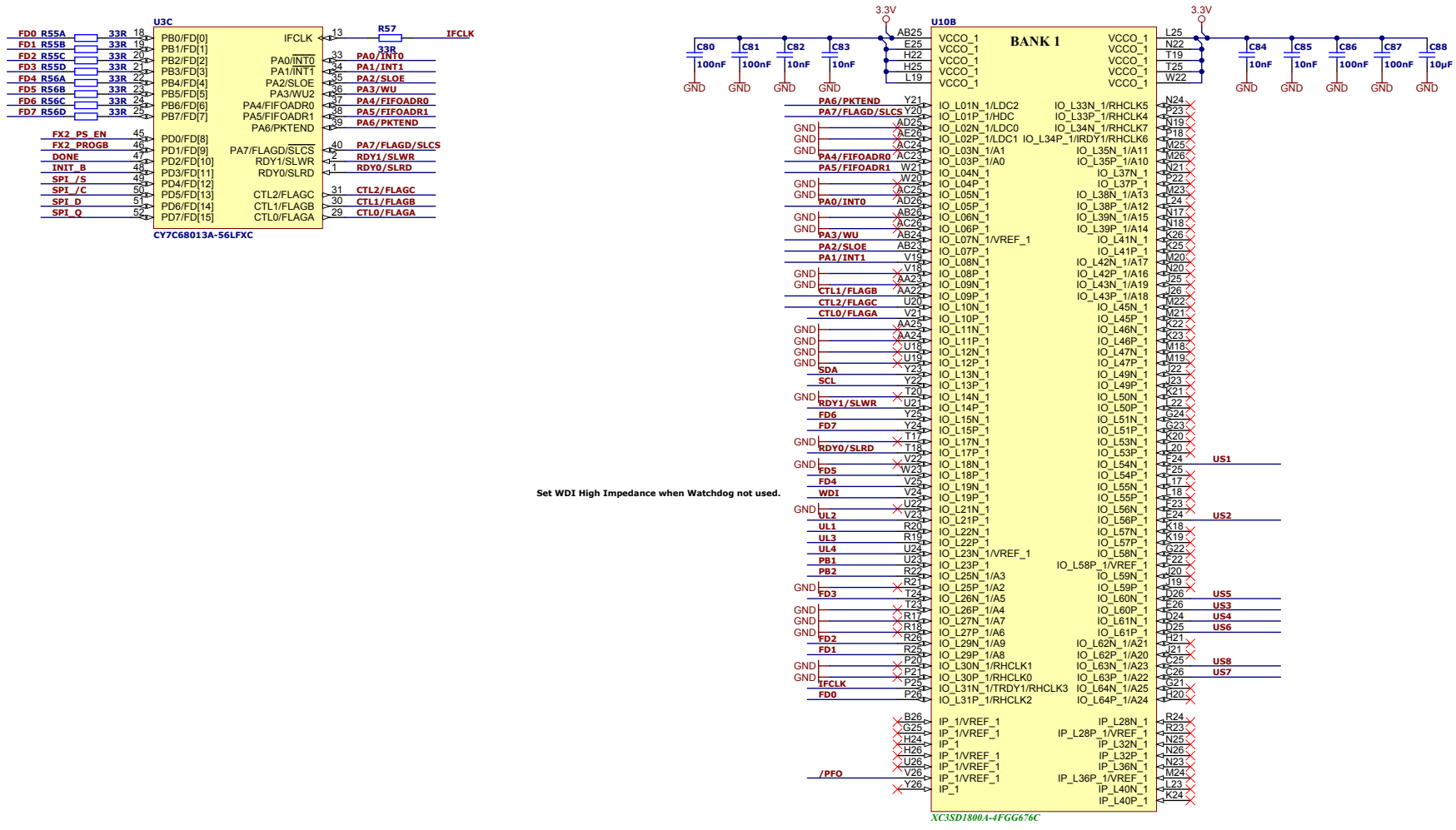
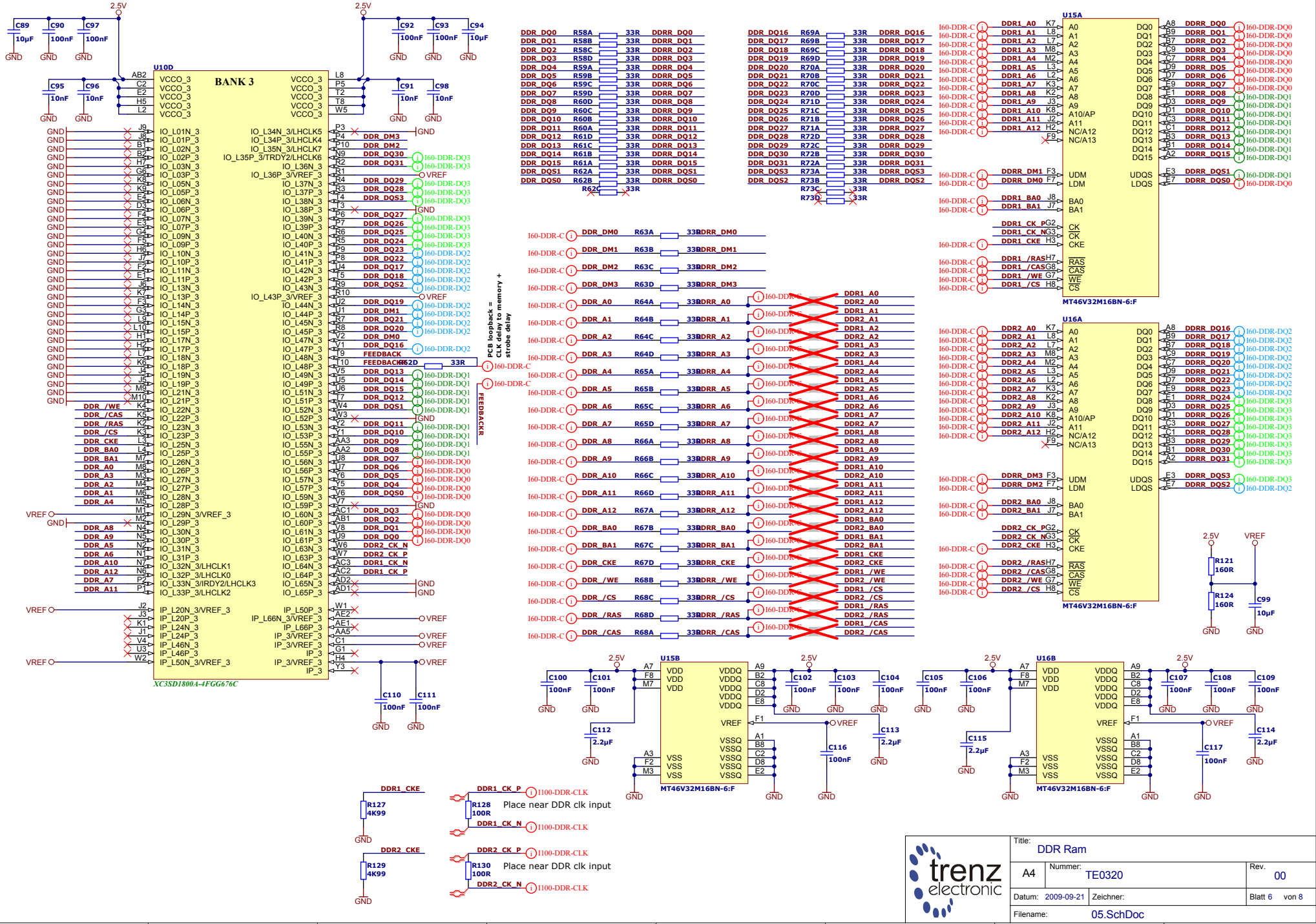
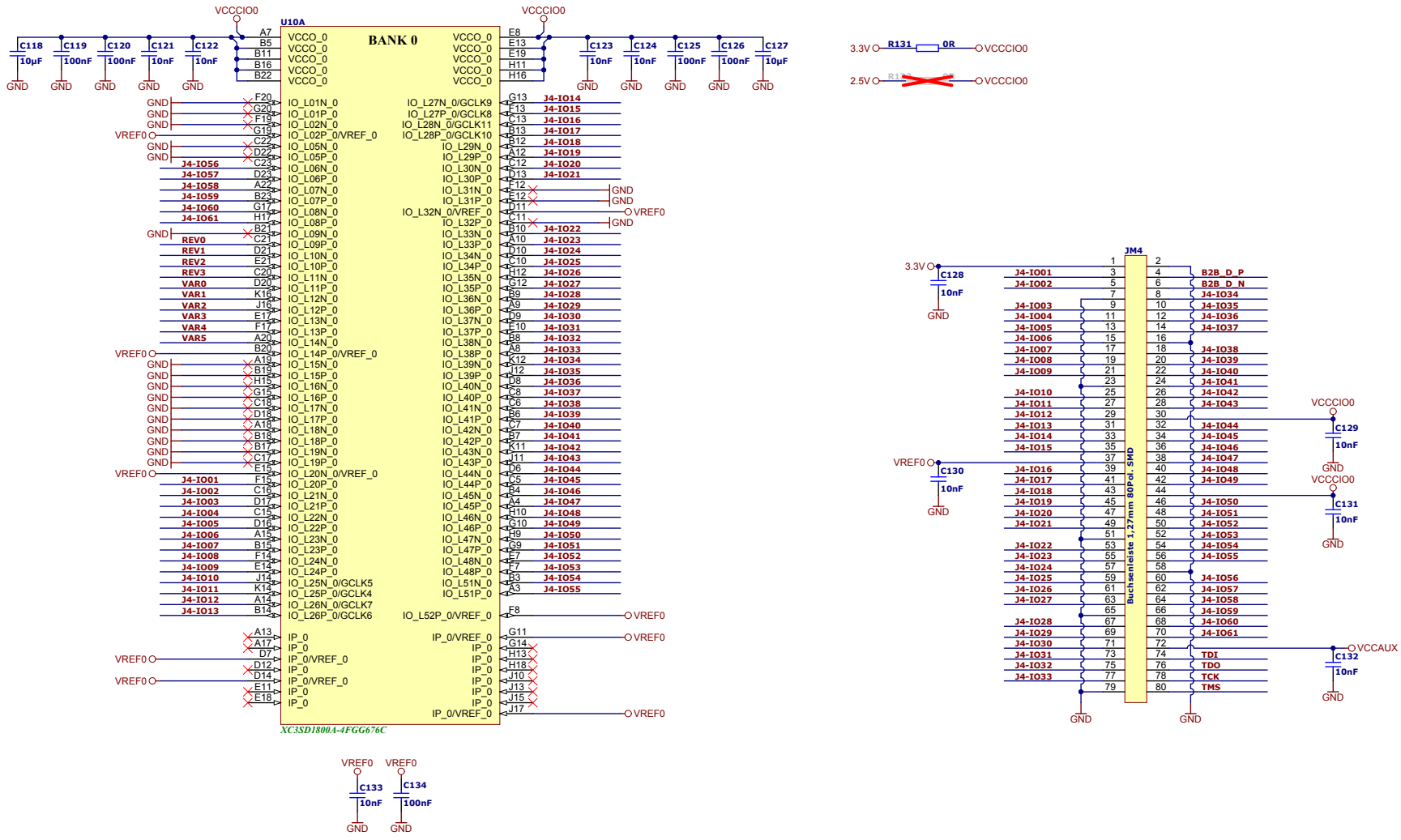
Title: Configuration and Clock
A4
Nummer: TE0320
Rev. 00
Datum: 2009-09-21
Zeichner:
Blatt 4 von 8
Filename: 03.SchDoc

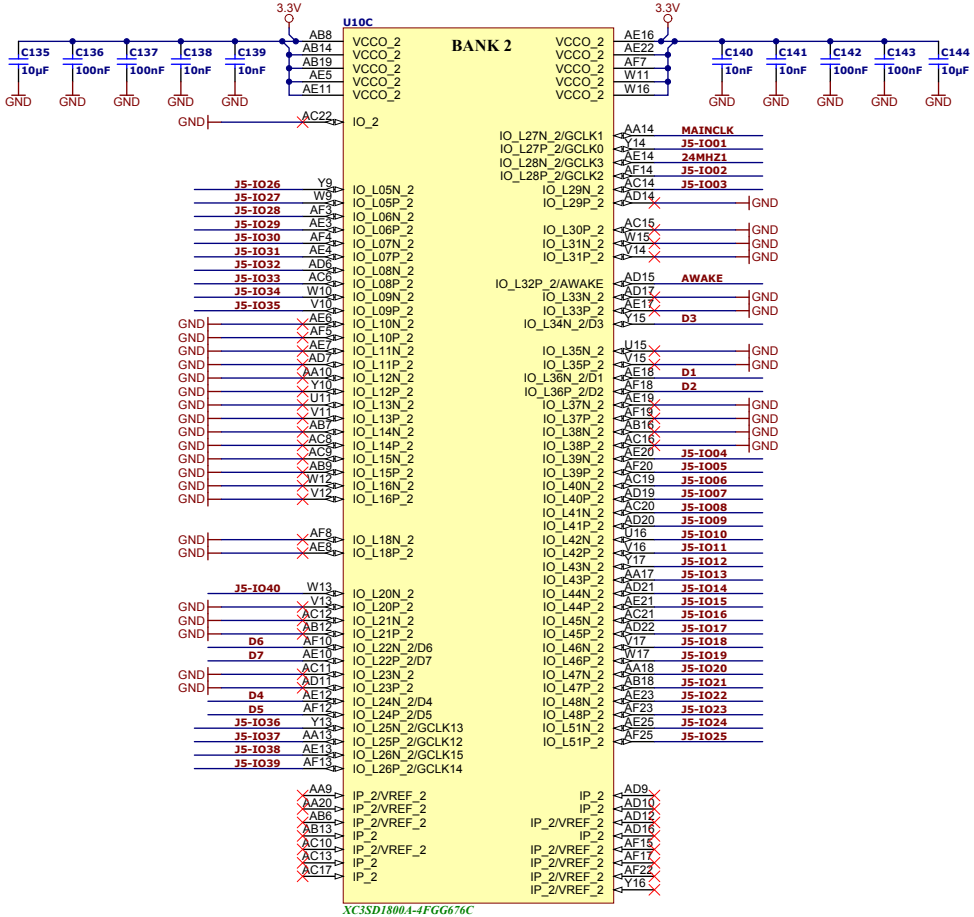


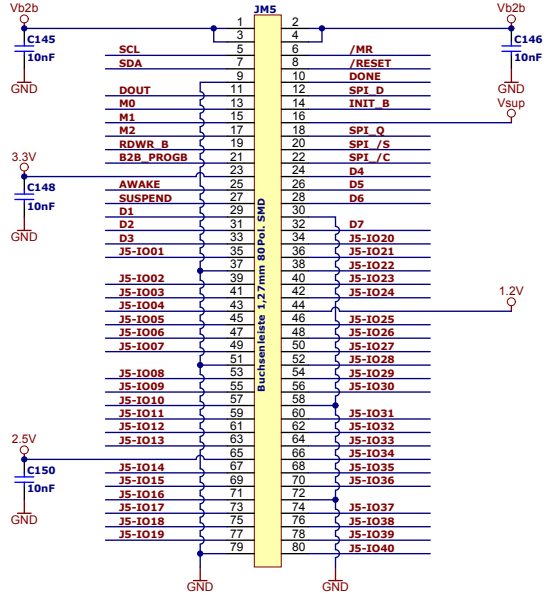
Title: FX2 USB			
A4	Nummer: TE0320		Rev. 00
Datum: 2009-09-21	Zeichner:		Blatt 5 von 8
Filename: 04.SchDoc			


U10D
BANK 3
XC3SD1800A-4FGG676C
U15A
U16A
U15B
U16B
MT46V32M16BN-6:F
PCB loopback = CLK delay to memory + strobe delay
FEEDBACK
Place near DDR clk input
Place near DDR clk input
Title: DDR Ram
A4
Nummer: TE0320
Rev. 00
Datum: 2009-09-21
Zeichner:
Blatt 6 von 8
Filename: 05.SchDoc
trenz electronic



Title: B2B Connector J4		
A4	Nummer: TE0320	Rev. 00
Datum: 2009-09-21	Zeichner:	Blatt 7 von 8
Filename: 06.SchDoc		





trenz electronic	Title: B2B Connector J5		
	A4	Nummer: TE0320	Rev. 00
	Datum: 2009-09-21	Zeichner:	Blatt 8 von 8
	Filename: 07.SchDoc		