INCH-POUND

MIL-M-38510/238B
16 December 2003
SUPERSEDING
MIL-M-38510/238A
9 March 1981

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, MOS, 4096 BIT STATIC RANDOM ACCESS MEMORY (RAM), MONOLITHIC SILICON

Inactive for new design after 24 July 1995.

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF 38535

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, N-channel static MOS, 4096 bit random access memories. Two product assurance classes and a choice of case outlines/lead finish are provided for each type and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.3).

1.2 Part or Identifying Number (PIN). The PIN should be in accordance with MIL-PRF-38535, and as specified herein.

1.2.1 Device types. The device types should be as follows:

Device type	Circuit	Address access time
01 (T_C = -55°C “instant-on” to +125°) [1]	4096 words/1-bit	t_{AA} = 85 ns
02 (T_C = -55°C “instant-on” to +125°) [1]	1024 words/4-bit	t_{AA} = 450 ns
03 (T_C = -55°C “instant-on” to +125°) [1]	4096 words/1-bit	t_{AA} = 70 ns
04 (T_C = -55°C “instant-on” to +125°) [1]	1024 words/4-bit	t_{AA} = 250 ns
05 (T_C = -55°C “instant-on” to +125°) [1]	4096 words/1-bit	t_{AA} = 55 ns
06 (T_C = -55°C “instant-on” to +125°) [1]	1024 words/4-bit	t_{AA} = 70 ns
07 (T_C = -55°C “instant-on” to +125°) [1]	4096 words/1-bit	t_{AA} = 45 ns

1.2.2 Device class. The device class should be the product assurance level as defined in MIL-PRF-38535.

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[1] $T_C = T_A$ at test time equals zero. “Instant-on” is defined as all functional characteristics guaranteed at all temperatures 50 ms after power is applied.

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, 3990 East Broad St., Columbus, OH 43216-5000, or emailed to bipolar@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at www.dodssp.daps.mil.

AMSC N/A FSC 5962

1.2.3 Case outlines. The case outlines should be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
V	GDIP1-T18 or CDIP2-T18	18	Dual-in-line

1.3 Absolute maximum ratings.

Voltage on any pin with respect to ground (01, 02)	-1.5 V to +7.0 V dc 2/
Voltage on any pin with respect to ground (03, 04, 05, 06, 07)	-3.5 to +7.0 V dc
Storage temperature range	-65° to 150°C
Power dissipation:	
Device type 01, 03, 05, 06, 07	1.2 W
Device type 02, 04	1.0 W
Lead temperature (soldering, 5 seconds)	270°C
Maximum junction temperature	T_J = 150°C 3/
Thermal resistance, junction to case (θ_{JC}):	25°C/W
Maximum DC output current:	
Device types 01, 03, 05, 06, 07	20 mA
Device types 02, 04	5 mA

1.4 Recommended operating conditions. 2/

Device types 01, 02, 03, 04, 05, 06, and 07	Min	Max	Units
Supply voltages:			
V_{CC}	4.5	5.5	Vdc
V_{SS}	0		Vdc
High-level input voltage	2.0	V_{CC}	Vdc
Low-level input voltage	-1.0	+0.8	Vdc
Case temperature	-55°	+125°	C
Device type 01			
Read cycle time (t_{RC})	85		ns
Address access time (t_{AA})		85	ns
CS access time (t_{ACS1}) 4/		85	ns
Chip select access time (t_{ACS2}) 5/		100	ns
Output hold time from address change (t_{OH})	5		ns

2/ Under absolute maximum ratings, the voltage values are with respect to the most negative supply voltage, V_{SS}. Throughout the remainder of this specification, the voltage values are with respect to V_{SS}.

3/ Maximum junction temperature (T_J) may be increased to 175°C during the burn-in and steady state life test.

4/ Chip deselected for greater than 55 ns prior to selection.

5/ Chip deselected for a finite time that is less than 55 ns prior to selection.

1.4 Recommended operating conditions – Continued.

Device types 01 - Continued	Min	Max	Units
Chip select to output in low-Z (t_{LZ}) 6/ 7/	10		ns
Chip deselect to output in high-Z (t_{HZ}) 6/ 7/	0	40	ns
Chip select to power-up time (t_{PU})	0		ns
Chip select to power-down time (t_{PD})		30	ns
Write cycle time (t_{WC})	85		ns
Pulse width, chip select to end of write (t_{CW})	70		ns
Address valid to end of write (${}_{AW}$)	70		ns
Pulse width, write (t_{WP})	55		ns
Data valid to end of write (t_{DW})	35		ns
Address set-up time (t_{AS})	0		ns
Write recovery time (t_{WR})	15		ns
Data on hold (t_{DH})	10		ns
Write enabled to output in high-Z (t_{WZ}) 7/	0	65	ns
Output active from end of write (t_{ow}) 7/	0		ns

Device type 02	Min	Max	Units
Read cycle time (t_{RC})	450		ns
Address access time (t_{AA})		450	ns
Chip select access time (t_{ACS})		120	ns
Output hold time from address change (t_{OH})	50		ns
Chip select to output in low-Z (t_{LZ}) 6/ 7/	20		ns
Chip deselect to output in high-Z (t_{HZ}) 6/ 7/	0	100	ns
Write cycle time (t_{WC})	450		ns
Pulse width, write (t_{WP})	200		ns
Data valid to end of write (t_{DW})	200		ns
Write recovery time (t_{WR})	0		ns
Data on hold (t_{DH})	0		ns
Write enabled to output in high-Z (t_{wz}) 7/	0	100	ns

Device type 03	Min	Max	Units
Read cycle time (t_{RC})	70		ns
Address access time (t_{AA})		70	ns
Chip select access time (t_{ACS1}) 8/		70	ns
Chip select access time (t_{ACS2}) 5/		80	ns
Output hold time form address change (t_{OH})	5		ns
Chip select to output in low-Z (t_{LZ}) 6/ 7/	10		ns
Chip deselect to output in high-Z (t_{HZ}) 6/ 7/	0	40	ns
Chip select to power-up time (t_{PU})	0		ns
Chip select to power-down time (t_{PD})		30	ns
Write cycle time (t_{WC})	70		ns
Pulse width, chip select to end of write (t_{CW})	55		ns
Address valid to end of write (t_{AW})	55		ns
Pulse width, write (t_{WP})	40		ns

6/ At any given temperature and voltage condition, t_{HZ} maximum is less than t_{LZ} mimimum both for a given device and from device to device.

7/ Transition is measured ±500 mV from steady state voltage with specified loading.

8/ Chip selected for greater than 55 ns prior to selection.

1.4 Recommended operating conditions – Continued.

Device types 03 - Continued	Min	Max	Units
Data valid to end of write (t_{DW})	30		ns
Address set-up time (t_{AS})	0		ns
Write recovery time (t_{WR})	15		ns
Data on hold time (t_{DH})	10		ns
Write enabled to output in high-Z (t_{WZ}) 7/	0	35	ns
Output active from end of write (t_{OW}) 7/	0		ns

Device type 04	Min	Max	Units
Read cycle time (t_{RC})	250		ns
Address access time (t_{AA})		250	ns
Chip select access time (t_{ACS})		85	ns
Output hold time from address change (t_{OH})	15		ns
Chip select to output in low-Z (t_{LZ}) 6/ 7/	10		ns
Chip deselect to output in high-Z (t_{HZ}) 6/ 7/	0	60	ns
Write cycle time (t_{WC})	250		ns
Pulse width, write (t_{WP})	135		ns
Data valid to end of write (t_{DW})	135		ns
Write recovery time (t_{WR})	0		ns
Data on hold time (t_{DH})	0		ns
Write enabled to output in high-Z (t_{WZ}) 7	0	60	ns

Device type 05	Min	Max	Units
Read cycle time (t_{RC})	55		ns
Address access time (t_{AA})		55	ns
Chip select access time (t_{ACS1}) 8/		55	ns
Chip select access time (t_{ACS2}) 5/		65	ns
Output hold time from address change (t_{OH})	5		ns
Chip select to output in low-Z (t_{LZ}) 6/ 7/	10		ns
Chip deselect to output in high-Z (t_{HZ}) 6/ 7/	0	30	ns
Chip select to power-up time (t_{PU})	0		ns
Ship select to power-down time (t_{PD})		20	ns
Write cycle time (t_{WC})	55		ns
Pulse width, chip select to end of write (t_{CW})	45		ns
Address valid to end of write (t_{AW})	45		ns
Pulse width, write (t_{WP})	25		ns
Data valid to end of write (t_{DW})	25		ns
Address set-up time (t_{AS})	0		ns
Write recovery time (t_{WR})	10		ns
Data on hold time (t_{DH})	10		ns
Write enabled to output in high-Z (t_{wz}) 7/	0	25	ns
Output active from end of write (t_{OW}) 7/	0		ns

Device type 06	Min	Max	Units
Read cycle time (t_{RC})	70		ns
Address access time (t_{AA})		70	ns
Chip select access time (t_{ACS1}) 8/		70	ns
Chip select access time (t_{ACS2}) 5/		80	ns
Output hold time form address change (t_{OH})	5		ns
Chip select to output in low-Z (t_{LZ}) 6/ 7/	20		ns
Chip deselect to output in high-Z (t_{HZ}) 6/ 7/	0	20	ns

1.4 Recommended operating conditions – Continued.

Device types 06 - Continued	Min	Max	Units
Chip select to power-up time (t_{PU})	0		ns
Chip select to power-down time (t_{PD})		30	ns
Write cycle time (t_{WC})	70		ns
Pulse width, chip select to end of write (t_{CW})	65		ns
Address valid to end of write (t_{AW})	65		ns
Address set-up time (t_{AS})	0		ns
Pulse width, write (t_{WP})	50		ns
Write recovery time (t_{WR})	5		ns
Data valid to end of write (t_{DW})	25		ns
Data on hold time (t_{DH})	0		ns
Write enabled to output in high-Z (t_{WZ}) 7/	0	25	ns
Output active from end of write (t_{OW}) 7/	0		ns
Device type 07			
Read cycle time (t_{RC})	45		ns
Address access time (t_{AA})		45	ns
Chip select access time (t_{ACS1}) 8/		45	ns
Chip select access time (t_{ACS2}) 5/		55	ns
Output hold time from address change (t_{OH})	5		ns
Chip select to output in low-Z (t_{LZ}) 6/ 7/	10		ns
Chip deselect to output in high-Z (t_{HZ}) 6/ 7/	0	30	ns
Chip select to power-up time (t_{PU})	0		ns
Chip select to power-down time (t_{PD})		20	ns
Write cycle time (t_{WC})	45		ns
Pulse width, chip select to end of write (t_{CW})	45		ns
Address valid to end of write (t_{AW})	45		ns
Pulse width, write (t_{WP})	30		ns
Data valid to end of write (t_{DW})	30		ns
Address set-up time (t_{AS})	0		ns
Write recovery time (t_{WR})	10		ns
Data on hold time (t_{DH})	10		ns
Write enabled to output in high-Z (t_{WZ}) 7	0	25	ns
Output active from end of write (t_{OW}) 7/	0		ns

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications and Standards. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38535	-	Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883	-	Test Method Standard for Microelectronics.
MIL-STD-1835	-	Interface Standard Electronic Component Case Outlines

(Copies of these documents are available online at http://assist.daps.dla.mil;quicksearch/ or www.dodssp.daps.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.4).

3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or other alternative approved by the qualifying activity.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.3.1 Terminal connections and logic diagrams. The terminal connections and logic diagrams shall be as specified on figure 1 and 2.

3.3.2 Truth tables. The truth tables and logic equations shall be as specified on figure 3.

3.3.4 Schematic circuits. The schematic circuits shall be maintained by the manufacturer and made available to the qualifying activity and the preparing activity (DSCC-VAS) upon request.

3.3.5 Case outlines. The case outlines shall be as specified in 1.2.3.

3.4 Lead material and finish. The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.5 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

3.6 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.7 Marking. Marking shall be in accordance with MIL-PRF-38535.

3.7.1 Certification/compliance mark. For product built in accordance with A.3.2.2 of MIL-PRF-38535, or as modified in the manufacturer’s QM plan, the “QD” certification mark shall be used in place of the “Q” or “QML” certification mark.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 46 (see MIL-PRF-38535, appendix A).

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with. MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with, MIL-PRF-38535 and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. Additional screening for space level product shall be as specified in MIL-PRF-38535, appendix B.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device types	Limits		Unit
				Min	Max	
Low-level input leakage current (all input pins)	I_{IL}	V_{CC} = 5.5 V V_{IN} = Gnd	All		10	µA
High-level input leakage current (all input pins)	I_{IH}	V_{CC} = 5.5 V V_{IN} = 5.5 V	All		10	µA
Output leakage current	I_{LO}	$\overline{CS}$ = V_{IH}, V_{CC} = 5.5 V V_{OUT} = Gnd to 4.5 V	All		50	µA
Power supply current	I_{CC}	V_{CC} = 5.5 V $\overline{CS}$ = V_{IL}, outputs open	01		160	mA
			02		100	mA
			03		180	mA
			04		70	mA
			05, 06, 07		180	mA
Standby current	I_{SB}	V_{CC} = 4.5 V to 5.5 V $\overline{CS}$ = V_{IH}	01, 03, 05, 07, 06		30	mA
Output low voltage	V_{OL}	I_{OL} = 2.1 mA	02, 04		0.4	V
		I_{OL} = 8.0 mA	01, 03, 05, 06, 07		0.4	V
Output high voltage	V_{OH}	I_{OH} = -1.0 mA	02, 04	2.4		V
		I_{OH} = -4.0 mA	01, 03, 05, 06, 07	2.4		V
Output Short circuit Current 3/ 4/	I_{OS}	V_{CC} = 5.5 V V_{OUT} = Gnd	All		300	mA
Input capacitance 4/	C_{IN}	V_{IN} = 0 V, f = 1 MHz T_C = 25°C	All		5	pF
Peak power on 4/	I_{PO}	V_{CC} = 4.5 V, $\overline{CS}$ = 2.4 V	01, 03, 05, 07		70	mA
			06		50	mA
Read cycle time 2/	t_{RC}	See table III	01	85		ns
			02	450		ns
			03	70		ns
			04	250		ns
			05	55		ns
			06	70		ns
			07	45		ns
Address access time	t_{AA}		01		85	ns
			02		450	ns
			03		70	ns
			04		250	ns
			05		55	ns
			06		70	ns
			07		45	ns
Chip select access time 5/	t_{ACS1}		01		85	ns
			02		120	ns
			03		70	ns
			04		85	ns
			05		55	ns
			06		70	ns
			07		45	ns

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ unless otherwise specified	Device types	Limits		Unit
				Min	Max	
Chip select access time 6/	t_{ACS2}	See table III	01		100	ns
			03		80	ns
			05		65	ns
			06		80	ns
			07		55	ns
Chip select to output in Low-Z 4/ 7/	t_{LZ}		01, 03, 04, 05, 07	10		ns
			02, 06	20		ns
Chip deselect to output in High-Z 4/ 7/	t_{HZ}		01, 03	0	40	ns
			02	0	100	ns
			04	0	60	ns
			05, 07	0	30	ns
			06	0	20	ns
Output hold from address change 4/	t_{OH}		01, 03, 05, 06, 07	5		ns
			02	50		ns
			04	15		ns
Chip select to power up time 4/	t_{PU}		01, 03, 05, 06, 07	0		ns
Chip deselect to power down time 4/	t_{PD}		01, 06		30	ns
			03, 05, 07		20	ns
Write cycle time	t_{WC}		01	85		ns
			02	450		ns
			03	70		ns
			04	250		ns
			05	55		ns
			06	70		ns
			07	45		ns
Chip select to end of write	t_{CW}		01	70		ns
			03	55		ns
			05, 07	45		ns
			06	65		ns
Address valid to end of write	t_{AW}		01	70		ns
			03	55		ns
			05, 07	45		ns
			06	65		ns
Address setup time	t_{AS}		01, 03, 05, 06, 07	0		ns
Write pulse width	t_{WP}		01	55		ns
			02	200		ns
			03	40		ns
			04	135		ns
			05	25		ns
			06	50		ns
			07	25		ns

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^\circ C \leq T_C \leq +125^\circ C$ unless otherwise specified	Device types	Limits		Unit
				Min	Max	
Write recovery time	t_{WR}	See table III	01, 03	15		ns
			02, 04	0		ns
			05, 07	10		ns
			06	5		ns
Data valid to end of write	t_{DW}		01	35		ns
			02	200		ns
			03	30		ns
			04	135		ns
			05, 06	25		ns
			07	25		ns
Data hold time	t_{DH}		01, 03 05, 07	10		ns
			02, 04, 06	0		ns
Write enabled to output in High-Z 4/ 7/	t_{WZ}		01	0	65	ns
			02	0	100	ns
			03	0	35	ns
			04	0	60	ns
			05, 06, 07	0	25	ns
Output active from end of write 4/ 7/	t_{OW}		01, 03, 05, 06, 07	0		ns

1/ Output levels are tested in static state and are specified over voltage range of V_{CC}.

2/ Unless otherwise specified, the dynamic load shall be in accordance with figure 4 (load A).

3/ Duration not exceed 1 second.

4/ Not tested.

5/ Complete terminal conditions are as specified in table III.

6/ Chip deselected for a finite time that is less than 55 ns prior to selection. (If the deselect time is 0 ns, the chip is by definition selected and access occurs according to read cycle no 1.)

7/ Transition is measured ±500 mV from steady state voltage using figure 4 (load B).

TABLE II. Electrical test requirements.

MIL-PRF-38535 test requirements	Subgroups (see table III)	
	Class S devices	Class B devices
Interim electrical parameters	2, 8*	NA
Final electrical test parameters	1**, 2, 3, 7**, 8	1**, 2, 3, 7**, 8
Group A test requirements	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8,
Group B test when using the method 5005 QCI option	1, 2, 3, 7, 8 9, 10, 11	N/A
Group C end-point electrical parameters	1, 2, 3,7, 8 9, 10, 11	1, 7
Group D end-point electrical parameters	1, 2, 3, 7, 8	1, 7

*Maximum Temperature only
**PDA applies to subgroups 1 and 7.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535 .

4.4 Technology Conformance inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II MIL-PRF-38535.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535. End-point electrical parameters shall be as specified in table II herein.

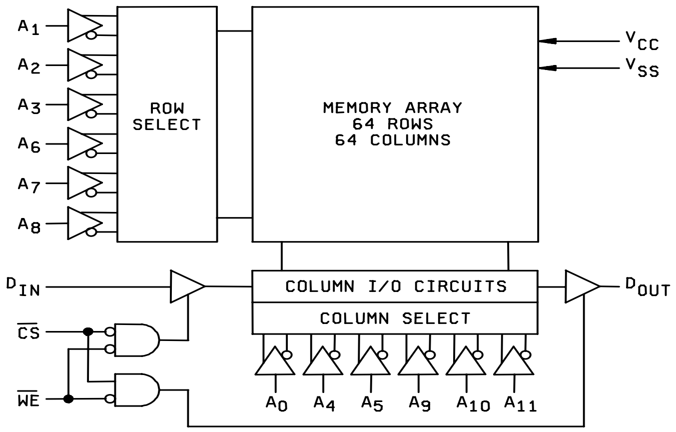
4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

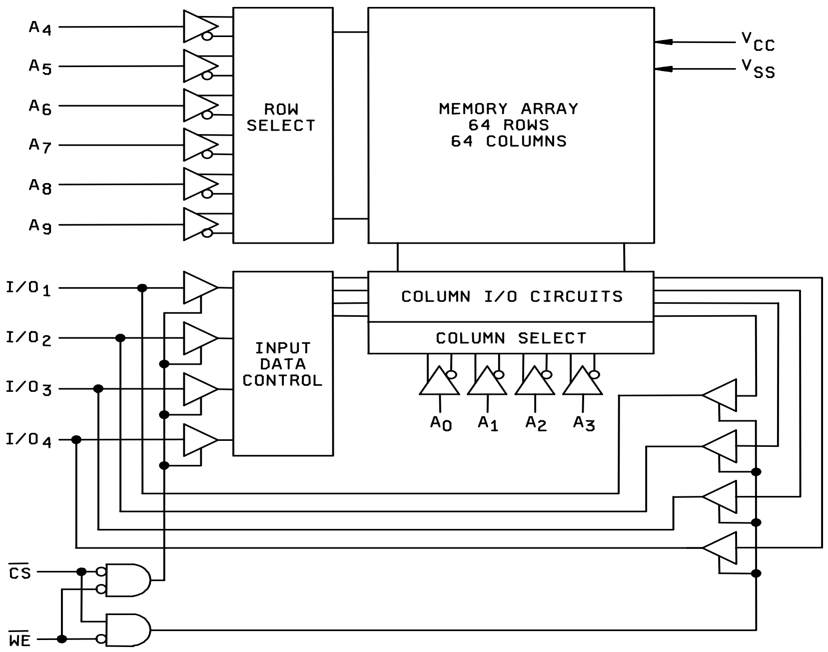
Pin number	Device types 01, 03, 05 and 07	Device types 02, 04 and 06
	Case V	Case V
1	A_0	A_6
2	A_1	A_5
3	A_2	A_4
4	A_3	A_3
5	A_4	A_0
6	A_5	A_1
7	D_{OUT}	A_2
8	$\overline{WE}$	$\overline{CS}$
9	V_{SS}	V_{SS}
10	$\overline{CS}$	$\overline{WE}$
11	D_{IN}	$1/0_4$
12	A_{11}	$1/0_3$
13	A_{10}	$1/0_2$
14	A_9	$1/0_1$
15	A_8	A_9
16	A_7	A_8
17	A_6	A_7
18	V_{CC}	V_{CC}

FIGURE 1. Terminal connections.

DEVICE TYPES 01,03,05 AND 07



DEVICE TYPES 02,04 AND 06



NOTE: Address numbering may vary between vendors.

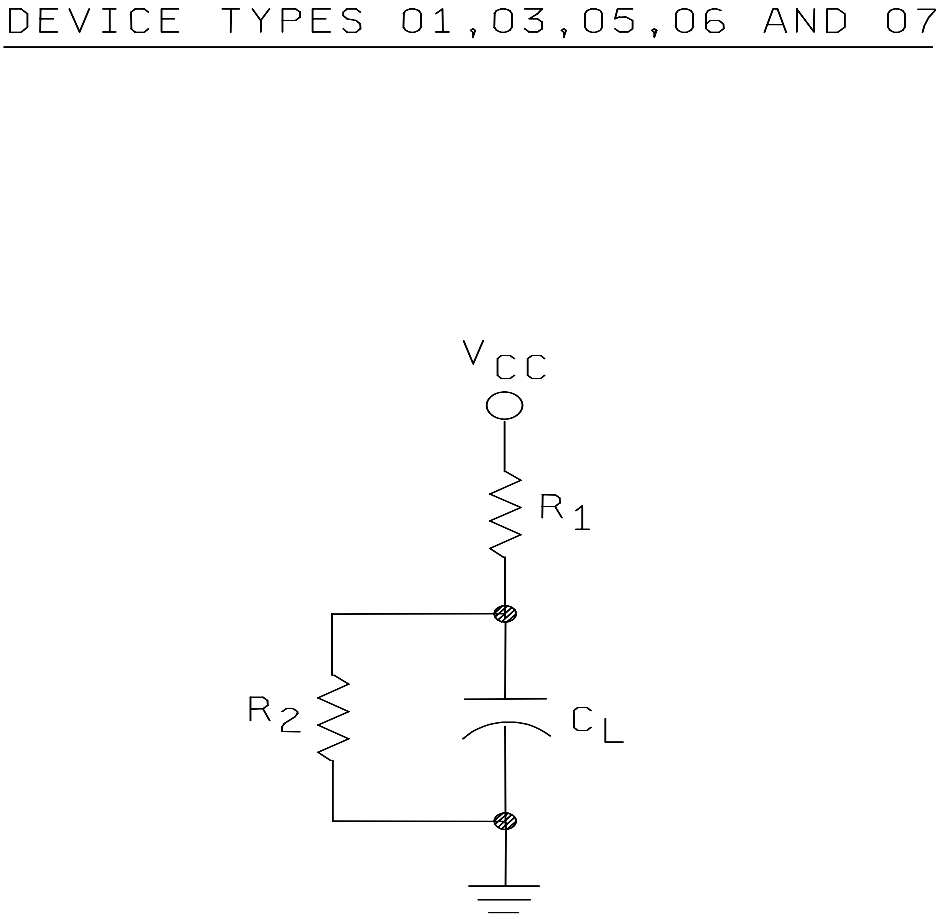
FIGURE 2. Block diagrams.

Device types 01, 02, 03, 04, 05, 06, and 07

$\overline{CS}$	$\overline{WE}$	Mode	01, 03, 05, 07	01, 03, 05, 06, 07	02, 04, 06
			Output	Power	I/O
H	X	Not selected	High Z	Stand by	High Z
L	L	Write	High Z	Active	D_{IN}
L	H	Read	D_{OUT}	Active	D_{OUT}

H = High voltage level.
L = Low voltage level.
X = Don’t care (high or low).

FIGURE 3. Truth table.

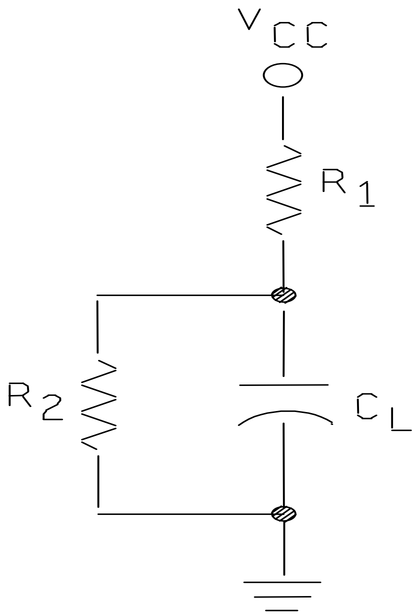


NOTES:

1. V_{CC} is defined in table III.
2. Load A: R1 = 480Ω ±5%; R2 = 255Ω ±5%; and C_L = 30 pF (including probe and jig capacitance).
3. Load B; R1 = 480Ω ±5%; R2 = 255Ω ±5%; and C_L = 5 pF (including probe and jig capacitance).

FIGURE 4. Dynamic load for switching tests.

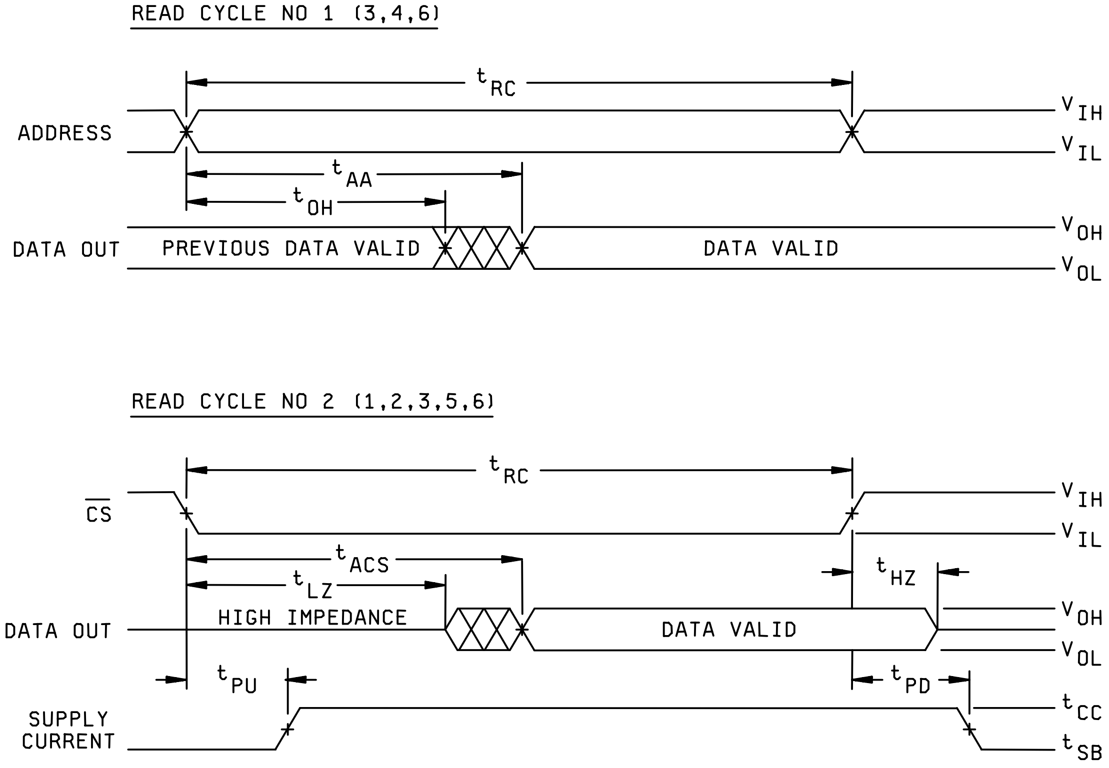
DEVICE TYPE 02 AND 04



NOTES:

1. V_{CC} is defined in table III.
2. C_L = 100 pF total, including probe and jig capacitance.
3. R1 = 1.8 kΩ ±5%, R2 = 1 kΩ ±5%.

FIGURE 4. Dynamic load for switching tests - Continued.

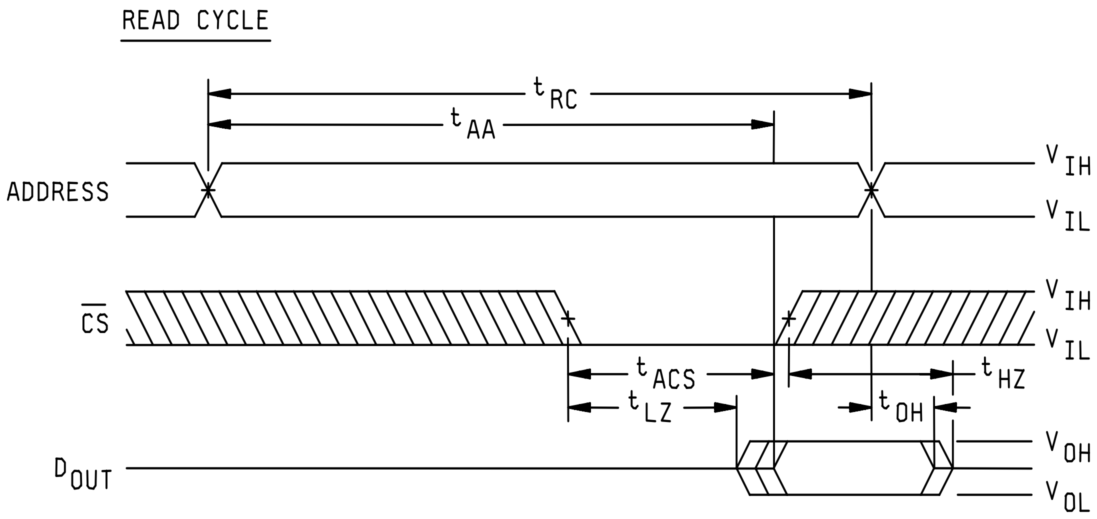


Wavefroms

NOTES:

1. Chip deselected for greater than 55 ns prior to selection.
2. Chip deselected for a finite time that is less than 55 ns prior to selection. (If the deselect time is 0 ns the chip is by definition selected and access occurs according to read cycle no. 1.)
3. $\overline{WE}$ is high for read cycles.
4. Device is continuously selected, $\overline{CS} = V_{IL}$.
5. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
6. See table I for limits and complete terminal conditions.
7. Input and output timing reference levels are 1.5 volts with input pulse levels of ground to 3.0 volts.
8. t_{LZ} and t_{HZ} are measured at ±500 mV from steady state with 5 pF load.

FIGURE 5. Read cycle waveforms and test conditions for device types 01, 03, 05, 06, and 07.

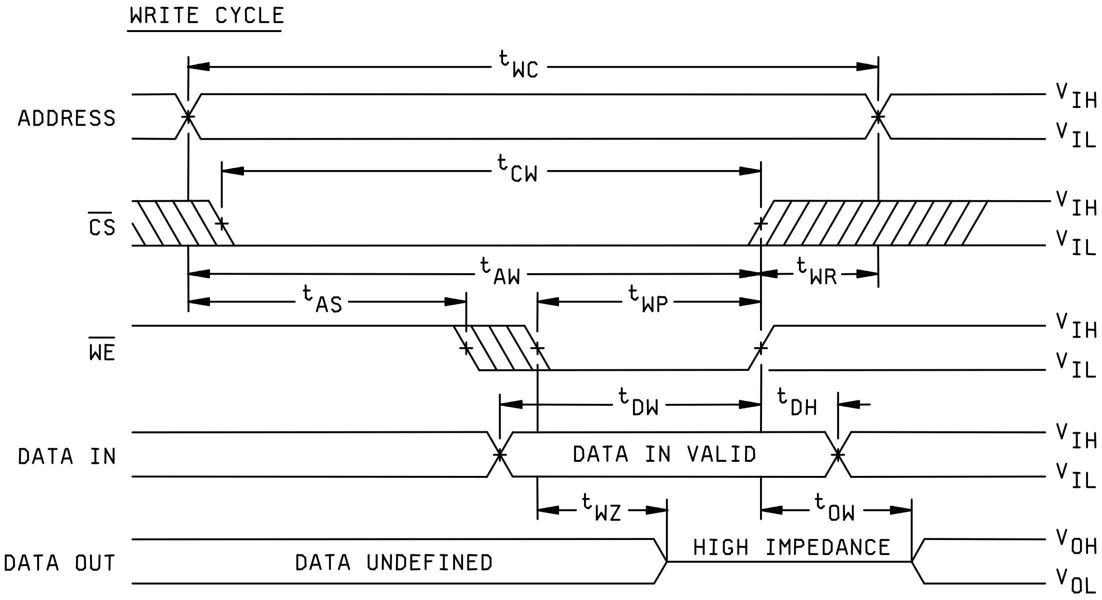


Waveforms

NOTES:

1. $\overline{\text{WE}}$ is high for a read cycle.
2. If the $\overline{\text{CS}}$ low transition occurs simultaneously with the $\overline{\text{WE}}$ low transitions, the output buffers remain in a high impedance state.
3. $\overline{\text{WE}}$ must be high during all address transitions.
4. Rise and fall times of input pulses ≤ 10 ns.
5. Input and output timing reference levels are 1.5 volts with input pulse levels of ground to 3.0 volts.
6. t_{hz} and t_{LZ} are measured at ±500 mV from steady state with 5 pF load.

FIGURE 5. Read cycle waveforms and test conditions for device types 02 and 04 – Continued.



Waveforms

NOTES:
1. See table 1 for limits and complete terminal conditions.
2. Input and output timing reference levels are 1.5 volts with input pulse levels of ground to 3.0 volts.
3. t_{OW} and t_{WZ} are measured at ±500 mV from steady state with 6 pF load.

FIGURE 6. Write cycle waveforms and test conditions for device types 01, 02, 03, 04, 05, 06, and 07.

TABLE III. Group A inspection for device type 01, 03, 05, and 07.

Terminal conditions (pins not designated may be high ≥ 2.0 V; or low ≤ 0.8 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Case V	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	Algorithms 1/	Measured terminal	Test Limits		Unit
			Test no.	A_0	A_1	2	3	4	5	D_{OUT}	$\overline{WE}$	V_{SS}	$\overline{CS}$	D_{IN}	11	A_{10}	9	8	7	6	CC			Min	Max	
1 Tc = 25°C	V_{OH}	3006	1	GND	GND A	GND A	GND A	GND A	GND	-4 mA	4.5 V	GND	GND	GND A	GND	GND A	GND A	GND A	GND A	GND V	4.5 V		D_{OUT}	2.4		V
“	V_{OL}	3007	2	GND	GND	“	“	“	“	+ 8 mA	4.5 V	“	“	“	“	“	“	“	“	“	4.5 V		D_{OUT}		0.4 V	V
“	I_{IH}	3010	3	5.5 V	GND	“	“	“	“		GND	“	“	“	“	“	“	“	“	“	5.5 V		A_0		10	µA
“	“	“	4	GND	5.5 V	“	“	“	“		“	“	“	“	“	“	“	“	“	“	“		1			“
“	“	“	5	“	GND	5.5 V					“	“	“	“	“	“	“	“	“	“	“		2			“
“	“	“	6	“	“	GND	5.5 V				“	“	“	“	“	“	“	“	“	“	“		3			“
“	“	“	7	“	“	“	GND	5.5 V			“	“	“	“	“	“	“	“	“	“	“		4	“		“
“	“	“	8	“	“	“	“	GND	5.5 V			“	“	“	“	“	“	“	“	“	“		5	“		“
“	“	“	9	“	“	“	“	“	GND		5.5 V	“	“	“	“	“	“	“	“	“	“	A	$\overline{WE}$	“ “		“
“	“	“	10	“	“	“	“	“	“	“	GND	“	5.5 V	“	“	“	“	“	“	“	“	A A	$\overline{CS}$	“		“
“	“	“	11	“	“	“	“	“	“			“	GND	5.5 V	“	“	“	“	“	“	“	A	IN	“	“	“
“	“	“	12	“	“	“	“	“	“			“	“	GND	5.5 V	“	“	“	“	“	“	A	11	“	“	“
“	“	“	13	“	“	“	“	“	“			“	“	“	GND	5.5 V	“	“	“	“	“		10		“	“
“	“	“	14	“	“	“	“	“	“	“		“	“	“	“	GND	5.5 V	“	“	“	“		A_9		“	“
“	“	“	15	“	“	“	“	“	“	“		“	“	“	“	“	GND	5.5 V	“	“	“		A_8		“	“
“	“	“	16	“	“	“	“	“	“	“		“	“	“	“	“	“	GND	5.5 V	“	“	D	7		“	“
“	“	“	17	“	“	“	“	“	“	“		“	“	“	“	“	“	“	GND	5.5 V	“	A	6		“	“
“	I_{IL}	3009	18	“	“	“	“	“	“	“		“	“	“	“	“	“	“	“	GND	“	A	0		“	“
“	“	“	19	“	“	“	“	“	“	“		“	“	“	“	“	“	“	“	“	“		1			“
“	“	“	20	“	“	“	“	“	“	“		“	“	“	“	“	“	“	“	“	“		2			“
“	“	“	21	“	“	“	“	“	“	“		“	“	“	“	“	“	“	“	“	“	A	3			“
“	“	“	22	“	“	“	“	“	“	“		“	“	“	“	“	“	“	“	“	“	A	4	“		“
“	“	“	23	“	“	“	“	“	“	“		“	“	“	“	“	“	“	“	“	“	A	5	“		“
“	“	“	24	“	“	“	“	“	“	“ “		“	“	“	“	“	“	“	“	“	“	A A	$\overline{WE}$	“ “		“
“	“	“	25	“	“	“	“	“	“	“		“	“	“	“	“	“	“	“	“	“	A	$\overline{CS}$	“ “		“
“	“	“	26	“	“	“	“	“	“	“		“	“	“	“	“	“	“	“	“	“	A	IN		“	“
“	“	“	27	“	“	“	“	“	“	“		“	“	“	“	“	“	“	“	“	“	A	11	“	“	“
“	“	“	28	“	“	“	“	“	“			“	“	“	“	“	“	“	“	“	“		10		“	“
“	“	“	29	“	“	“	“	“	“	“		“	“	“	“	“	“	“	“	“	“		9		“	“

“
“
“

See footnotes at end of device types 01, 03, 05 and 07.

D
A
A
A

TABLE III. Group A inspection for device type 01, 03, 05, and 07 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V; or low ≤ 0.8 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Case V	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	Algorithms 1/	Measured terminal	Test Limits		Unit
			Test no.	A_0	A_1	2	3	4	5	D_{OUT}	$\overline{WE}$	V_{SS}	$\overline{CS}$	D_{IN}	11	A_{10}	9	8	7	6	CC			Min	Max	
1 Tc = 25°C	I_{IL}	3009	30	GND	GND A	GND A	GND A	GND A	GND		GND	GND	GND	GND A	GND	GND A	GND A	GND A	GND A	GND V	5.5 V		A_8		10	µA
“	I_{IL}	3009	31	GND	GND	GND	GND	GND	GND		GND	“	GND	GND	GND	GND	GND	GND	GND	GND	5.5 V		A_7		10	“
“	I_{IL}	3009	32	GND	GND	GND	GND	GND	GND		GND	“	GND	GND	GND	GND	GND	GND	GND	GND	5.5 V		A_6		10	“
“	I_{L01}		33							4.5 V	2.0 V	“	2.0 V	2.0 V							4.5 V		D_{OUT}		50	“
“	I_{L01}		34							5.5 V	“	“	“	“							5.5 V		D_{OUT}			“
“	I_{L02}		35							0.4 V	“	“	“	“							4.5 V		D_{OUT}			“
“	I_{L02}		36							0.4 V	“	“	“	“							5.5 V		D_{OUT}			“
“	I_{SB}		37	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	GND	GND	“	4.5	GND	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	4.5 V		$_{CC}$	“	30	mA
“	I_{SB}		38	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	GND	GND	“	5.5 V	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V		$_{CC}$	“	30	“
“	I_{CC}		39	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	GND	GND	“	GND	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V		$_{CC}$	“	_/	“
2	Same tests, terminal conditions, and limits as subgroup 1, except T_C = 125°C.																									
3	Same tests, terminal conditions, and limits as subgroup 1, except T_C = -55°C.																					V V		2		
BIT STRESS TEST			40	3/	3/	3/	3/	3/	3/	3/	3/	GND	3/	3/	3/	3/	3/	3/	3/	3/	3/	CKBD V and $\overline{CKBD}$	D_{OUT}	V_{OL} <1.5	V_{OH} >1.5	V
7	t_{AA}	Fig. 5, 6	41	4/	4/	4/	4/	4/	4/	4/	4/	“	4/	4/	4/	4/	4/	4/	4/	4/	4.5 V	“	“	“	“	“
T_C = 25°C	“	“	42	4/	4/	4/	4/	4/	4/	4/	4/	“	4/	4/	4/	4/	4/	4/	4/	4/	5.5 V	“	“	“	“	“
“	“	“	43	5/	5/	5/	5/	5/	5/	5/	5/	“	5/	5/	5/	5/	5/	5/	5/	5/	4.5 V	“	“	“	“	“
“	“	“	44	5/	5/	5/	5/	5/	5/	5/	5/	“	5/	5/	5/	5/	5/	5/	5/	5/	5.5 V	“	“	“	“	“
“	“	“	45	6/	6/	6/	6/	6/	6/	6/	6/	“	6/	6/	6/	6/	6/	6/	6/	6/	4.5 V	“	“	“	“	“
“	“	“	46	6/	6/	6/	6/	6/	6/	6/	6/	“	6/	6/	6/	6/	6/	6/	6/	6/	5.5 V	“	“	“	“	“
“	“	“	47	7/	7/	7/	7/	7/	7/	7/	7/	“	7/	7/	7/	7/	7/	7/	7/	7/	4.5 V	“	“	“	“	“
“	“	“	48	7/	7/	7/	7/	7/	7/	7/	7/	“	7/	7/	7/	7/	7/	7/	7/	7/	5.5 V	“	“	“	“	“
“	“	“	49	8/	8/	8/	8/	8/	8/	8/	8/	“	8/	8/	8/	8/	8/	8/	8/	8/	4.5 V	“	“	“	“	“
“	“	“	50	8/	8/	8/	8/	8/	8/	8/	8/	“	8/	8/	8/	8/	8/	8/	8/	8/	5.5 V	“	“	“	“	“
“	“	“	51	9/	9/	9/	9/	9/	9/	9/	9/	“	9/	9/	9/	9/	9/	9/	9/	9/	4.5 V	“	“	“	“	“
“	“	“	52	9/	9/	9/	9/	9/	9/	9/	9/	“	9/	9/	9/	9/	9/	9/	9/	9/	5.5 V	“	“	“	“	“
“	t_{ACS1}	“	53	10/	10/	10/	10/	10/	10/	10/	10/	“	10/	10/	10/	10/	10/	10/	10/	10/	5.5 V	“	“	“	“	“
“	t_{ACS2}	“	54	10/	10/	10/	10/	10/	10/	10/	10/	“	10/	10/	10/	10/	10/	10/	10/	10/	5.5 V	“	“	“	“	“

See footnotes at end of device types 01, 03, 05 and 07.

TABLE III. Group A inspection for device type 01, 03, 05, and 07 - Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V; or L ≤ 0.8 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Case V	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	Algorithms 1/	Measured terminal	Test Limits		Unit
			Test no.	A_0	A_1	$_2$	$_3$	$_4$	$_5$	D_{OUT}	$\overline{WE}$	V_{SS}	$\overline{CS}$	D_{IN}	$_{11}$	A_{10}	$_9$	$_8$	$_7$	$_6$	$_{CC}$			Min	Max	
7 Tc = 25°C	t_{ACS1}	Fig. 5, 6	55	10/	10/ A	10/ A	10/ A	10/ A	10/	10/	10/	GND	10/	10/ A	10/	10/ A	10/ A	10/ A	10/ A	10/ V	4.5 V	CKBD and $\overline{\text{CKBD}}$	D_{OUT}	V_{OL} <1.5	V_{OH} >1.5	V
7 Tc = 25°C	t_{ACS2}	Fig. 5, 6	56	10/	10/	10/	10/	10/	10/	10/	10/	GND	10/	10/	10/	10/	10/	10/	10/	10/	4.5 V	CKBD and $\overline{\text{CKBD}}$	D_{OUT}	V_{OL} <1.5	V_{OH} >1.5	V
8	Same tests, terminal conditions, and limits as subgroup 7, except T_C = 125°C and -55°C																									
9	t_{AA}	Fig. 5, 6	57	11/	11/	11/	11/	11/	11/	11/	11/	GND	11/	11/	11/	11/	11/	11/	11/	11/	4.5 V	GALPAT and GALRESH	D_{OUT}		12/	ns
Tc = 25°C	t_{AA}	“	58	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	“	“		12/	
“	t_{ACS1}	“	59	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“	“		13/	“
“	t_{ACS1}	“	60	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	“	“		13/	“
“	t_{ACS2}	“	61	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“	“		14/	“
“	t_{ACS2}	“	62	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	“	“		14/	“
“	t_{WC}	“	63	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“	“	15/		“
“	t_{WC}	“	64	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	“	“	15/		“
“	t_{CW}		65	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“	“	16/		
“	t_{CW}	“	66	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	“	“	16/		
“	t_{AW}	“	67	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“	“	17/		
“	t_{AW} “	“	68	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	“	“	17/	“	
“	t_{AS}	“	69	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“	“	0	“	
“	t_{AS}	“	70	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	“	“	0	“	
“	t_{WP}	“	71	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“	“	18/	“	
“	t_{WP}	“	72	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	“	“	18/	“	
“	t_{WR}	“	73	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“	“	19/	“	
“	t_{WR}	“	74	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	“	“	19/	“	
“	t_{DW}	“	75	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“	“	20/	“	
“	t_{DW}	“	76	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	“	“	20/	“	
“	t_{DH}	“	77	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“	“	10	“	“
“	t_{DH}	“	78	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	“	“	10	“	“

“

See footnotes at end of device types 01, 03, 05 and 07.

TABLE III. Group A inspection for device type 01, 03, 05, and 07 - Continued.

Terminal conditions (pins not designated may be high ≥ 2.0 V; or low ≤ 0.8 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Case V	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	Algorithms 1/	Measured terminal	Test Limits		Unit
			Test no.	A_0	A_1	A_2	A_3	A_4	A_5	D_{OUT}	$\overline{WE}$	V_{SS}	$\overline{CS}$	D_{IN}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	V_{CC}			Min	Max	
10	Same tests, terminal conditions, and limits as subgroup 9, except T_C = 125°C.																									
11	Same tests, terminal conditions, and limits as subgroup 9, except T_C = -55°C.																									

1/ See appendix for description of algorithms.
2/ I_{CC} = 160 for device type 01; 180 for device types 03, 05 and 07.
3/ V_{IL} = GND, V_{IH} = 6.0 V, pause time = 250 ms/loop max, $\overline{CS}$ = high, only performed once at 125°C, and V_{CC} = 0.7 V min.
4/ V_{IL} = 0.8 V and V_{IH} = 2.0 V.
5/ Algorithm has 60 ms where chip is deselected between the write.
6/ V_{IL} = GND, V_{IH} = 3.0 V, and all address setup times are shown at minimum.
7/ V_{IL} = GND, V_{IH} = 3.0 V and all write pulse timing are at a minimum.
8/ V_{IL} = GND, V_{IH} = 3.0 V and all address ending timing are at minimums.
9/ V_{IL} = GND, V_{IH} = 3.0 V, and t_{AA} is measured at minimum timing.
10/ V_{IL} = GND, V_{IH} = 3.0 V, t_{ACS1} and t_{ACS2} are measured at minimum timing.
11/ V_{IL} = 0.8 V, V_{IH} = 2.0 V, and all parameters are measured at minimum timing.
12/ t_{AA} = 85 ns for device type 01; 70 ns for device type 03; 55 ns for device type 05; 45 ns for device type 07.
13/ t_{ACS1} = 85 ns for device type 01; 70 ns for device type 03; 55 ns for device type 05; 45 ns for device type 07.
14/ t_{ACS2} = 100 ns for device type 01; 80 ns for device type 03; 65 ns for device type 05; 555 ns for device type 07.
15/ t_{WC} = 85 ns for device type 01; 70 ns for device type 03; 55 ns for device type 05; 45 ns for device type 07.
16/ t_{CW} = 70 ns for device type 01; 55 ns for device type 03; 45 ns for device types 05 and 07.
17/ t_{AW} = 70 ns for device type 01; 55 ns for device type 03; 45 ns for device types 05 and 07.
18/ t_{WP} = 55 ns for device type 01; 40 ns for device type 03; 25 ns for device type 05; 25 ns for device type 07.
19/ t_{WR} = 15 ns for device type 01 and 03; 10 ns for device type 05 and 07.
20/ t_{DW} = 35 ns for device type 01; 30 ns for device type 03; 25 ns for device type 05; 25 ns for device type 07.

TABLE III. Group A inspection for device type 02 and 04.
Terminal conditions (pins not designated may be high ≥ 2.0 V; or low ≤ 0.8 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Case V	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	Algorithms 1/	Measured terminal	Test Limits		Unit
			Test no.	A_6	A_5	4	3	0	1	A_2	$\overline{CS}$	V_{SS}	$\overline{WE}$	I/O_4	I/O_3	I/O_2	I/O_1	9	8	7	CC			Min	Max	
1	V_{OH}	3006	1	GND	GND A	GND A	GND A	GND A	GND	GND	GND	GND	3.0 V	-1.0 mA			A	GND A	GND A	GND V	4.5 V		I/O_4	2.4		V
Tc = 25°C	“	“	2	“	“	“	“	“	“	“	“	“	“		-1.0 mA			“	“	“	“		I/O_3	“		
“	“	“	3	“	“	“	“	“	“	“	“	“	“			-1.0 mA			“	“	“		I/O_2	“		
“	“	“	4	“	“	“	“	“	“	“	“	“	“				-1.0 mA	“	“	“	“		I/O_1	“		
“	V_{OL}	3007	5	“	“	“	“	“	“	“	“	“	“	2.1 mA				“	“	“	“		I/O_4		0.4	“
“	“	“	6	“	“	“	“	“	“	“	“	“	“		2.1 mA		“		“	“	“		I/O_3		“	“
“	“	“	7	“	“	“	“	“	“	“	“	“	“			2.1 mA			“	“	“		I/O_2		“	“
“	“	“	8	“	“	“	“	“	“	“	“	“	“				2.1 mA	“	“	“	“		I/O_1			“
“	I_{IH}	3010	9	5.5 V	“	“	“	“	“	“	“	“	“	GND	GND	GND	GND	“	“	“	5.5 V		6	“	10	µA
“	“	“	10	GND	5.5 V	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“		5	“		“
“	“	“	11	“	GND	5.5 V	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“		4	“		“
“	“	“	12	“	“	GND	5.5 V	“	“	“	“	“	“	“	“	“	“	“	“	“	“		3	“		“
“	“	“	13	“	“	“	GND	5.5 V	“	“	“	“	“	“	“	“	“	“	“	“	“		0	“		“
“	“	“	14	“	“	“	“	GND	5.5 V	“	“	“	“	“	“	“	“	“	“	“	“	A	1	“		“
“	“	“	15	“	“	“	“	“	GND	5.5 V	“	“	“	“	“	“	“	“	“	“	“	A	2	“		“
“	“	“	16	“	“	“	“	“	“	GND	5.5 V	“	“	“	“	“	“	“	“	“	“	A A	$\overline{CS}$	“		“
“	“	“	17	“	“	“	“	“	“	“	GND	“	5.5 V	“	“	“	“	“	“	“	“	A A	$\overline{WE}$	“ “		“
“	“	“	18	“	“	“	“	“	“	“	“	“	GND	5.5 V	“	“	“	“	“	“	“	A	I/O_4	“		“
“	“	“	19	“	“	“	“	“	“	“	“	“	“	GND	5.5 V	“	“	“	“	“	“		I/O_3			“
“	“	“	20	“	“	“	“	“	“	“	“	“	“	“	GND	5.5 V	“	“	“	“	“		I/O_2	“		“
“	“	“	21	“	“	“	“	“	“	“	“	“	“	“	“	GND	5.5 V	“	“	“	“		I/O_1	“		“
“	“	“	22	“	“	“	“	“	“	“	“	“	“	“	“	“	GND	5.5 V	“	“	“		9	“		“
“	“	“	23	“	“	“	“	“	“	“	“	“	“	“	“	“	“	GND	5.5 V	“	“		8	“		“
“	“	“	24	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	GND	5.5 V	“		7	“		“
“	I_{IL}	3009	25	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	GND	“		6	“		“
“	“	“	26	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“		5	“		“
“	“	“	27	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	A	4	“		“
“	“	“	28	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	A	3	“		“
“	“	“	29	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	A	0	“		“
																						A A A A A		“ “		

See footnotes at end of device types 02 and 04.

TABLE III. Group A inspection for device type 02 and 04 - Continued.

Terminal conditions (pins not designated may be high ≥ 2.0 V; or low ≤ 0.8 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Case V	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	Algorithms 1/	Measured terminal	Test Limits		Unit
			Test no.	A_6	A_5	$_4$	$_3$	$_0$	$_1$	A_2	$\overline{CS}$	V_{SS}	$\overline{WE}$	I/O_4	I/O_3	I/O_2	I/O_1	$_9$	$_8$	$_7$	$_{CC}$			Min	Max	
1 Tc = 25°C	I_{IL}	3009	30	GND	GND A	GND A	GND A	GND A	GND	GND	GND	GND	GND	GND	GND	GND	GND A	GND A	GND A	GND V	5.5 V		A_1		10	µA
“	“	“	31	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“		$_2$		“	“
“	“	“	32	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“		$\overline{CS}$		“	“
“	“	“	33	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“		$\overline{WE}$			“
“	“	“	34	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	A	I/O_4			“
“	“	“	35	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“		I/O_3	“		“
“	“	“	36	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“		I/O_2			“
“	“	“	37	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“		I/O_1	“		“
“	“	“	38	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“		$_9$	“		“
“	“	“	39	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“		$_8$	“		“
“	“	“	40	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“		$_7$	“	“	“
“	I_{L01}			“	“	“	“	“	“	“	3.0 V	“	3.0 V	“				“	“	“	“		I/O_4	“		“
“	“		42	“	“	“	“	“	“	“	“	“	“		GND			“	“	“	“		I/O_3	“		“
“	“		43	“	“	“	“	“	“	“	“	“	“			GND		“	“	“	“	A	I/O_2			“
“	“		44	“	“	“	“	“	“	“	“	“	“				GND	“	“	“	“	A	I/O_1	50		“
“	I_{L02}	41	45	“	“	“	“	“	“	“	“	“	“	4.5 V				“	“	“	“	A	I/O_4	“		“
“	“		46	“	“	“	“	“	“	“	“	“	“		4.5 V			“	“	“	“		I/O_3	“		“
“	“		47	“	“	“	“	“	“	“	“	“	“			4.5 V		“	“	“	“		I/O_2	“		“
“	“		48	“	“	“	“	“	“	“	“	“	“				4.5 V	“	“	“	“		I/O_1	“		“
“	I_{CC}	3005	49	“	“	“	“	“	“	“	GND	“	GND	GND	GND	GND	GND	“	“	“	“		$_{CC}$	“	2/	mA
BIT STRESS TEST			50	3/	3/	3/	3/	3/	3/	3/	3/	“	3/	“	3/	3/	3/	3/	3/	3/	3/	CKBD and $\overline{CKBD}$	All I/O	V_{OL} “ <1.5	V_{OH} >1.5	V
7 T_C = 25°C	t_{AA}	Fig. 5,6	51	4/	4/	4/	4/	4/	4/	4/	4/	“	4/	4/	4/	4/	4/	4/	4/	4/	4.5 V	“	“	“	“	“
	“	“	52	4/	4/	4/	4/	4/	4/	4/	4/	“	4/	4/	4/	4/	4/	4/	4/	4/	5.5 V	“ V	“	“	“	“
“	“	“	53	5/	5/	5/	5/	5/	5/	5/	5/	“	5/	5/	5/	5/	5/	5/	5/	5/	4.5 V	“	“	“	“	“
“	“	“	54	5/	5/	5/	5/	5/	5/	5/	5/	“	5/	5/	5/	5/	5/	5/	5/	5/	5.5 V	“	“	“	“	“
“	“	“	55	6/	6/	6/	6/	6/	6/	6/	6/	“	6/	6/	6/	6/	6/	6/	6/	6/	4.5 V	“	“	“	“	“
“	“	“	56	6/	6/	6/	6/	6/	6/	6/	6/	“	6/	6/	6/	6/	6/	6/	6/	6/	5.5 V	“	“	“	“	“

See footnotes at end of device types 02 and 04.

TABLE III. Group A inspection for device type 02 and 04 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V; or low ≤ 0.8 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Case V	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	Algorithms 1/	Measured terminal	Test Limits		Unit
			Test no.	A_6	A_5	$_4$	$_3$	$_0$	$_1$	A_2	$\overline{\text{CS}}$	V_{SS}	$\overline{\text{WE}}$	I/O_4	I/O_3	I/O_2	I/O_1	$_9$	$_8$	$_7$	$_{CC}$			Min	Max	
7 Tc = 25°C	t_{AA}	Fig. 5, 6	57	7/	7/ A	7/ A	7/ A	7/ A	7/	7/	7/	GND	7/	7/	7/	7/	7/ A	7/ A	7/ A	7/ V	4.5 V	CKBD and $\overline{\text{CKBD}}$	All I/O	V_{OL} < 1.5	V_{OH} > 1.5	V
“	“	“	58	7/	7/	7/	7/	7/	7/	7/	7/	“	7/	7/	7/	7/	7/	7/	7/	7/	5.5 V	“	“	“	“	“
“	“	“	59	8/	8/	8/	8/	8/	8/	8/	8/	“	8/	8/	8/	8/	8/	8/	8/	8/	4.5 V	“	“	“	“	“
“	“	“	60	8/	8/	8/	8/	8/	8/	8/	8/	“	8/	8/	8/	8/	8/	8/	8/	8/	5.5 V	“	“	“	“	“
“	“	“	61	9/	9/	9/	9/	9/	9/	9/	9/	“	9/	9/	9/	9/	9/	9/	9/	9/	4.5 V	“	“	“	“	“
“	“	“	62	9/	9/	9/	9/	9/	9/	9/	9/	“	9/	9/	9/	9/	9/	9/	9/	9/	5.5 V	“	“	“	“	“
“	t_{ACS1}	“	63	10/	10/	10/	10/	10/	10/	10/	10/	“	10/	10/	10/	10/	10/	10/	10/	10/	4.5 V	“	“	“	“	“
“	t_{ACS1}	“	64	10/	10/	10/	10/	10/	10/	10/	10/	“	10/	10/	10/	10/	10/	10/	10/	10/	5.5 V	“	“	“	“	“
“	t_{ACS1}	“	65	10/	10/	10/	10/	10/	10/	10/	10/	“	10/	10/	10/	10/	10/	10/	10/	10/	4.5 V	MARCH	“	“	“	“
“	t_{ACS1}	“	66	10/	10/	10/	10/	10/	10/	10/	10/	“	10/	10/	10/	10/	10/	10/	10/	10/	5.5 V	MARCH	“	“	“	“
8	Same tests, terminal conditions, and limits as subgroup 7, except T_C = 125°C and -55°C																									
9 Tc =25°C	t_{AA}	Fig. 5, 6	67	11/	11/	11/	11/	11/	11/	11/	11/	GND	11/	11/	11/	11/	11/	11/	11/	11/	4.5 V	GALPAT and GALRESH	All I/O		12/	ns
	$_{AA}$	“	68	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	“	“		12/	
“	t_{ACS1}	“	69	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“	“		13/	“
“	t_{ACS1}	“	70	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	“	“		13/	“
“	t_{WC}	“	71	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“	“	14/		
“	t_{WC}	“	72	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	“	“	14/		
“	t_{WP}	“	73	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“	“	15/		“
“	t_{WP}	“	74	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	“	“	15/	“	“
“	t_{WR}		75	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“	“	0	“	
“	t_{WR}	“	76	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	“	“	0		
“	t_{DW}	“	77	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“	“	16/		
“	t_{DW} “	“	78	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	“	“	16/	“	

“
“
“

See footnotes at end of device types 02 and 04.

TABLE III. Group A inspection for device type 02 and 04 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V; or low ≤ 0.8 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Case V	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	Algorithms 1/	Measured terminal	Test Limits		Unit
			Test no.	A_6	A_5	$_4$	$_3$	$_0$	$_1$	A_2	$\overline{CS}$	V_{SS}	$\overline{WE}$	I/O_4	I/O_3	I/O_2	I/O_1	$_9$	$_8$	$_7$	$_{CC}$			Min	Max	
9 Tc = 25°C	t_{DH}	Fig. 5, 6	79	11/	11/A	11/A	11/A	11/A	11/	11/	11/	GND	11/	11/	11/	11/	11/A	11/A	11/A	11/V	4.5 V	GALPAT and GALRESH	All I/O	0		ns
9 Tc = 25°C	t_{DH}	Fig. 5 ,6	80	11/	11/	11/	11/	11/	11/	11/	11/	GND	11/	11/	11/	11/	11/	11/	11/	11/	4.5 V	GALPAT and GALRESH	All I/O	0		ns
10	Same tests, terminal conditions, and limits as subgroup 9, except T_C = 125°C.																									
11	Same tests, terminal conditions, and limits as subgroup 9, except T_C = -55°C.																									

_/ See appendix for description of algorithms.
_/ I_{CC} = 100 mA for device type 02; 70 mA for device type 04.
_/ V_{IL} = GND, V_{IH} = 6.0 V, pause time = 250 ms/loop max, $\overline{CS}$ = high, only performed once at 125°C, and V_{CC} = 7.0 V min.
1 _/ V_{IL} = 0.8 V and V_{IH} = 2.0 V.
2 _/ Algorithm has 60 ms where chip is deselected between the write.
_/ V_{IL} = GND, V_{IH} = 3.0 V, and all address setup times are at minimums.
3 _/ V_{IL} = GND, V_{IH} = 3.0 V and all write pulse timing are at a minimum.
4 _/ V_{IL} = GND, V_{IH} = 3.0 V and all address ending timing are at minimums.
5 _/ V_{IL} = GND, V_{IH} = 3.0 V, and t_{AA} is measured at minimum timing.
6 10/ V_{IL} = GND, V_{IH} = 2.0 V, t_{ACS1} and t_{ACS2} are measured at minimum timing.
7 11/ V_{IL} = 0.8 V, V_{IH} = 2.0 V, and all parameters are measured at minimum timing.
8 12/ t_{AA} = 450 ns for device type 02; 250 ns for device type 04.
9 13/ t_{ACS1} = 120 ns for device type 02; 85 ns for device type 04.
14/ t_{WC} = 450 ns for device type 02; 250 ns for device type 04.
15/ t_{WP} = 200 ns for device type 02; 135 ns for device type 04.
16/ t_{DW} = 200 ns for device type 02; 135 ns for device type 04.

TABLE III. Group A inspection for device type 06.

Terminal conditions (pins not designated may be high ≥ 2.0 V; or low ≤ 0.8 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Case V	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	Algorithms 1/	Measured terminal	Test Limits		Unit
			Test no.	A_6	A_5	A_4	$_3$	$_0$	$_1$	A_2	$\overline{CS}$	V_{SS}	$\overline{WE}$	I/O$_4$	I/O$_3$	I/O$_2$	I/O$_1$	$_9$	$_8$	$_7$	$_{CC}$			Min	Max	
1	V_{OH}	3006	1	GND	GND	GNDA	GNDA	GNDA	GND	GND	GND	GND	3.0 V	-4 mA			A	GNDA	GNDA	GNDV	4.5 V		I/O$_4$	2.4		V
Tc = 25°C	“	“	2	“	“	“	“	“	“	“	“	“	“		-4 mA			“	“	“	“		I/O$_3$	“		
“	“	“	3	“	“	“	“	“	“	“	“	“	“			-4 mA			“	“	“		I/O$_2$	“		
“	“	“	4	“	“	“	“	“	“	“	“	“	“				-4 mA	“	“	“	“		I/O$_1$	“		
“	V_{OL}	3007	5	“	“	“	“	“	“	“	“	“	“	8 mA				“	“	“	“		I/O$_4$		0.4	“
“	“	“	6	“	“	“	“	“	“	“	“	“	“	“	8 mA		“		“	“	“		I/O$_3$		“	“
“	“	“	7	“	“	“	“	“	“	“	“	“	“	“	“	8 mA			“	“	“		I/O$_2$		“	“
“	“	“	8	“	“	“	“	“	“	“	“	“	“	“	“	“	8 mA	“	“	“	“		I/O$_1$	“		“
“	I_{IH}	3010	9	5.5 V	“	“	“	“	“	“	“	“	“	GND	GND	GND	GND	“	“	“	5.5 V		$_6$	“	10	µA
“	“	“	10	GND	5.5 V	“	“	“	“	“	“	“	“	“	“	“	““	“	“	“	“		$_5$	“		“
“	“	“	11	“	GND	5.5 V	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“		$_4$			“
“	“	“	12	“	“	GND	5.5 V	“	“	“	“	“	“	“	“	“	“	“	“	“	“		$_3$	“		“
“	“	“	13	“	“	“	GND	5.5 V	“	“	“	“	“	“	“	“	“	“	“	“	“		$_0$	“		“
“	“	“	14	“	“	“	“	GND	5.5 V	“	“	“	“	“	“	“	“	“	“	“	“	A	$_1$	“		“
“	“	“	15	“	“	“	“	“	GND	5.5 V	“	“	“	“	“	“	“	“	“	“	“	A	$_2$	“		“
“	“	“	16	“	“	“	“	“	“	GND	5.5 V	“	“	“	“	“	“	“	“	“	“	A A	$\overline{CS}$	“ “		“
“	“	“	17	“	“	“	“	“	“	“	GND	“	5.5 V	“	“	“	“	“	“	“	“	A A	$\overline{WE}$	“		“
“	“	“	18	“	“	“	“	“	“	“	“	“	GND	5.5 V	“	“	“	“	“	“	“	A	I/O$_4$	“		“
“	“	“	19	“	“	“	“	“	“	“	“	“	“	GND	5.5 V	“	“	“	“	“	“		I/O$_3$			“
“	“	“	20	“	“	“	“	“	“	“	“	“	“	“	GND	5.5 V	“	“	“	“	“		I/O$_2$	“		“
“	“	“	21	“	“	“	“	“	“	“	“	“	“	“	“	GND	5.5 V	“	“	“	“		I/O$_1$	“		“
“	“	“	22	“	“	“	“	“	“	“	“	“	“	“	“	“	GND	5.5 V	“	“	“		$_9$	“		“
“	“	“	23	“	“	“	“	“	“	“	“	“	“	“	“	“	“	GND	5.5 V	“	“		$_8$	“		“
“	“	“	24	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	GND	5.5 V	“		$_7$	“		“
“	I_{IL}	3009	25	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	GND	“		$_6$	“		“
“	“	“	26	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“		$_5$	“		“
“	“	“	27	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	A	$_4$	“		“
“	“	“	28	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	A	$_3$	“		“
“	“	“	29	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	A	$_0$	“		“
																						A A A A A		“ “		

See footnotes at end of device types 06.

TABLE III. Group A inspection for device type 06 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V; or low ≤ 0.8 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Case V	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	Algorithms 1/	Measured terminal	Test Limits		Unit
			Test no.	A_6	A_5	4	3	0	1	A_2	$\overline{CS}$	V_{SS}	$\overline{WE}$	I/O_4	I/O_3	I/O_2	I/O_1	9	8	7	CC			Min	Max	
1 Tc = 25°C	I_{IL}	3009	30	GND	GND A	GND A	GND A	GND A	GND	GND	GND	GND	GND	GND	GND	GND	GND A	GND A	GND A	GND V	5.5 V		A_1		10	μA
“	“	“	31	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“		2		“	“
“	“	“	32	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“		$\overline{CS}$		“	“
“	“	“	33	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“		$\overline{WE}$			“
“	“	“	34	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	A	I/O_4			“
“	“	“	35	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“		I/O_3	“		“
“	“	“	36	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“		I/O_2			“
“	“	“	37	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“		I/O_1	"		“
“	“	“	38	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“		9	“		“
“	“	“	39	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“		8	“		“
“	“	“	40	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“		7	“	“	“
“	I_{L01}			“	“	“	“	“	“	“	3.0 V	“	3.0 V	“				“	“	“	“		I/O_4	“		“
“	“		42	“	“	“	“	“	“	“	“	“	“		GND			“	“	“	“		I/O_3	“		“
“	“		43	“	“	“	“	“	“	“	“	“	“			GND		“	“	“	“	A	I/O_2			“
“	“		44	“	“	“	“	“	“	“	“	“	“				GND	“	“	“	“	A	I/O_1	50		“
“	I_{L02}	41	45	“	“	“	“	“	“	“	“	“	“	4.5 V				“	“	“	“	A	I/O_4	“		“
“	“		46	“	“	“	“	“	“	“	“	“	“		4.5 V			“	“	“	“		I/O_3	“		“
“	“		47	“	“	“	“	“	“	“	“	“	“			4.5 V		“	“	“	“		I/O_2	“		“
“	“		48	“	“	“	“	“	“	“	“	“	“				4.5 V	“	“	“	“		I/O_1	“		“
“	I_{CC}	3005	49	“	“	“	“	“	“	“	GND	“	GND	GND	GND	GND	GND	“	“	“	“		CC	“	2/	mA
BIT STRESS TEST			50	3/	3/	3/	3/	3/	3/	3/	3/	“	3/	“	3/	3/	3/	3/	3/	3/	3/	CKBD and $\overline{CKBD}$	All I/O	V_{OL} “ <1“.5	V_{OH} >1.5	V
7 T_C = 25°C	t_{AA}	Fig. 5,6	51	4/	4/	4/	4/	4/	4/	4/	4/	“	4/	4/	4/	4/	4/	4/	4/	4/	4.5 V	“	“	“	“	“
	“	“	52	4/	4/	4/	4/	4/	4/	4/	4/	“	4/	4/	4/	4/	4/	4/	4/	4/	5.5 V	“ V	“	“	“	“
“	“	“	53	5/	5/	5/	5/	5/	5/	5/	5/	“	5/	5/	5/	5/	5/	5/	5/	5/	4.5 V	“	“	“	“	“
“	“	“	54	5/	5/	5/	5/	5/	5/	5/	5/	“	5/	5/	5/	5/	5/	5/	5/	5/	5.5 V	“	“	“	“	“
“	“	“	55	6/	6/	6/	6/	6/	6/	6/	6/	“	6/	6/	6/	6/	6/	6/	6/	6/	4.5 V	“	“	“	“	“
“	“	“	56	6/	6/	6/	6/	6/	6/	6/	6/	“	6/	6/	6/	6/	6/	6/	6/	6/	5.5 V	“	“	“	“	“

See footnotes at end of device types 02 and 04.

TABLE III. Group A inspection for device type 06 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V; or low ≤ 0.8 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Case V	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	Algorithms 1/	Measured terminal	Test Limits		Unit
			Test no.	A_6	A_5	$_4$	$_3$	$_0$	$_1$	A_2	$\overline{CS}$	V_{SS}	$\overline{WE}$	I/O_4	I/O_3	I/O_2	I/O_1	$_9$	$_8$	$_7$	$_{CC}$			Min	Max	
7 Tc = 25°C	t_{AA}	Fig. 5, 6	57	7/	7/ A	7/ A	7/ A	7/ A	7/	7/	7/	GND	7/	7/	7/	7/	7/ A	7/ A	7/ A	7/ V	4.5 V	CKBD and $\overline{CKBD}$	All I/O	V_{OL} < 1.5	V_{OH} > 1.5	V
“	“	“	58	7/	7/	7/	7/	7/	7/	7/	7/	“	7/	7/	7/	7/	7/	7/	7/	7/	5.5 V	“	“	“	“	“
“	“	“	59	8/	8/	8/	8/	8/	8/	8/	8/	“	8/	8/	8/	8/	8/	8/	8/	8/	4.5 V	“	“	“	“	“
“	“	“	60	8/	8/	8/	8/	8/	8/	8/	8/	“	8/	8/	8/	8/	8/	8/	8/	8/	5.5 V	“	“	“	“	“
“	“	“	61	9/	9/	9/	9/	9/	9/	9/	9/	“	9/	9/	9/	9/	9/	9/	9/	9/	4.5 V	“	“	“	“	“
“	“	“	62	9/	9/	9/	9/	9/	9/	9/	9/	“	9/	9/	9/	9/	9/	9/	9/	9/	5.5 V	“	“	“	“	“
“	t_{ACS1}	“	63	10/	10/	10/	10/	10/	10/	10/	10/	“	10/	10/	10/	10/	10/	10/	10/	10/	5.5 V	“	“	“	“	“
“	t_{ACS2}	“	64	10/	10/	10/	10/	10/	10/	10/	10/	“	10/	10/	10/	10/	10/	10/	10/	10/	5.5 V	“	“	“	“	“
“	t_{ACS1}	“	65	10/	10/	10/	10/	10/	10/	10/	10/	“	10/	10/	10/	10/	10/	10/	10/	10/	4.5 V	MARCH	“	“	“	“
“	t_{ACS2}	“	66	10/	10/	10/	10/	10/	10/	10/	10/	“	10/	10/	10/	10/	10/	10/	10/	10/	4.5 V	MARCH	“	“	“	“
8	Same tests, terminal conditions, and limits as subgroup 7, except T_C = 125°C and -55°C																									
9 Tc =25°C	t_{AA}	Fig. 5, 6	67	11/	11/	11/	11/	11/	11/	11/	11/	GND	11/	11/	11/	11/	11/	11/	11/	11/	4.5 V	GALPAT and GALRESH	All I/O		70	ns
	$_{AA}$	“	68	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	“	“		70	
“	t_{ACS1}	“	69	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“	“		70	“
“	t_{ACS1}	“	70	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	“	“		70	“
“	$t_{ ACS2}$	“	71	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“	“		80	“
“t	$t_{ ACS2}$	“	72	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	“	“		80	“
“	t_{WC}	“	73	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“	“	70		“
“	t_{WC}	“	74	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	“	“	70		“
“	t_{WP}		75	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“	“	50		
“	t_{WP}	“	76	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	“	“	50		
“	t_{WR}	“	77	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“	“	5		
“	t_{WR} “	“	78	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	“	“	5	“	

“
“
“

See footnotes at end of device types 06.

TABLE III. Group A inspection for device type 06 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.0 V; or low ≤ 0.8 V; or open).

Subgroup	Symbol	MIL-STD-883 method	Case V	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	Algorithms 1/	Measured terminal	Test Limits		Unit
			Test no.	A_6	A_5	4	3	0	1	A_2	$\overline{CS}$	V_{SS}	$\overline{WE}$	I/O_4	I/O_3	I/O_2	I/O_1	9	8	7	CC			Min	Max	
9 Tc = 25°C	t_{DW}	Fig. 5, 6	79	11/	11/A	11/A	11/A	11/A	11/	11/	11/	GND	11/	11/	11/	11/	11/A	11/A	11/A	11/V	4.5 V	GALPAT and GALRESH	All I/O	25		ns
“	t_{DW}	“	80	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	“	“	25		“
“	t_{DH}	“	81	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“	“	0		“
“	t_{DH}	“	82	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“	“	0		“
10	Same tests, terminal conditions, and limits as subgroup 9, except T_C = 125°C.																									
11	Same tests, terminal conditions, and limits as subgroup 9, except T_C = -55°C.																									

_/ See appendix for description of algorithms.
_/ I_{CC} = 180 mA .
_/ V_{IL} = GND, V_{IH} = 6.0 V,cycle time = 250 ms/loop max, $\overline{CS}$ = high, only performed once at 125°C, and V_{CC} = 7.0 V min.
1 _/ V_{IL} = 0.8 V and V_{IH} = 2.0 V.
2 _/ Algorithm has 60 ms where chip is deselected between the write.
_/ V_{IL} = GND, V_{IH} = 3.0 V, and all address setup times are at minimums.
3 _/ V_{IL} = GND, V_{IH} = 3.0 V and all write pulse timing are at a minimum.
4 _/ V_{IL} = GND, V_{IH} = 3.0 V and all address ending timing are at minimums.
5 _/ V_{IL} = GND, V_{IH} = 3.0 V, and t_{AA} is measured at minimum timing.
6 10/ V_{IL} = GND, V_{IH} = 3.0 V, t_{ACS1} and t_{ACS2} are measured at minimum timing.
7 11/ V_{IL} = 0.8 V, V_{IH} = 2.0 V, and all parameters are measured at minimum timing.
8
9

5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the military service's system command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature which may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of the specification.

b. Complete part number (see 1.2).

c. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

d. Requirements for certificate of compliance, if applicable.

e. Requirements for notification of change of product or process to contracting activity in addition to notification to the qualifying activity, if applicable.

f. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.

g. Requirements for product assurance options.

h. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

j. Requirements for packaging (see 5.1.)

6.3 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

6.4 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43123-1199.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

V_{CC}	Supply voltage
V_{SS}	Common or reference voltage node
CS	Chip-selection, input
D_{IN}	Data input
D_{OUT}	Data output
A_0 thru A_{11}	Address input
WE	Read or write input
I_{OHZ}	High-impedance-state high output current
I_{OLZ}	High-impedance-state low output current
I_{CC}	Supply current from V_{CC} supply
t_{RC}	Read cycle time
t_{AS}	Address set-up time
t_{WP}	Write pulse width
t_{WR}	Write recovery time
t_{DW}	Data valid to end of write
t_{DH}	Data hold time
t_{OH}	Output hold time from address change
t_{AA}	Address access time
t_{ACS}	Chip selection to output valid
t_{WC}	Write cycle time
t_{CW}	Chip selection to end of write
t_{AW}	Address valid to end of write
t_{LZ}	Chip selection to output in low impedance
t_{HZ}	Chip deselection to output in high impedance
t_{PU}	Chip selection to power up time
t_{PD}	Chip deselection to power down time
t_{WZ}	Write enabled to output in high impedance
t_{OW}	Output active from end of write
T_{LO}	Output leakage current
T_C	Case temperature
T_A	Ambient temperature

6.6 Logistic support. Lead materials and finishes (see 3.4) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish A (see 3.4). Longer length leads and lead forming should not affect the part number.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

Military device type	Generic-industry type
01	2147, 9147-85
02	2114, 9114B
03	2147H, 9147-70
04	2114A, 9114D
05	2147H-3, 9147-55
06	2148H, 9148-70
07	2147H-2, 9147-45

6.8 Change from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

APPENDIX A

FUNCTIONAL ALGORITHMS

Functional algorithms are test patterns which define the exact sequence of tests used to verify proper operation of a random access memory (RAM). Each algorithm serves a specified purpose for the testing of the device.

A.1 FUNCTIONAL PATTERNS.

A.1.1 Pattern 1.

CKBD.

a. Write a checkerboard pattern into memory (O in address O) from address O to N**.**

b. When the $\overline{CS}$ off test is performed, attempt to write the complement pattern into cell memory with the device not selected.

c. Read checkerboard pattern in the memory**.**

A.1.2 Pattern 2.

CKBD. Same as CKBD only with data complemented.

A.1.3 Pattern 3.

MARCH.

a. Write test word into every location.

b. The addressing is then scanned from location “O” to location “N”.

c. At each address, the test word is read and a complemented test word is written back into the same location.

d. The addressing is then scanned in reverse from location “N” to location “O”.

e. At each address, the complemented test word is read and the test word is written back in.

A.1.4 Pattern 4.

GALPAT. This program will test all bits in the array. The addressing and interaction between bits for ac performance. The memory is initialized by writing a field of “1” and then a field of “0” into the cell memory.

a. Write a “1” in word location 0 (reference location).

b. Word 0 is read.

c. Word 1 is read.

d. Word 0 is read.

e. Word 2 is read.

f. Word 0 is read.

g. The reading procedure continues back and forth between word 0 and the next higher number word until word 4095(-1) or 1023(-2) is reached. Then increment to the next word which becomes the reference location and then step a through g again until all the words in the memory are used at least once as a reference.

A.1.5 Pattern 5.

Diagonal GALRESH (with row column ping pong read GG II). This pattern will test all bits in the array for writing interaction for switching performance.

a. Initialize the memory by writing a field of 0's.

b. Perform the following read write sequence moving the test bit along the diagonal of the memory; and reading only the row and column of the test bit in ping ping fashion:

R0 = Read "0" WI = Write "1" etc.

	STEP								
	1	2	3	4	5	6	7	8	9
BACKROUND BIT		RO		RO		RO		RO	
TEST BIT	R0		WI		RI		WO		RO

c. Reinitialize the memory by writing a field of l's.

d. Perform the following read write sequence moving the test bit along the diagonal of the memory; and reading only the row and column of the test bit in ping pong fashion:

	STEP								
	1	2	3	4	5	6	7	8	9
BACKROUND BIT		RI		RI		RI		RI	
TEST BIT	RI		WO		RO		WI		RI

Custodians:
  Army - CR
  Navy - EC
  Air Force - 11
  DLA - CC

Review activities:
  Army – SM, MI
  Navy - AS, CG, MC, SH TD
  Air Force – 03, 19, 99

Preparing activity:
  DLA - CC

(Project 5962-2012)