**CY7C1041G Automotive**

# 4-Mbit (256K words × 16-bit) Static RAM with Error-Correcting Code (ECC)

## Features

- AEC-Q100 qualified
- High speed
  - $t_{AA}$ = 10 ns
- Temperature range
  - Automotive-E: –40 °C to 125 °C
  - Automotive-A: –40 °C to 85 °C
- Embedded ECC for single-bit error correction[1, 2]
- Low active and standby currents
  - Active current $I_{CC}$ = 40 mA typical
  - Standby current $I_{SB2}$ = 6 mA typical
- Operating voltage range: 2.2 V to 3.6 V
- 1.0 V data retention
- TTL- compatible inputs and outputs
- Pb-free 48-ball VFBGA and 44-pin TSOP II packages

## Functional Description

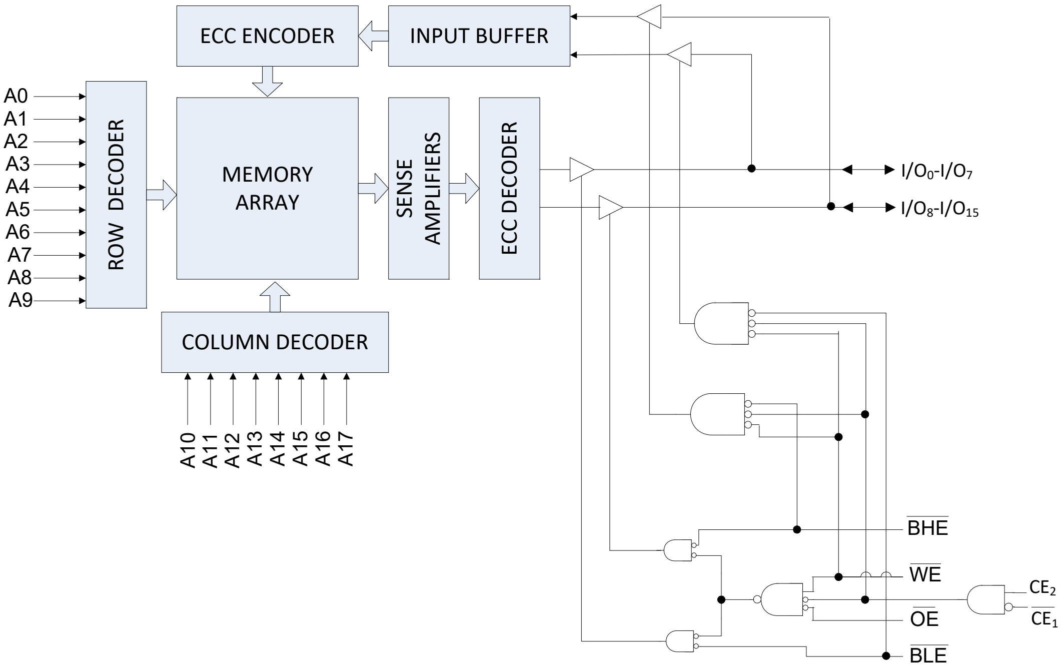
CY7C1041G is a high-performance CMOS fast static RAM automotive part with embedded ECC. This device has a single Chip Enable ($\overline{CE}$) input and is accessed by asserting it LOW.

Data writes are performed by asserting the Write Enable ($\overline{WE}$) input LOW, while providing the data on $I/O_0$ through $I/O_{15}$ and the address on $A_0$ through $A_{17}$ pins. The Byte High Enable ($\overline{BHE}$) and Byte Low Enable ($\overline{BLE}$) inputs control write operations to the upper and lower bytes of the specified memory location. $\overline{BHE}$ controls $I/O_8$ through $I/O_{15}$ and $\overline{BLE}$ controls $I/O_0$ through $I/O_7$.

Data reads are performed by asserting the Output Enable ($\overline{OE}$) input and providing the required address on the address lines. Read data is accessible on the I/O lines ($I/O_0$ through $I/O_{15}$). Byte accesses can be performed by asserting the required byte enable signal ($\overline{BHE}$ or $\overline{BLE}$) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os ($I/O_0$ through $I/O_{15}$) are placed in a HI-Z state when the device is deselected ($\overline{CE}$ LOW), or when the control signals are deasserted ($\overline{OE}$, $\overline{BLE}$, $\overline{BHE}$). Refer to the following logic block diagram.

## Logic Block Diagram – CY7C1041G



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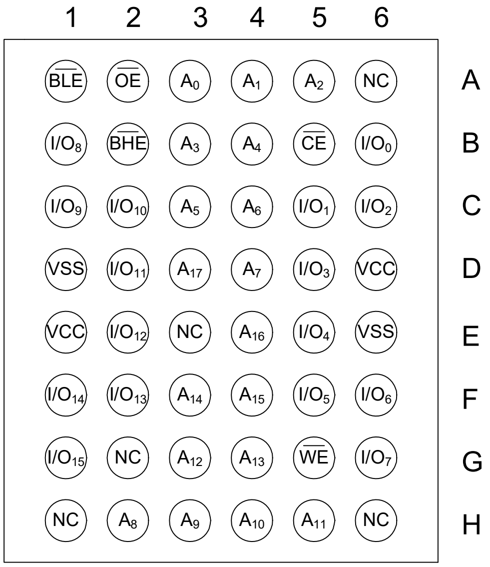
**Note**

1. This device does not support automatic write-back on error detection.
2. SER FIT Rate <0.1 FIT/Mb. Refer AN88889 for details.

## Contents

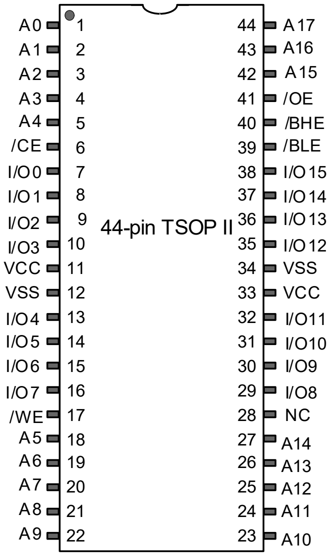
## Pin Configurations

**Figure 1. 48-ball VFBGA Pinout [3]**



| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| A | $\overline{BLE}$ | $\overline{OE}$ | $A_0$ | $A_1$ | $A_2$ | NC |
| B | $I/O_8$ | $\overline{BHE}$ | $A_3$ | $A_4$ | $\overline{CE}$ | $I/O_0$ |
| C | $I/O_9$ | $I/O_{10}$ | $A_5$ | $A_6$ | $I/O_1$ | $I/O_2$ |
| D | VSS | $I/O_{11}$ | $A_{17}$ | $A_7$ | $I/O_3$ | VCC |
| E | VCC | $I/O_{12}$ | NC | $A_{16}$ | $I/O_4$ | VSS |
| F | $I/O_{14}$ | $I/O_{13}$ | $A_{14}$ | $A_{15}$ | $I/O_5$ | $I/O_6$ |
| G | $I/O_{15}$ | NC | $A_{12}$ | $A_{13}$ | $\overline{WE}$ | $I/O_7$ |
| H | NC | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ | NC |

**Figure 2. 44-pin TSOP II Pinout [3]**



| | | | |
|---|---|---|---|
| A0 | 1 | 44 | A17 |
| A1 | 2 | 43 | A16 |
| A2 | 3 | 42 | A15 |
| A3 | 4 | 41 | /OE |
| A4 | 5 | 40 | /BHE |
| /CE | 6 | 39 | /BLE |
| I/O0 | 7 | 38 | I/O15 |
| I/O1 | 8 | 37 | I/O14 |
| I/O2 | 9 | 36 | I/O13 |
| I/O3 | 10 | 35 | I/O12 |
| VCC | 11 | 34 | VSS |
| VSS | 12 | 33 | VCC |
| I/O4 | 13 | 32 | I/O11 |
| I/O5 | 14 | 31 | I/O10 |
| I/O6 | 15 | 30 | I/O9 |
| I/O7 | 16 | 29 | I/O8 |
| /WE | 17 | 28 | NC |
| A5 | 18 | 27 | A14 |
| A6 | 19 | 26 | A13 |
| A7 | 20 | 25 | A12 |
| A8 | 21 | 24 | A11 |
| A9 | 22 | 23 | A10 |

## Product Portfolio

| Product | Range | $V_{CC}$ Range (V) | Speed (ns) | Power Dissipation | | | |
|---|---|---|---|---|---|---|---|
| | | | | Operating $I_{CC}$, (mA), f = $f_{max}$ | | Standby, $I_{SB2}$ (mA) | |
| | | | | Typ[4] | Max | Typ[4] | Max |
| CY7C1041G | Automotive-E | 2.2 V–3.6 V | 10 | 40 | 50 | 6 | 14 |
| | Automotive-A | | | 38 | 45 | 6 | 8 |

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**Notes**

[3] NC pins are not connected internally to the die.

[4] Typical values are included for reference only and are not guaranteed or tested.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ................................ –65 °C to +150 °C

Ambient temperature
with power applied .................................. –55 °C to +125 °C

Supply voltage
on $V_{CC}$ relative to GND[5] .....................–0.5 V to Vcc +0.3 V

DC voltage applied to outputs
in HI-Z State[5] ......................................–0.3 V to Vcc +0.3 V

DC input voltage[5] ..............................–0.3 V to $V_{CC}$ + 0.3 V

Current into outputs (in low state) ............................... 20 mA

Static discharge voltage
(MIL-STD-883, Method 3015) ................................. > 2001 V

Latch-up current .................................................... > 140 mA

## Operating Range

| Grade | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Automotive-E | –40 °C to +125 °C | 2.2 V to 3.6 V |
| Automotive-A | –40 °C to +85 °C | 2.2 V to 3.6 V |

## DC Electrical Characteristics

Over the Operating Range

| Parameter | Description | | Test Conditions | 10 ns (Automotive-E) | | | 10 ns (Automotive-A) | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{OH}$ | Output HIGH voltage | 2.2 V to 2.7 V | $V_{CC}$ = Min, $I_{OH}$ = –1.0 mA | 2 | – | – | 2 | – | – | V |
| | | 2.7 V to 3.0 V | $V_{CC}$ = Min, $I_{OH}$ = –4.0 mA | 2.2 | – | – | 2.2 | – | – | |
| | | 3.0 V to 3.6 V | $V_{CC}$ = Min, $I_{OH}$ = –4.0 mA | 2.4 | – | – | 2.4 | – | – | |
| $V_{OL}$ | Output LOW voltage | 2.2 V to 2.7 V | $V_{CC}$ = Min, $I_{OL}$ = 2 mA | – | – | 0.4 | – | – | 0.4 | V |
| | | 2.7 V to 3.6 V | $V_{CC}$ = Min, $I_{OL}$ = 8 mA | – | – | 0.4 | – | – | 0.4 | |
| $V_{IH}$ | Input HIGH voltage | 2.2 V to 2.7 V | – | 2 | – | $V_{CC}$ + 0.3[5] | 2 | – | $V_{CC}$ + 0.3[5] | V |
| | | 2.7 V to 3.6 V | – | 2 | – | $V_{CC}$ + 0.3[5] | 2 | – | $V_{CC}$ + 0.3[5] | |
| $V_{IL}$ | Input LOW voltage | 2.2 V to 2.7 V | – | –0.3[5] | – | 0.6 | –0.3[5] | – | 0.6 | V |
| | | 2.7 V to 3.6 V | – | –0.3[5] | – | 0.8 | –0.3[5] | – | 0.8 | |
| $I_{IX}$ | Input leakage current | | GND $\leq V_{IN} \leq V_{CC}$ | –5 | – | +5 | –1 | – | +1 | µA |
| $I_{OZ}$ | Output leakage current | | GND $\leq V_{OUT} \leq V_{CC}$, Output disabled | –5 | – | +5 | –1 | – | +1 | µA |
| $I_{CC}$ | Operating supply current | | $V_{CC}$ = 3.6 V, $I_{OUT}$ = 0 mA, CMOS levels<br>f = $f_{MAX}$ = 1/$t_{RC}$ | – | 40 | 50 | – | 38 | 45 | mA |
| $I_{SB1}$ | Automatic CE power down current – TTL inputs | | $V_{CC}$ = 3.6 V, $\overline{CE} \geq V_{IH}$,<br>$V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$,<br>f = $f_{MAX}$ | – | – | 24 | – | – | 15 | mA |
| $I_{SB2}$ | Automatic CE power down current – CMOS inputs | | $V_{CC}$ = 3.6 V,<br>$\overline{CE} \geq V_{CC}$ – 0.2 V,<br>$V_{IN} \geq V_{CC}$ – 0.2 V or $V_{IN} \leq$ 0.2 V,<br>f = 0 | – | 6 | 14 | – | 6 | 8 | mA |

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**Note**

5. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = $V_{CC}$ + 2 V for pulse durations of less than 20 ns.

## Capacitance

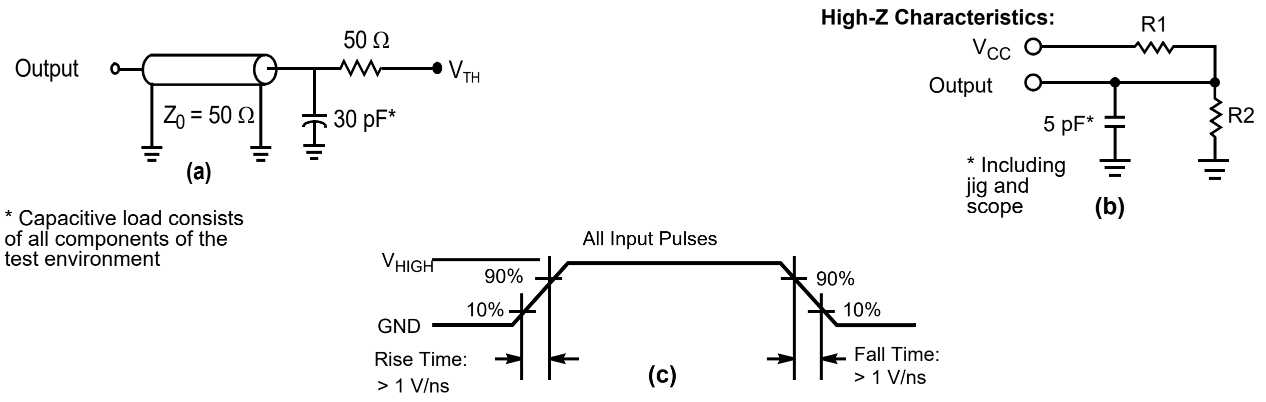
| Parameter[6] | Description | Test Conditions | All Packages | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $T_A = 25$ °C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$ | 10 | pF |
| $C_{OUT}$ | I/O capacitance | | 10 | pF |

## Thermal Resistance

| Parameter[6] | Description | Test Conditions | 48-ball VFBGA | 44-pin TSOPII | Unit |
|---|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance (junction to ambient) | Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board | 30.68 | 66.82 | °C/W |
| $\Theta_{JC}$ | Thermal resistance (junction to case) | | 14.83 | 15.97 | °C/W |

## AC Test Loads and Waveforms

**Figure 3. AC Test Loads and Waveforms** [7]



| Parameters | 3.0 V | Unit |
|---|---|---|
| R1 | 317 | Ω |
| R2 | 351 | Ω |
| $V_{TH}$ | 1.5 | V |
| $V_{HIGH}$ | 3 | V |

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**Notes**

6. Tested initially and after any design or process change that may affect these parameters.
7. Full-device AC operation assumes a 100 µs ramp time from 0 to $V_{CC(min)}$ and a 100 µs wait time after $V_{CC}$ stabilization.

## Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | Automotive-E | | Automotive-A | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $V_{DR}$ | $V_{CC}$ for data retention | – | 1 | – | 1 | – | V |
| $I_{CCDR}$ | Data retention current | $V_{CC}$ = 1.2 V,<br>$\overline{CE} \geq V_{CC} - 0.2$ V,<br>$V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V | – | 14 | – | 8 | mA |
| $t_{CDR}$[8] | Chip deselect to data retention time | – | 0 | – | 0 | – | ns |
| $t_R$[8, 9] | Operation recovery time | $V_{CC} \geq 2.2$ V | 10 | – | 10 | – | ns |

## Data Retention Waveform

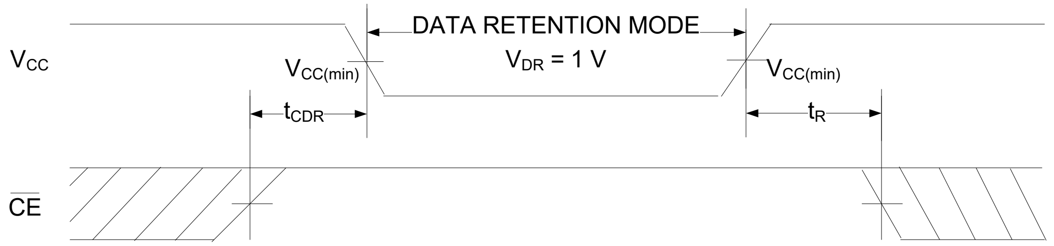

**Figure 4. Data Retention Waveform** [9]

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**Notes**

8. These parameters are guaranteed by design.
9. Full-device operation requires linear $V_{CC}$ ramp from $V_{DR}$ to $V_{CC(min.)} \geq 100$ µs or stable at $V_{CC(min.)} \geq 100$ µs.

## AC Switching Characteristics

Over the Operating Range

| Parameter[10] | Description | 10 ns (Automotive-A/Automotive-E) Min | Max | Unit |
|---|---|---|---|---|
| **Read Cycle** | | | | |
| $t_{RC}$ | Read cycle time | 10 | – | ns |
| $t_{AA}$ | Address to data | – | 10 | ns |
| $t_{OHA}$ | Data | 3 | – | ns |
| $t_{ACE}$ | $\overline{\text{CE}}$ LOW to data[11] | – | 10 | ns |
| $t_{DOE}$ | $\overline{\text{OE}}$ LOW to data | – | 4.5 | ns |
| $t_{LZOE}$ | $\overline{\text{OE}}$ LOW to low impedance[12, 13] | 0 | – | ns |
| $t_{HZOE}$ | $\overline{\text{OE}}$ HIGH to HI-Z[12, 13] | – | 5 | ns |
| $t_{LZCE}$ | $\overline{\text{CE}}$ LOW to low impedance[11, 12, 13] | 3 | – | ns |
| $t_{HZCE}$ | $\overline{\text{CE}}$ HIGH to HI-Z[11, 12, 13] | – | 5 | ns |
| $t_{PU}$ | $\overline{\text{CE}}$ LOW to power up[11, 13] | 0 | – | ns |
| $t_{PD}$ | $\overline{\text{CE}}$ HIGH to power down[11, 13] | – | 10 | ns |
| $t_{DBE}$ | Byte enable to data valid | – | 4.5 | ns |
| $t_{LZBE}$ | Byte enable to low impedance[13] | 0 | – | ns |
| $t_{HZBE}$ | Byte disable to HI-Z[13] | – | 6 | ns |
| **Write Cycle**[14, 15] | | | | |
| $t_{WC}$ | Write cycle time | 10 | – | ns |
| $t_{SCE}$ | $\overline{\text{CE}}$ LOW to write end[10] | 7 | – | ns |
| $t_{AW}$ | Address setup to write end | 7 | – | ns |
| $t_{HA}$ | Address hold from write end | 0 | – | ns |
| $t_{SA}$ | Address setup to write start | 0 | – | ns |
| $t_{PWE}$ | $\overline{\text{WE}}$ pulse width | 7 | – | ns |
| $t_{SD}$ | Data setup to write end | 5 | – | ns |
| $t_{HD}$ | Data hold from write end | 0 | – | ns |
| $t_{LZWE}$ | $\overline{\text{WE}}$ HIGH to low impedance[12, 13] | 3 | – | ns |
| $t_{HZWE}$ | $\overline{\text{WE}}$ LOW to HI-Z[12, 13] | – | 5 | ns |
| $t_{BW}$ | Byte Enable to write end | 7 | – | ns |

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**Notes**

10. Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to $V_{CC}$ (for $V_{CC} < 3$ V). Test conditions for the read cycle use output loading shown in part (a) of Figure 3 on page 5, unless specified otherwise.
11. For all dual chip enable devices, $\overline{\text{CE}}$ is the logical combination of $\overline{\text{CE}}_1$ and $CE_2$. When $\overline{\text{CE}}_1$ is LOW and $CE_2$ is HIGH, $\overline{\text{CE}}$ is LOW; when $\overline{\text{CE}}_1$ is HIGH or $CE_2$ is LOW, $\overline{\text{CE}}$ is HIGH.
12. $t_{HZOE}$, $t_{HZCE}$, $t_{HZWE}$, $t_{HZBE}$, $t_{LZOE}$, $t_{LZCE}$, $t_{LZWE}$, and $t_{LZBE}$ are specified with a load capacitance of 5 pF as in (b) of Figure 3 on page 5. Transition is measured ±200 mV from steady state voltage.
13. These parameters are guaranteed by design and are not tested.
14. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{IL}$, $\overline{\text{CE}} = V_{IL}$ and $\overline{\text{BHE}}$ or $\overline{\text{BLE}} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
15. The minimum write cycle pulse width for Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) should be equal to sum of $t_{SD}$ and $t_{HZWE}$.

## Switching Waveforms

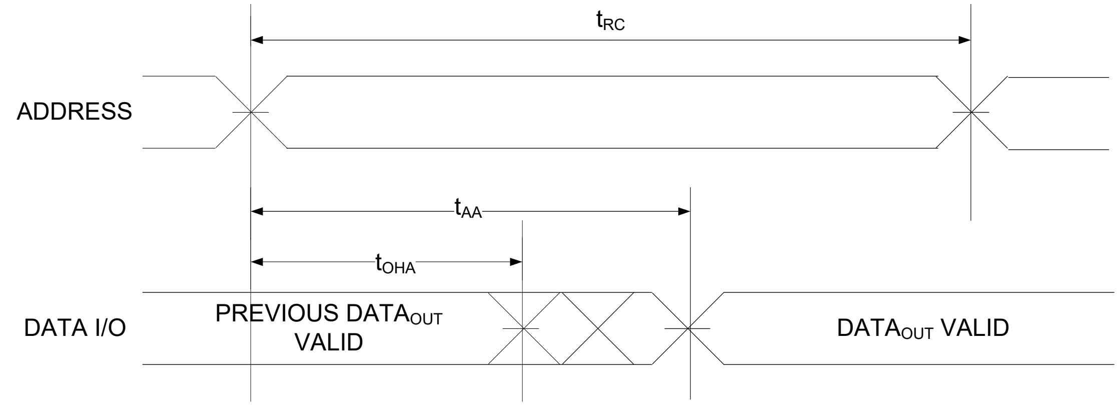

**Figure 5. Read Cycle No. 1 of CY7C1041G (Address Transition Controlled)** [16, 17]

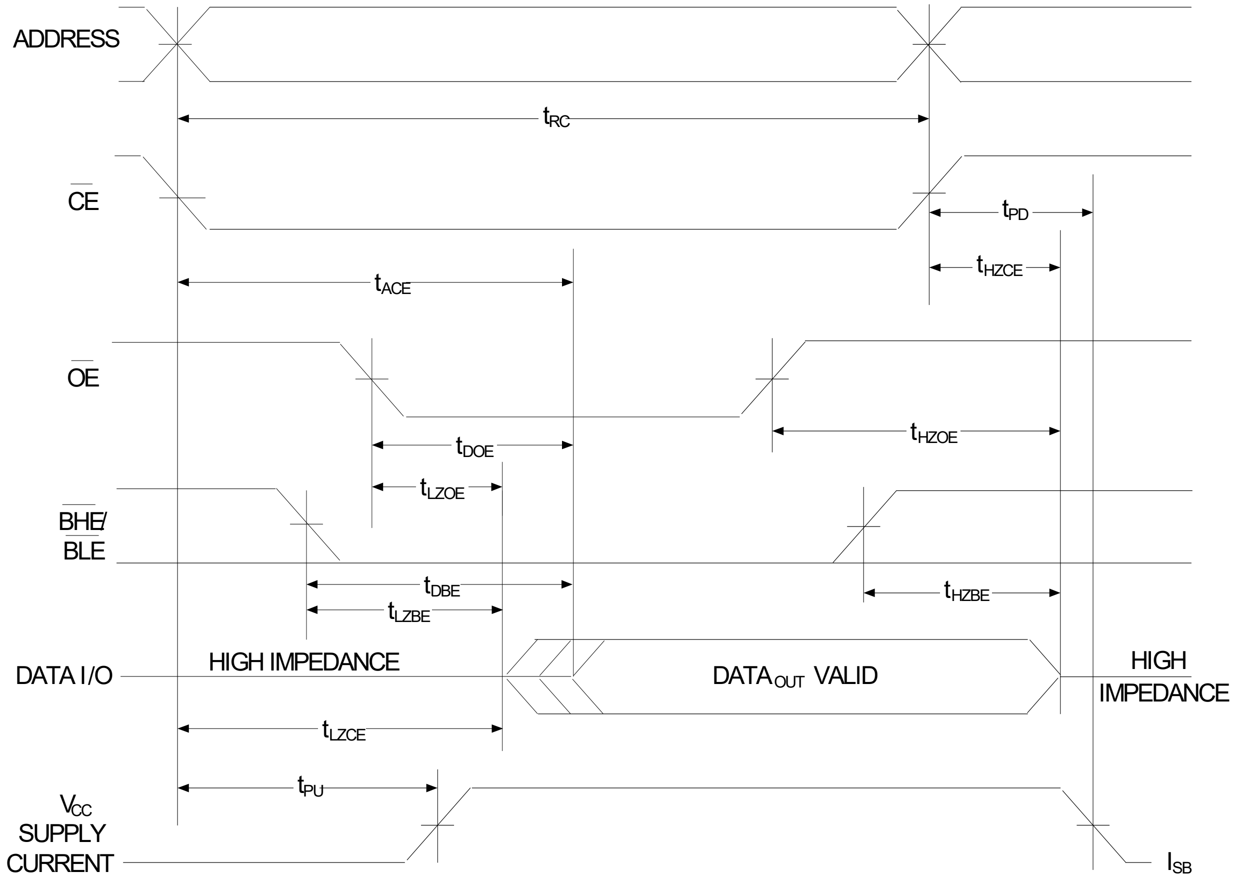

**Figure 6. Read Cycle No. 2 ($\overline{OE}$ Controlled)** [17]

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**Notes**

[16] The device is continuously selected, $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both = $V_{IL}$.

[17] $\overline{WE}$ is HIGH for read cycle.

## Switching Waveforms (continued)

**Figure 7. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled)** [18, 19, 20]

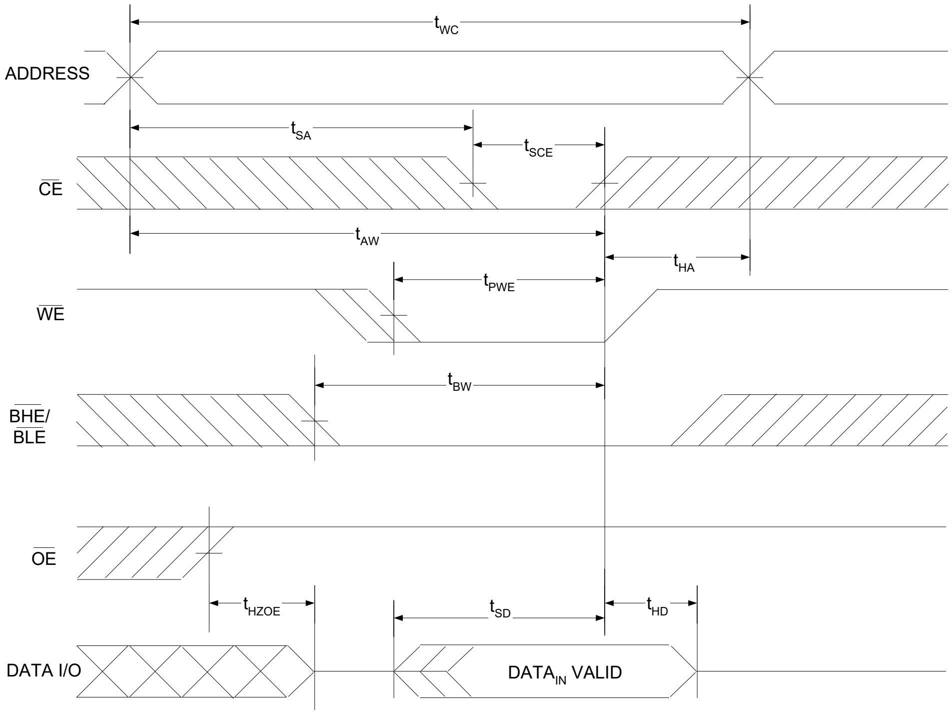
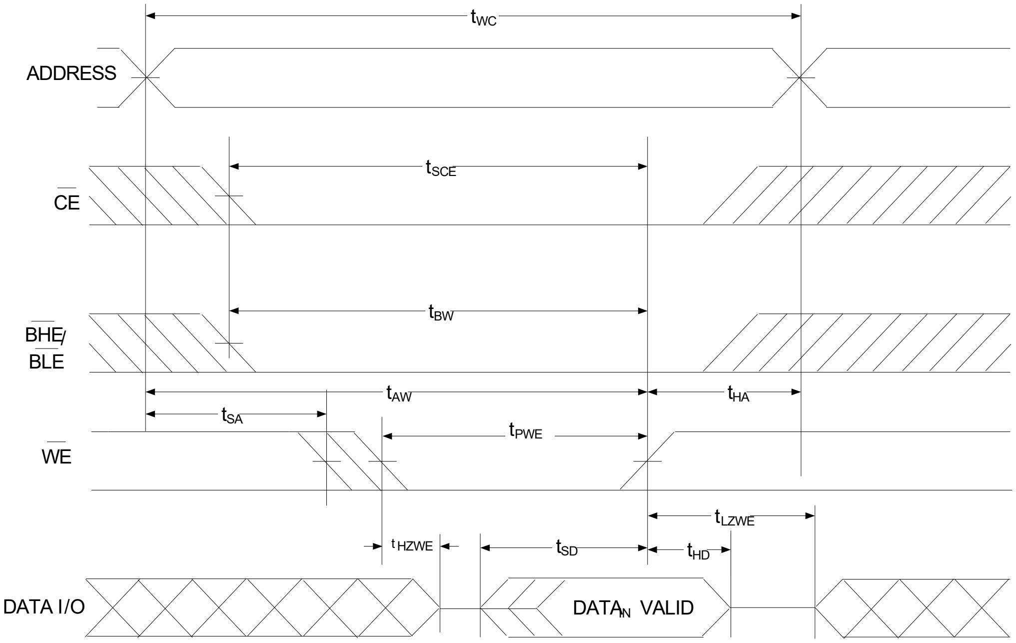


**Figure 8. Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)** [18, 19, 20, 21]



**Notes**

18. Address valid prior to or coincident with $\overline{\text{CE}}$ LOW transition.
19. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{IL}$, $\overline{\text{CE}} = V_{IL}$ and $\overline{\text{BHE}}$ or $\overline{\text{BLE}} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
20. Data I/O is in HI-Z state if $\overline{\text{CE}} = V_{IH}$, or $\overline{\text{OE}} = V_{IH}$ or $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}} = V_{IH}$.
21. The minimum write cycle pulse width should be equal to sum of $t_{SD}$ and $t_{HZWE}$.

## Switching Waveforms (continued)

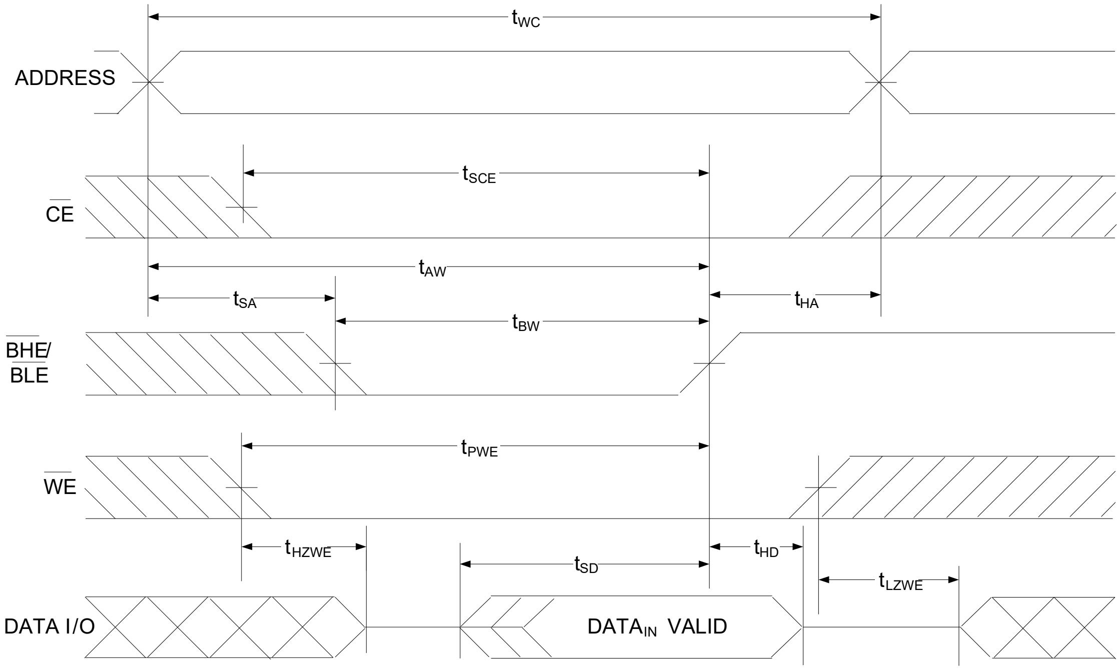


Figure 9. Write Cycle No. 3 (BLE or BHE Controlled) [22, 23]

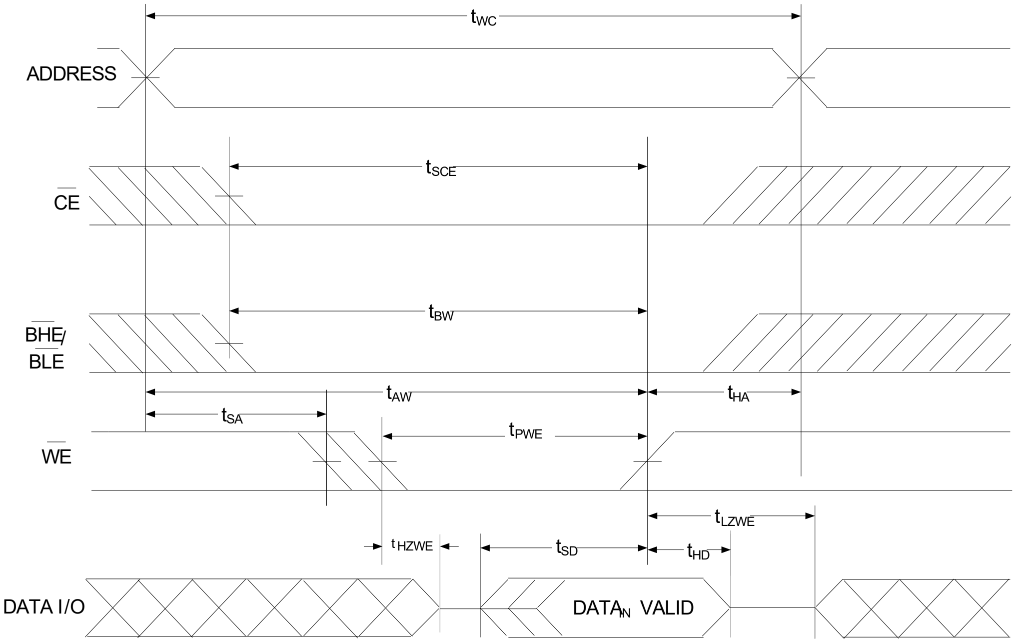


Figure 10. Write Cycle No. 4 (WE Controlled) [22, 23, 24]

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**Notes**

22. The internal write time of the memory is defined by the overlap of WE = $V_{IL}$, CE = $V_{IL}$ and BHE or BLE = $V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
23. Data I/O is in HI-Z state if CE = $V_{IH}$, or OE = $V_{IH}$ or BHE, and/or BLE = $V_{IH}$.
24. Data I/O is high impedance if OE = $V_{IH}$.
25. During this period the I/Os are in output state. Do not apply input signals.

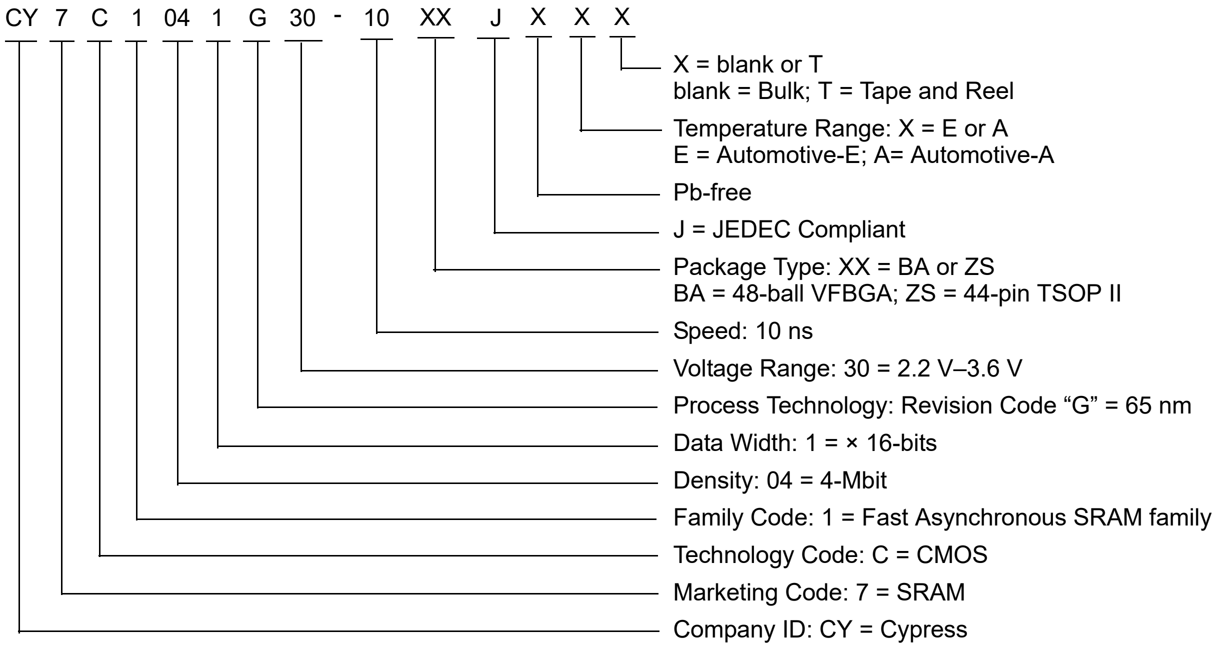
## Truth Table

| $\overline{\text{CE}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | $\overline{\text{BLE}}$ | $\overline{\text{BHE}}$ | $I/O_0$–$I/O_7$ | $I/O_8$–$I/O_{15}$ | Mode | Power |
|---|---|---|---|---|---|---|---|---|
| H | X | X | X | X | HI-Z | HI-Z | Power down | Standby ($I_{SB}$) |
| L | L | H | L | L | Data out | Data out | Read all bits | Active ($I_{CC}$) |
| L | L | H | L | H | Data out | HI-Z | Read lower bits only | Active ($I_{CC}$) |
| L | L | H | H | L | HI-Z | Data out | Read upper bits only | Active ($I_{CC}$) |
| L | X | L | L | L | Data in | Data in | Write all bits | Active ($I_{CC}$) |
| L | X | L | L | H | Data in | HI-Z | Write lower bits only | Active ($I_{CC}$) |
| L | X | L | H | L | HI-Z | Data in | Write upper bits only | Active ($I_{CC}$) |
| L | H | H | X | X | HI-Z | HI-Z | Selected, outputs disabled | Active ($I_{CC}$) |

## Ordering Information

| Speed (ns) | Voltage Range | Ordering Code | Package Diagram | Package Type (all Pb-free) | Operating Range |
|---|---|---|---|---|---|
| 10 | 2.2 V–3.6 V | CY7C1041G30-10BAJXE | 001-85259 | 48-ball VFBGA | Automotive-E |
| | | CY7C1041G30-10BAJXET | 001-85259 | 48-ball VFBGA, Tape and Reel | |
| | | CY7C1041G30-10ZSXE | 51-85087 | 44-pin TSOP II | |
| | | CY7C1041G30-10ZSXET | 51-85087 | 44-pin TSOP II, Tape and Reel | |
| | | CY7C1041G30-10ZSXA | 51-85087 | 44-pin TSOP II | Automotive-A |
| | | CY7C1041G30-10ZSXAT | 51-85087 | 44-pin TSOP II, Tape and Reel | |

### Ordering Code Definitions

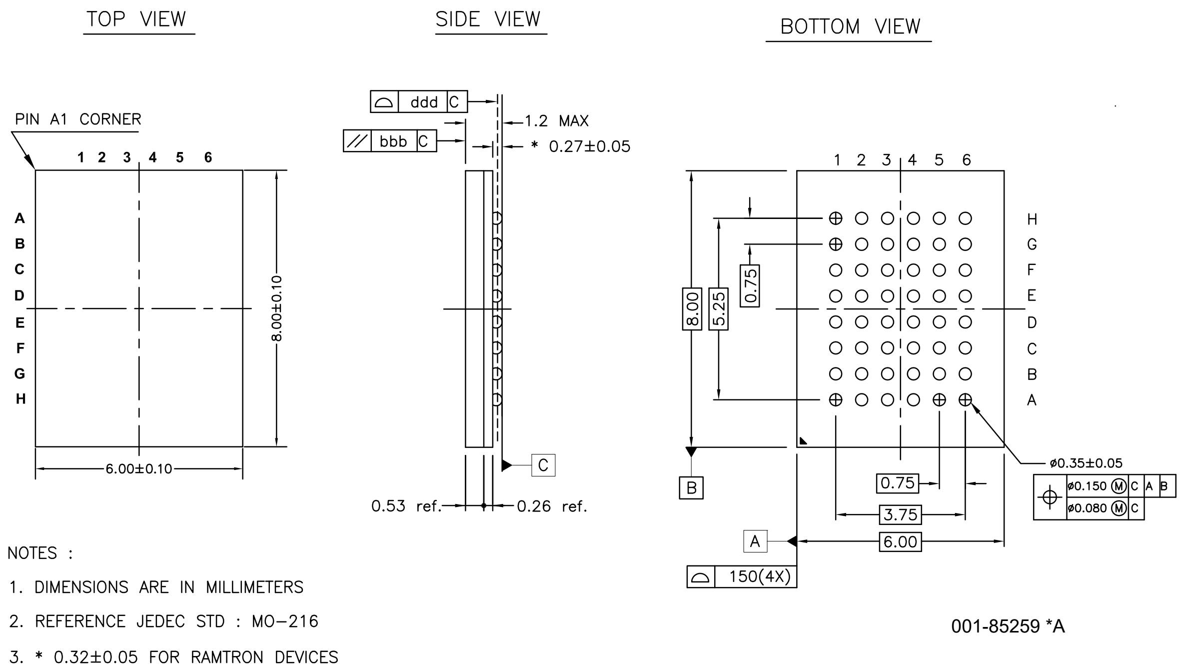


CY 7 C 1 04 1 G 30 - 10 XX J X X X

X = blank or T
blank = Bulk; T = Tape and Reel
Temperature Range: X = E or A
E = Automotive-E; A= Automotive-A
Pb-free
J = JEDEC Compliant
Package Type: XX = BA or ZS
BA = 48-ball VFBGA; ZS = 44-pin TSOP II
Speed: 10 ns
Voltage Range: 30 = 2.2 V–3.6 V
Process Technology: Revision Code “G” = 65 nm
Data Width: 1 = × 16-bits
Density: 04 = 4-Mbit
Family Code: 1 = Fast Asynchronous SRAM family
Technology Code: C = CMOS
Marketing Code: 7 = SRAM
Company ID: CY = Cypress

## Package Diagrams

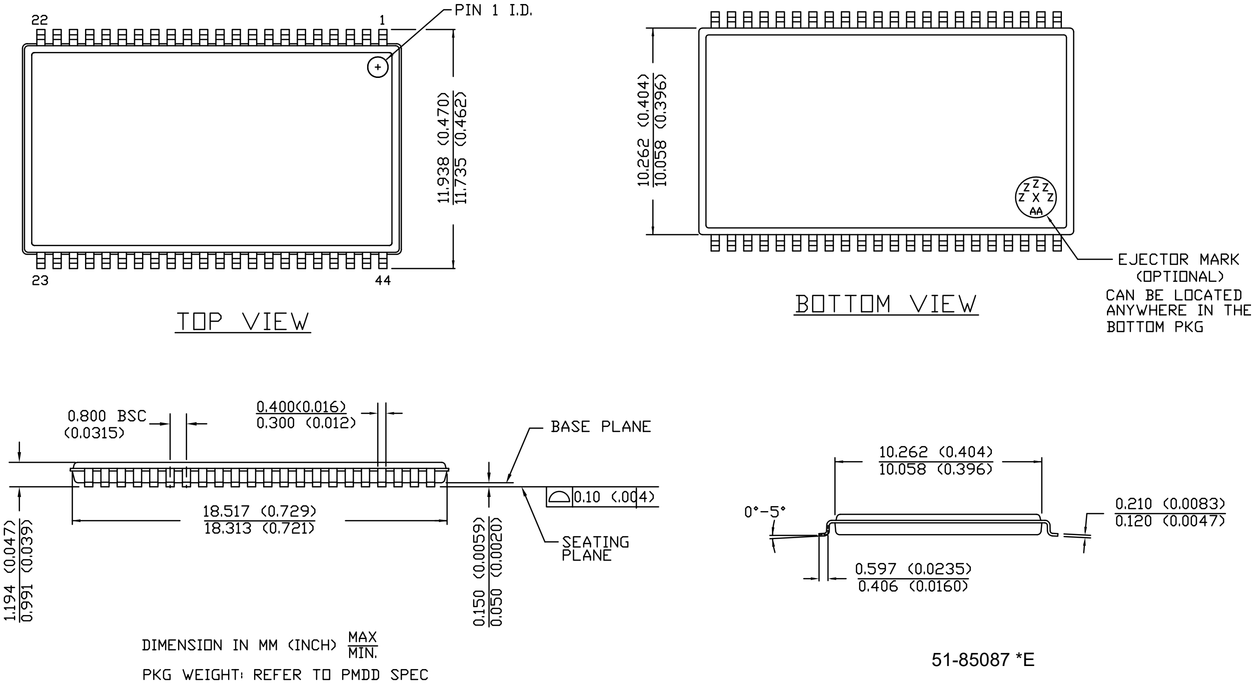
Figure 11. 48-ball VFBGA (6 × 8 × 1.2 mm) BA48M/BK48M (0.35 mm Ball Diameter) Package Outline, 001-85259



NOTES :

1. DIMENSIONS ARE IN MILLIMETERS
2. REFERENCE JEDEC STD : MO-216
3. * 0.32±0.05 FOR RAMTRON DEVICES

Figure 12. 44-pin TSOP Z44-II Package Outline, 51-85087



## Acronyms

**Table 1. Acronyms Used in this Document**

| Acronym | Description |
|---|---|
| $\overline{\text{BHE}}$ | Byte High Enable |
| $\overline{\text{BLE}}$ | Byte Low Enable |
| $\overline{\text{CE}}$ | Chip Enable |
| CMOS | Complementary Metal Oxide Semiconductor |
| I/O | Input/Output |
| $\overline{\text{OE}}$ | Output Enable |
| SRAM | Static Random Access Memory |
| TSOP | Thin Small Outline Package |
| TTL | Transistor-Transistor Logic |
| VFBGA | Very Fine-Pitch Ball Grid Array |
| $\overline{\text{WE}}$ | Write Enable |

## Document Conventions

### Units of Measure

**Table 2. Units of Measure**

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| MHz | megahertz |
| µA | microampere |
| µs | microsecond |
| mA | milliampere |
| mm | millimeter |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

## Document History Page

| Document Title: CY7C1041G Automotive, 4-Mbit (256K words × 16-bit) Static RAM with Error-Correcting Code (ECC)<br>Document Number: 001-91255 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *F | 4996293 | NILE | 10/30/2015 | Changed status from Preliminary to Final. |
| *G | 5026902 | NILE | 11/25/2015 | Added Automotive-A Temperature Range related information in all instances across the document.<br>Updated Ordering Information:<br>Updated part numbers. |
| *H | 5427560 | NILE | 09/07/2016 | Updated Maximum Ratings:<br>Updated Note 5 (Replaced “2 ns” with “20 ns”).<br>Updated DC Electrical Characteristics:<br>Removed details of $V_{OH}$ parameter corresponding to Test Condition “2.7 V to 3.6 V”.<br>Added details of $V_{OH}$ parameter corresponding to Test Conditions “2.7 V to 3.0 V” and “3.0 V to 3.6 V”.<br>Updated Ordering Information:<br>Updated part numbers.<br>Updated to new template. |
| *I | 5787756 | NILE | 06/27/2017 | Updated to new template.<br>Completing Sunset Review. |
| *J | 6249178 | NILE | 07/16/2018 | Updated Features:<br>Added “AEC-Q100 qualified”.<br>Added Note 2 and referred the same note in “Embedded ECC for single-bit error correction”.<br>Updated to new template.<br>Completing Sunset Review. |

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