

## AT25DL161

### 16-Mbit, 1.65 V Minimum SPI Serial Flash Memory with Dual-I/O Support

#### Features

- Single 1.65 V – 1.95 V supply
- Serial Peripheral Interface (SPI) compatible
  - Supports SPI Modes 0 and 3
  - Supports RapidS™ operation
  - Supports Dual-Input Program and Dual-Output Read
- Very high operating frequencies
  - 100 MHz for RapidS
  - 85 MHz for SPI
  - Clock-to-output time ( $t_{\text{CO}}$ ) of 5 ns maximum
- Flexible, optimized erase architecture for code + data storage applications
  - Uniform 4-kB, 32-kB, and 64-kB Block Erase
  - Full-Chip Erase
- Individual sector protection with Global Protect/Unprotect feature
  - 32 sectors of 64 kB each
- Hardware controlled locking of protected sectors via  $\overline{\text{WP}}$  pin
- Sector Lock-down with permanent freeze option
  - Make any combination of 64KB sectors permanently read-only
- 128-byte, One-Time Programmable (OTP) Security Register
  - 64 bytes factory preprogrammed, 64 bytes user programmable
- Flexible programming
  - Byte/Page Program (1 to 256 bytes)
- Fast program and erase times
  - 1.0 ms typical Page Program (256 bytes) time
  - 50 ms typical 4-kB Block Erase time
  - 250 ms typical 32-kB Block Erase time
  - 550 ms typical 64-kB Block Erase time
- Program and Erase Suspend/Resume
- Automatic checking and reporting of erase/program failures
- Software controlled reset
- JEDEC Standard Manufacturer and Device ID Read Methodology
- Low power dissipation
  - 10 mA Active Read current (typical at 20 MHz)
  - 8  $\mu\text{A}$  Deep Power-Down current (typical)
- Endurance:
  - 100,000 program/erase cycles (-40 °C to +85 °C)
  - 20,000 program/erase cycles (-40 °C to +105 °C)
- Data retention: 20 years
- Complies with full industrial temperature range
- Industry standard green (Pb/halide-free/RoHS-compliant) package options
  - 8-lead SOIC (150-mil wide)
  - 8-pad Ultra-thin DFN (5 x 6 x 0.6 mm)

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## 1. Description

The AT25DL161 is a serial interface Flash memory device designed for use in a wide variety of high-volume, consumer-based applications in which program code is shadowed from Flash memory into embedded or external RAM for execution. The flexible erase architecture of the AT25DL161, with its erase granularity as small as 4 kB, makes it ideal for data storage as well, eliminating the need for additional data storage EEPROM devices.

The physical sectoring and the erase block sizes of the AT25DL161 have been optimized to meet the needs of today's code and data storage applications. By optimizing the size of the physical sectors and erase blocks, the memory space can be used much more efficiently. Because certain code modules and data storage segments must reside by themselves in their own protected sectors, the wasted and unused memory space that occurs with large sectored and large Block Erase Flash memory devices can be greatly reduced. This increased memory space efficiency allows additional code routines and data storage segments to be added, while still maintaining the same overall device density.

The AT25DL161 also offers a sophisticated method for protecting individual sectors against erroneous or malicious program and erase operations. By providing the ability to individually protect and unprotect sectors, a system can unprotect a specific sector to modify its contents while keeping the remaining sectors of the memory array securely protected. This is useful in applications where program code is patched, updated on a subroutine or module basis, or in applications where data storage segments need to be modified without running the risk of errant modifications to the program code segments. In addition to individual sector protection capabilities, the AT25DL161 incorporates Global Protect and Global Unprotect features that allow the entire memory array to be either protected or unprotected all at once. This reduces overhead during the manufacturing process because sectors do not have to be unprotected one by one prior to initial programming.

To take code and data protection to the next level, the AT25DL161 incorporates a sector lockdown mechanism that allows any combination of individual 64 kB sectors to be locked down and become permanently read-only. This addresses the need of certain secure applications that require portions of the Flash memory array to be permanently protected against malicious attempts at altering program code, data modules, security information or encryption/decryption algorithms, keys, and routines. The device also contains a specialized, OTP (One-Time Programmable) security register, which can be used for unique device serialization, system-level Electronic Serial Number (ESN) storage, locked key storage, or other purposes.

Specifically designed for use in 1.8 V systems, the AT25DL161 supports read, program, and erase operations with a supply voltage range of 1.65 V to 1.95 V. No separate voltage is required for programming and erasing.

## 2. Pin Descriptions and Pinouts

Table 1. Pin Descriptions

Symbol	Name and Function	Asserted State	Type
$\overline{\text{CS}}$	<p><b>Chip Select:</b> Asserting the <math>\overline{\text{CS}}</math> pin selects the device. When the <math>\overline{\text{CS}}</math> pin is deasserted, the device is deselected and normally be placed in standby mode (not deep Power-Down mode) and the SO pin is in a high-impedance state. When the device is deselected, data are not accepted on the SI pin.</p> <p>A high-to-low transition on the <math>\overline{\text{CS}}</math> pin is required to start an operation and a low-to-high transition is required to end an operation. When ending an internally self-timed operation, such as a program or erase cycle, the device does not enter the standby mode until the completion of the operation.</p>	Low	Input
SCK	<p><b>Serial Clock:</b> This pin is used to provide a clock to the device and is used to control the flow of data to and from the device. Command, address, and input data present on the SI pin is always latched in on the rising edge of SCK, while output data on the SO pin is always clocked out on the falling edge of SCK.</p>	—	Input
SI (SIO)	<p><b>Serial Input (Serial Input/Output):</b> The SI pin is used to shift data into the device. The SI pin is used for all data input including command and address sequences. Data on the SI pin is always latched in on the rising edge of SCK.</p> <p>With the Dual-Output Read Array command, the SI pin becomes an output pin (SIO) to allow two bits (on the SO and SIO pins) of data to be clocked out on every falling edge of SCK. To maintain consistency with SPI nomenclature, the SIO pin is referenced as SI throughout this document except for those sections dealing with the Dual-Output Read Array command, in which it is referenced as SIO.</p> <p>Data present on the SI pin are ignored whenever the device is deselected (<math>\overline{\text{CS}}</math> is deasserted).</p>	—	Input/Output
SO (SOI)	<p><b>Serial Output (Serial Output/Input):</b> The SO pin is used to shift data out from the device. Data on the SO pin is always clocked out on the falling edge of SCK.</p> <p>With the Dual-Input Byte/Page Program command, the SO pin becomes an input pin (SOI) to allow two bits (on the SOI and SI pins) of data to be clocked in on every rising edge of SCK. To maintain consistency with nomenclature, the SOI pin is referenced as SO throughout this document except for those sections dealing with the Dual-Input Byte/Page Program command in which it is referenced as SOI.</p> <p>The SO pin is in a high-impedance state whenever the device is deselected (<math>\overline{\text{CS}}</math> is deasserted).</p>	—	Input/Output
$\overline{\text{WP}}$	<p><b>Write Protect:</b> The <math>\overline{\text{WP}}</math> pin controls the hardware locking feature of the device. See <a href="#">“Protection Commands and Features” on page 25</a> for more details on protection features and the <math>\overline{\text{WP}}</math> pin.</p> <p>The <math>\overline{\text{WP}}</math> pin is internally pulled-high and can be left floating if hardware controlled protection is not used. However, it is recommended that the <math>\overline{\text{WP}}</math> pin also be externally connected to <math>V_{\text{CC}}</math> whenever possible.</p>	Low	Input

Table 1. Pin Descriptions (Continued)

Symbol	Name and Function	Asserted State	Type
$\overline{\text{HOLD}}$	<p><b>Hold:</b> The <math>\overline{\text{HOLD}}</math> pin is used to temporarily pause serial communication without deselecting or resetting the device. While the <math>\overline{\text{HOLD}}</math> pin is asserted, transitions on the SCK pin and data on the SI pin are ignored and the SO pin is in a high-impedance state.</p> <p>The <math>\overline{\text{CS}}</math> pin must be asserted and the SCK pin must be in the low state in order for a Hold condition to start. A Hold condition pauses serial communication only and does not have an affect on internally self-timed operations, such as a program or erase cycle. See “Hold” on page 51 for additional details on the Hold operation.</p> <p>The <math>\overline{\text{HOLD}}</math> pin is internally pulled-high and can be left floating if the Hold function is not used. However, it is recommended that the <math>\overline{\text{HOLD}}</math> pin also be externally connected to the <math>V_{\text{CC}}</math> whenever possible.</p>	Low	Input
$V_{\text{CC}}$	<p><b>Device Power Supply:</b> The <math>V_{\text{CC}}</math> pin is used to supply the source voltage to the device. Operations at invalid <math>V_{\text{CC}}</math> voltages can produce spurious results and must not be attempted.</p>	—	Power
GND	<p><b>Ground:</b> The ground reference for the power supply. GND must be connected to the system ground.</p>	—	Power

Figure 1. 8-lead SOIC

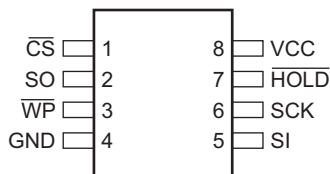
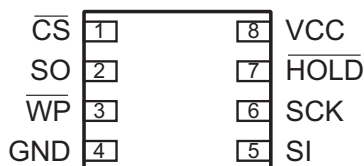
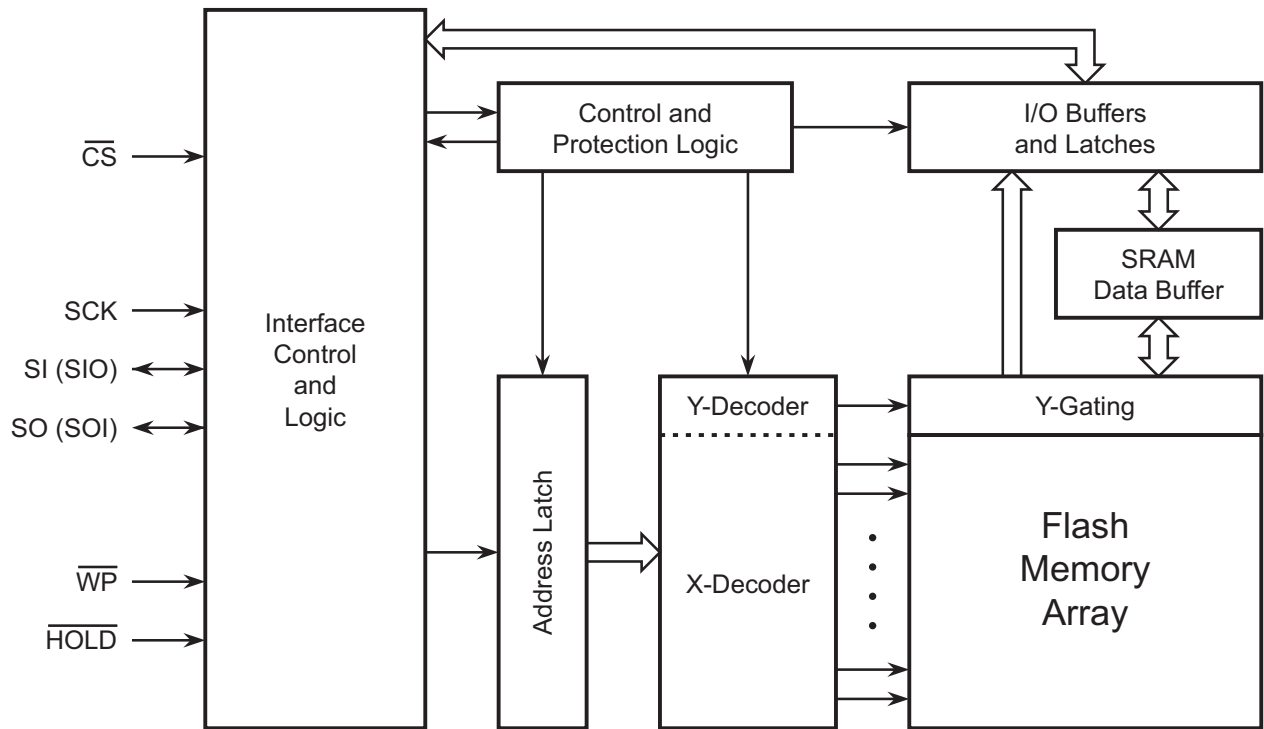


Figure 2. 8-pad UDFN





### 3. Block Diagram



Note: SIO and SOI pin naming convention is used for Dual-I/O commands.

Figure 3. Block Diagram

## 4. Memory Array

To provide the greatest flexibility, the AT25DL161 memory array can be erased in four levels of granularity, including a full Chip Erase. In addition, the array has been divided into physical sectors of uniform size, which can be individually protected from program and erase operations. The size of the physical sectors is optimized for both code and data storage applications, allowing both code and data segments to reside in their own isolated regions. The memory architecture diagram illustrates the breakdown of each erase level, as well as the breakdown of each physical sector.

Internal Sectoring for Protection, Lockdown, and Suspend Functions	Block Erase Detail				Page Program Detail	
	64KB Block Erase (D8h Command)	32KB Block Erase (52h Command)	4KB Block Erase (20h Command)	Block Address Range	1-256 byte Page Program (02h Command)	Page Address Range
64KB (Sector 31)	64KB	32KB	4KB	1FFFFh – 1FF00h	256 bytes	1FFFFh – 1FF00h
			4KB	1FEFFFh – 1FE00h	256 bytes	1FEFFFh – 1FE00h
			4KB	1FDFFFh – 1FD00h	256 bytes	1FDFFFh – 1FD00h
			4KB	1FCFFFh – 1FC00h	256 bytes	1FCFFFh – 1FC00h
			4KB	1FBFFFh – 1FB00h	256 bytes	1FBFFFh – 1FB00h
			4KB	1FAFFFh – 1FA00h	256 bytes	1FAFFFh – 1FA00h
			4KB	1F9FFFh – 1F900h	256 bytes	1F9FFFh – 1F900h
		32KB	4KB	1F8FFFh – 1F800h	256 bytes	1F8FFFh – 1F800h
			4KB	1F7FFFh – 1F700h	256 bytes	1F7FFFh – 1F700h
			4KB	1F6FFFh – 1F600h	256 bytes	1F6FFFh – 1F600h
			4KB	1F5FFFh – 1F500h	256 bytes	1F5FFFh – 1F500h
			4KB	1F4FFFh – 1F400h	256 bytes	1F4FFFh – 1F400h
			4KB	1F3FFFh – 1F300h	256 bytes	1F3FFFh – 1F300h
			4KB	1F2FFFh – 1F200h	256 bytes	1F2FFFh – 1F200h
64KB (Sector 30)	64KB	32KB	4KB	1EFFFh – 1EF00h	256 bytes	1EFFFh – 1EF00h
			4KB	1EFFFFh – 1EE00h	256 bytes	1EFFFFh – 1EE00h
			4KB	1EDFFFh – 1ED00h	256 bytes	1EDFFFh – 1ED00h
			4KB	1ECFFFh – 1EC00h	256 bytes	1ECFFFh – 1EC00h
			4KB	1EBFFFh – 1EB00h	256 bytes	1EBFFFh – 1EB00h
			4KB	1EAFh – 1EA00h	256 bytes	1EAFh – 1EA00h
			4KB	1E9FFFh – 1E900h	256 bytes	1E9FFFh – 1E900h
		32KB	4KB	1E8FFFh – 1E800h	256 bytes	1E8FFFh – 1E800h
			4KB	1E7FFFh – 1E700h	256 bytes	1E7FFFh – 1E700h
			4KB	1E6FFFh – 1E600h	256 bytes	1E6FFFh – 1E600h
			4KB	1E5FFFh – 1E500h	256 bytes	1E5FFFh – 1E500h
			4KB	1E4FFFh – 1E400h	256 bytes	1E4FFFh – 1E400h
			4KB	1E3FFFh – 1E300h	256 bytes	1E3FFFh – 1E300h
			4KB	1E2FFFh – 1E200h	256 bytes	1E2FFFh – 1E200h
64KB (Sector 0)	64KB	32KB	4KB	1E1FFFh – 1E100h	256 bytes	1E1FFFh – 1E100h
			4KB	1E0FFFh – 1E000h	256 bytes	1E0FFFh – 1E000h
			4KB	00FFFh – 00F00h	256 bytes	00FFFh – 00F00h
			4KB	00EFFFh – 00E00h	256 bytes	00EFFFh – 00E00h
			4KB	00DFFFh – 00D00h	256 bytes	00DFFFh – 00D00h
			4KB	00CFFFh – 00C00h	256 bytes	00CFFFh – 00C00h
			4KB	00BFFFh – 00B00h	256 bytes	00BFFFh – 00B00h
		32KB	4KB	00AFFh – 00A00h	256 bytes	00AFFh – 00A00h
			4KB	009FFFh – 00900h	256 bytes	009FFFh – 00900h
			4KB	008FFFh – 00800h	256 bytes	008FFFh – 00800h
			4KB	007FFFh – 00700h	256 bytes	007FFFh – 00700h
			4KB	006FFFh – 00600h	256 bytes	006FFFh – 00600h
			4KB	005FFFh – 00500h	256 bytes	005FFFh – 00500h
			4KB	004FFFh – 00400h	256 bytes	004FFFh – 00400h
32KB	4KB	003FFFh – 00300h	256 bytes	003FFFh – 00300h		
	4KB	002FFFh – 00200h	256 bytes	002FFFh – 00200h		
	4KB	001FFFh – 00100h	256 bytes	001FFFh – 00100h		
	4KB	000FFFh – 00000h	256 bytes	000FFFh – 00000h		

Figure 4. Memory Architecture Diagram

## 5. Device Operation

The AT25DL161 is controlled by a set of instructions that are sent from a host controller, commonly referred to as the SPI master. The SPI master communicates with the AT25DL161 via the SPI bus, which is comprised of four signal lines: Chip Select ( $\overline{CS}$ ), Serial Clock (SCK), Serial Input (SI), and Serial Output (SO).

The SPI protocol defines a total of four modes of operation (Mode 0, 1, 2, or 3), with each mode differing in respect to the SCK polarity and phase and how the polarity and phase control the flow of data on the SPI bus. The AT25DL161 supports the two most common modes, SPI Modes 0 and 3. The only difference between SPI Modes 0 and 3 is the polarity of the SCK signal when in the inactive state (when the SPI master is in standby mode and not transferring any data). With SPI Modes 0 and 3, data is always latched in on the rising edge of SCK and always output on the falling edge of SCK.

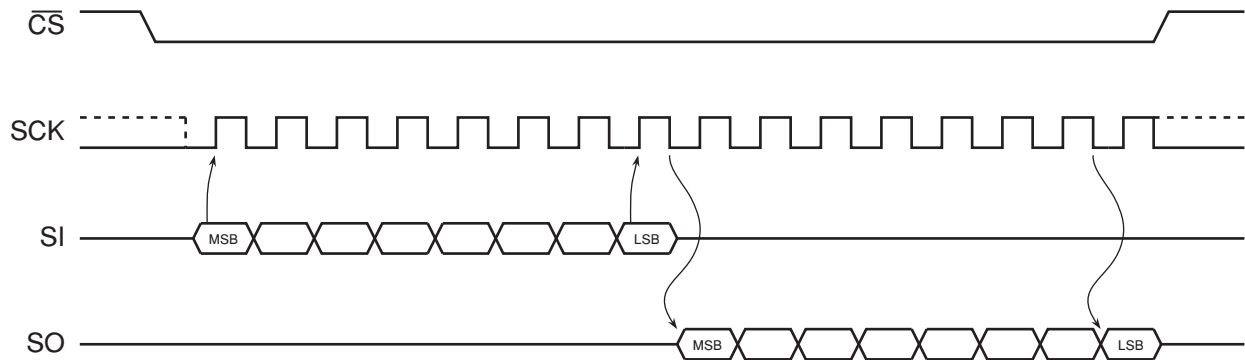


Figure 5. SPI Mode 0 and 3

### 5.1 Dual-I/O Operation

The AT25DL161 features a Dual-Input Program mode and a Dual-Output Read mode that allow two bits of data to be clocked into or out of the device every clock cycle to improve throughput. To accomplish this, both the SI and SO pins are utilized as inputs/outputs for the transfer of data bytes. With the Dual-Input Byte/page Program command, the SO pin becomes an input along with the SI pin. Alternatively, with the Dual-Output Read Array command, the SI pin becomes an output along with the SO pin. For both Dual-I/O commands, the SO pin is referred to as the SOI (Serial Output/Input) pin and the SI pin is referred to as the SIO (Serial Input/Output) pin.

## 6. Commands and Addressing

A valid instruction or operation must always be started by first asserting the  $\overline{CS}$  pin. After the  $\overline{CS}$  pin has been asserted, the host controller must then clock out a valid 8-bit opcode on the SPI bus. Following the opcode, instruction-dependent information, such as address and data bytes, would then be clocked out by the host controller. All opcode, address, and data bytes are transferred with the Most-Significant Bit (MSB) first. An operation is ended by deasserting the  $\overline{CS}$  pin.

Opcodes not supported by the AT25DL161 are ignored by the device and no operation is started. The device continues to ignore any data presented on the SI pin until the start of the next operation ( $\overline{CS}$  pin being deasserted and then reasserted). In addition, if the  $\overline{CS}$  pin is deasserted before complete opcode and address information is sent to the device, then no operation is performed, and the device simply returns to the idle state and wait for the next operation.

Addressing of the device requires a total of three bytes of information to be sent, representing address bits A23-A0. Since the upper address limit of the AT25DL161 memory array is 1FFFFFFh, address bits A23-A21 are always ignored by the device.

Table 2. Command Listing

Command			Clock Frequency	Address Bytes	Dummy Bytes	Data Bytes
<b>Read Commands</b>						
Read Array	1Bh	0001 1011	Up to 100 MHz	3	2	1+
	0Bh	0000 1011	Up to 85 MHz	3	1	1+
	03h	0000 0011	Up to 40 MHz	3	0	1+
Dual-Output Read Array	3Bh	0011 1011	Up to 66 MHz	3	1	1+
<b>Program and Erase Commands</b>						
Block Erase (4 kB)	20h	0010 0000	Up to 100 MHz	3	0	0
Block Erase (32 kB)	52h	0101 0010	Up to 100 MHz	3	0	0
Block Erase (64 kB)	D8h	1101 1000	Up to 100 MHz	3	0	0
Chip Erase	60h	0110 0000	Up to 100 MHz	0	0	0
	C7h	1100 0111	Up to 100 MHz	0	0	0
Byte/Page Program (1 to 256 bytes)	02h	0000 0010	Up to 100 MHz	3	0	1+
Dual-Input Byte/Page Program (1 to 256 bytes)	A2h	1010 0010	Up to 100 MHz	3	0	1+
Program/Erase Suspend	B0h	1011 0000	Up to 100 MHz	0	0	0
Program/Erase Resume	D0h	1101 0000	Up to 100 MHz	0	0	0
<b>Protection Commands</b>						
Write Enable	06h	0000 0110	Up to 100 MHz	0	0	0
Write Disable	04h	0000 0100	Up to 100 MHz	0	0	0
Protect Sector	36h	0011 0110	Up to 100 MHz	3	0	0
Unprotect Sector	39h	0011 1001	Up to 100 MHz	3	0	0
Global Protect/Unprotect	Use Write Status Register Byte 1 Command					
Read Sector Protection Registers	3Ch	0011 1100	Up to 100 MHz	3	0	1+

Table 2. Command Listing (Continued)

Command			Clock Frequency	Address Bytes	Dummy Bytes	Data Bytes
<b>Security Commands</b>						
Sector Lockdown	33h	0011 0011	Up to 100 MHz	3	0	1
Freeze Sector Lockdown State	34h	0011 0100	Up to 100 MHz	3	0	1
Read Sector Lockdown Registers	35h	0011 0101	Up to 100 MHz	3	0	1+
Program OTP Security Register	9Bh	1001 1011	Up to 100 MHz	3	0	1+
Read OTP Security Register	77h	0111 0111	Up to 100 MHz	3	2	1+
<b>Status Register Commands</b>						
Read Status Register	05h	0000 0101	Up to 100 MHz	0	0	1+
Write Status Register Byte 1	01h	0000 0001	Up to 100 MHz	0	0	1
Write Status Register Byte 2	31h	0011 0001	Up to 100 MHz	0	0	1
<b>Miscellaneous Commands</b>						
Reset	F0h	1111 0000	Up to 100 MHz	0	0	1
Read Manufacturer and Device ID	9Fh	1001 1111	Up to 85 MHz	0	0	1 to 5
Deep Power-Down	B9h	1011 1001	Up to 100 MHz	0	0	0
Resume from Deep Power-Down	ABh	1010 1011	Up to 100 MHz	0	0	0

## 7. Read Commands

### 7.1 Read Array

The Read Array command can be used to sequentially read a continuous stream of data from the device by simply providing the clock signal once the initial starting address has been specified. The device incorporates an internal address counter that automatically increments on every clock cycle.

Three opcodes (1Bh, 0Bh, and 03h) can be used for the Read Array command. The use of each opcode depends on the maximum clock frequency that is used to read data from the device. The 0Bh opcode can be used at any clock frequency up to the maximum specified by  $f_{CLK}$ , and the 03h opcode can be used for lower frequency read operations, up to the maximum specified by  $f_{RDLF}$ . The 1Bh opcode allows the highest read performance possible and can be used at any clock frequency up to the maximum specified by  $f_{MAX}$ ; however, use of the 1Bh opcode at clock frequencies above  $f_{CLK}$  must be reserved for systems employing the RapidS protocol.

To perform the Read Array operation, the  $\overline{CS}$  pin must first be asserted and then the appropriate opcode (1Bh, 0Bh, or 03h) must be clocked into the device. After the opcode has been clocked in, the three address bytes must be clocked in to specify the location of the first byte to read within the memory array. Following the three address bytes, additional dummy bytes may need to be clocked into the device, depending on which opcode is used for the Read Array operation. If the 1Bh opcode is used, then two dummy bytes must be clocked into the device after the three address bytes. If the 0Bh opcode is used, then a single dummy byte must be clocked in after the address bytes.

After the three address bytes (and any dummy bytes) have been clocked in, additional clock cycles result in data being output on the SO pin. The data is always output with the MSB of a byte first. When the last byte (1FFFFh) of the memory array has been read, the device continues reading from the beginning of the array (00000h). No delays are incurred when wrapping around from the end of the array to the beginning of the array.

Deasserting the  $\overline{CS}$  pin terminates the read operation and put the SO pin into a high-impedance state. The  $\overline{CS}$  pin can be deasserted at any time and does not require that a full byte of data be read.

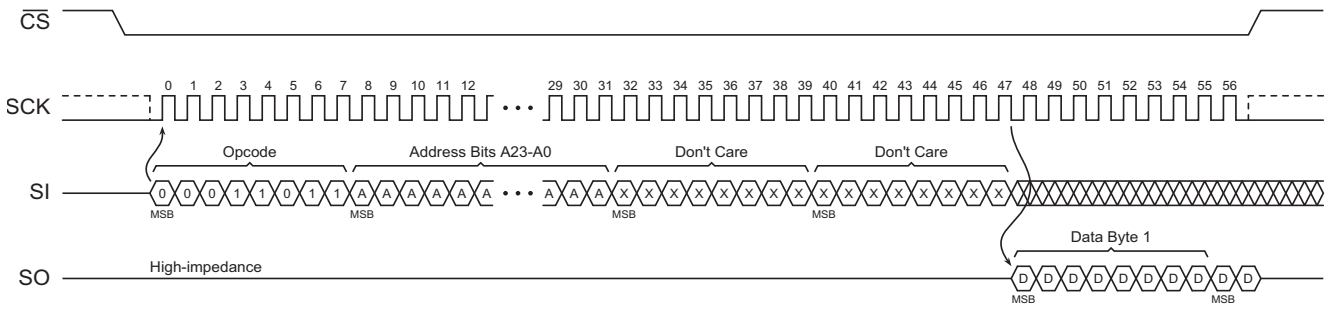


Figure 6. Read Array – 1Bh Opcode

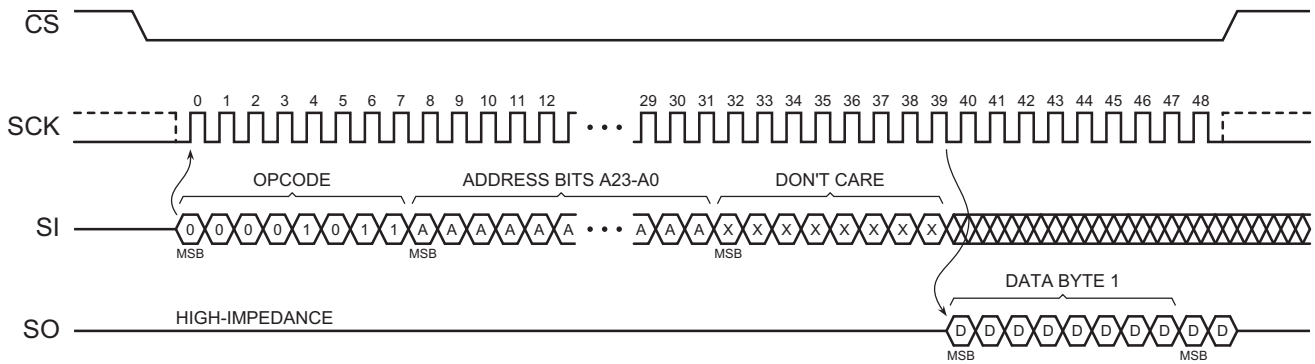


Figure 7. Read Array – 0Bh Opcode

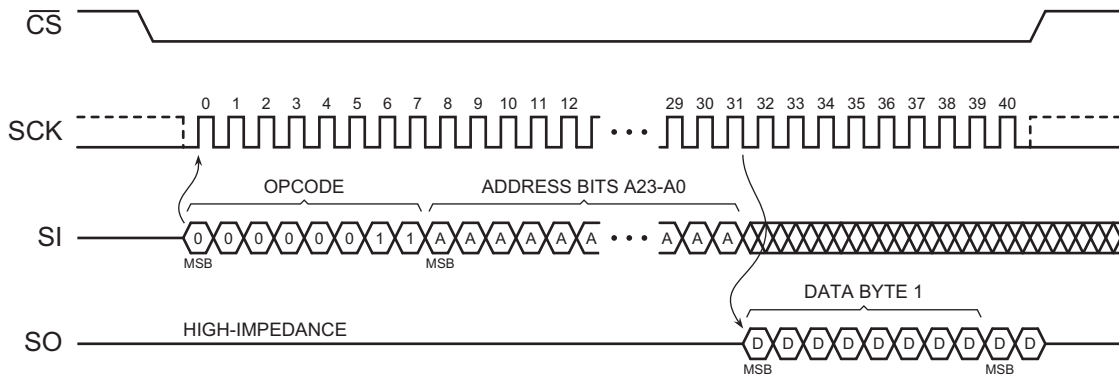


Figure 8. Read Array – 03h Opcode

## 7.2 Dual-Output Read Array

The Dual-Output Read Array command is similar to the standard Read Array command and can be used to sequentially read a continuous stream of data from the device by simply providing the clock signal once the initial starting address has been specified. Unlike the standard Read Array command, however, the Dual-Output Read Array command allows two bits of data to be clocked out of the device on every clock cycle, rather than just one.

The Dual-Output Read Array command can be used at any clock frequency, up to the maximum specified by  $f_{RDO}$ . To perform the Dual-Output Read Array operation, the  $\overline{CS}$  pin must first be asserted and then the opcode 3Bh must be clocked into the device. After the opcode has been clocked in, the three address bytes must be clocked in to specify the location of the first byte to read within the memory array. Following the three address bytes, a single dummy byte must also be clocked into the device.

After the three address bytes and the dummy byte have been clocked in, additional clock cycles results in data being output on both the SO and SIO pins. The data is always output with the MSB of a byte first and the MSB is always output on the SO pin. During the first clock cycle, bit 7 of the first data byte is output on the SO pin, while bit 6 of the same data byte is output on the SIO pin. During the next clock cycle, bits 5 and 4 of the first data byte are output on the SO and SIO pins, respectively. The sequence continues with each byte of data being output after every four clock cycles. When the last byte (1FFFFh) of the memory array has been read, the device continues reading from the beginning of the array (00000h). No delays are incurred when wrapping around from the end of the array to the beginning of the array.

Deasserting the  $\overline{CS}$  pin terminates the read operation and put the SO and SIO pins into a high-impedance state. The  $\overline{CS}$  pin can be deasserted at any time and does not require that a full byte of data be read.

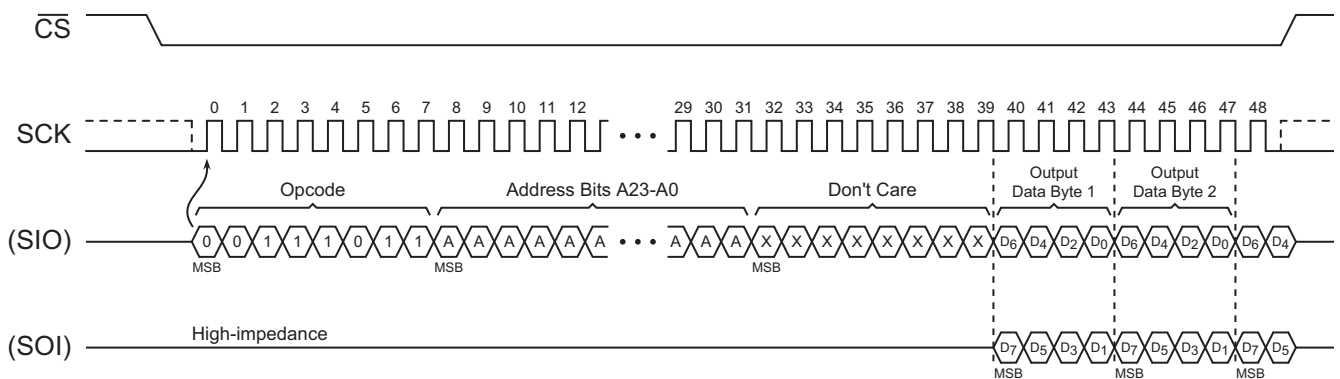


Figure 9. Dual-Output Read Array



## 8. Program and Erase Commands

### 8.1 Byte/Page Program

The Byte/Page program command allows anywhere from a single byte of data to 256 bytes of data to be programmed into previously erased memory locations. An erased memory location is one that has all eight bits set to the Logical 1 state (a byte value of FFh). Before a byte/page program command can be started, the Write Enable command must have been previously issued to the device (see “Write Enable” on page 25) to set the Write Enable Latch (WEL) bit of the Status Register to a Logical 1 state.

To perform a Byte/Page Program command, a 02h opcode must be clocked into the device followed by the three address bytes denoting the first location of the memory array to begin programming at. After the address bytes have been clocked in, data can then be clocked into the device and be stored in an internal buffer.

If the starting memory address denoted by A23-A0 does not fall on an even 256-byte page boundary (A7-A0 are not all 0), then special circumstances regarding which memory locations are to be programmed apply. In this situation, any data that are sent to the device that go beyond the end of the page wrap around to the beginning of the same page. In addition, if more than 256 bytes of data are sent to the device, then only the last 256 bytes sent are latched into the internal buffer.

**Example:** If the starting address denoted by A23-A0 is 0000FEh and three bytes of data are sent to the device, then the first two bytes of data are programmed at addresses 0000FEh and 0000FFh, while the last byte of data is programmed at address 000000h. The remaining bytes in the page (addresses 000001h through 0000FDh) are not programmed and remain in the erased state (FFh).

When the  $\overline{\text{CS}}$  pin is deasserted, the device programs the data stored in the internal buffer into the appropriate memory array locations based on the starting address specified by A23-A0 and the number of data bytes sent to the device. If fewer than 256 bytes of data are sent to the device, then the remaining bytes within the page are not programmed and remains in the erased state (FFh). The programming of the data bytes is internally self-timed and takes place in a time of  $t_{\text{PP}}$  or  $t_{\text{BP}}$  if only programming a single byte.

The three address bytes and at least one complete byte of data must be clocked into the device before the  $\overline{\text{CS}}$  pin is deasserted, and the  $\overline{\text{CS}}$  pin must be deasserted on even byte boundaries (multiples of eight bits); otherwise, the device aborts the operation and no data are programmed into the memory array. In addition, if the address specified by A23-A0 points to a memory location within a sector that is in the protected state (see “Protect Sector” on page 27) or locked down (see “Sector Lockdown” on page 33), then the Byte/Page Program command is not executed and the device returns to the idle state once the  $\overline{\text{CS}}$  pin has been deasserted. The WEL bit in the Status Register is reset back to the Logical 0 state if the program cycle aborts due to an incomplete address being sent, an incomplete byte of data being sent, the  $\overline{\text{CS}}$  pin being deasserted on uneven byte boundaries, or because the memory location to be programmed is protected or locked down.

While the device is programming, the Status Register can be read and indicates that the device is busy. For faster throughput, it is recommended that the Status Register be polled rather than waiting the  $t_{\text{BP}}$  or  $t_{\text{PP}}$  time to determine if the data bytes have finished programming. At some point before the program cycle completes, the WEL bit in the Status Register is reset back to the Logical 0 state.

The device also incorporates an intelligent programming algorithm that can detect when a byte location fails to program properly. If a programming error arises, it is indicated by the EPE bit in the Status Register.

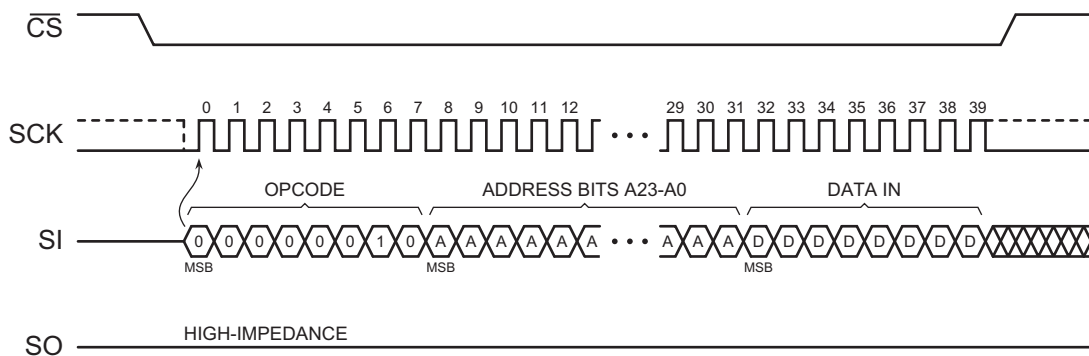


Figure 10. Byte Program

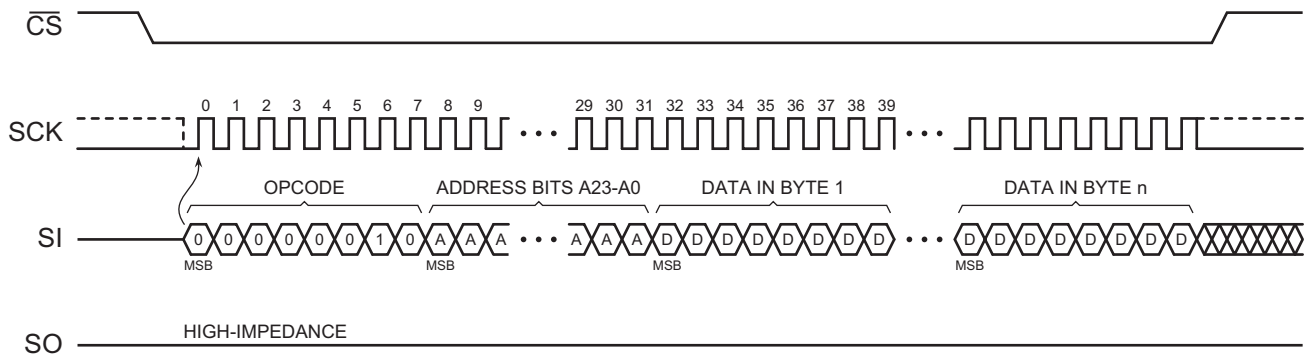


Figure 11. Page Program

## 8.2 Dual-Input Byte/Page Program

The Dual-Input Byte/Page Program command is similar to the standard Byte/Page Program command and can be used to program anywhere from a single byte of data up to 256 bytes of data into previously erased memory locations. Unlike the standard byte/page program command, however, the Dual-Input Byte/Page Program command allows two bits of data to be clocked into the device on every clock cycle rather than just one.

Before the Dual-Input Byte/Page Program command can be started, the Write Enable command must have been previously issued to the device (see “Write Enable” on page 25) to set the Write Enable Latch (WEL) bit of the Status Register to a Logical 1 state. To perform a Dual-Input Byte/Page Program command, an A2h opcode must be clocked into the device followed by the three address bytes denoting the first location of the memory array to begin programming at. After the address bytes have been clocked in, data can then be clocked into the device two bits at a time on both the SOI and SI pins.

The data is always input with the MSB of a byte first, and the MSB is always input on the SOI pin. During the first clock cycle, bit 7 of the first data byte is input on the SOI pin while bit 6 of the same data byte is input on the SI pin. During the next clock cycle, bits 5 and 4 of the first data byte are input on the SOI and SI pins, respectively. The sequence continues with each byte of data being input after every four clock cycles. Like the standard Byte/Page Program command, all data clocked into the device are stored in an internal buffer.

If the starting memory address denoted by A23-A0 does not fall on an even 256-byte page boundary (A7-A0 are not all 0), then special circumstances regarding which memory locations are to be programmed apply. In this situation, any data that are sent to the device that go beyond the end of the page wrap around to the beginning of the same page. In addition, if more than 256 bytes of data are sent to the device, then only the last 256 bytes sent are latched into the internal buffer.

**Example:** If the starting address denoted by A23-A0 is 0000FEh and three bytes of data are sent to the device, then the first two bytes of data are programmed at addresses 0000FEh and 0000FFh, while the last byte of data is programmed at address 000000h. The remaining bytes in the page (addresses 000001h through 0000FDh) are not programmed and remain in the erased state (FFh).

When the  $\overline{CS}$  pin is deasserted, the device programs the data stored in the internal buffer into the appropriate memory array locations based on the starting address specified by A23-A0 and the number of data bytes sent to the device. If fewer than 256 bytes of data are sent to the device, then the remaining bytes within the page are not programmed and remain in the erased state (FFh). The programming of the data bytes is internally self-timed and takes place in a time of  $t_{PP}$  or  $t_{BP}$  if only programming a single byte.

The three address bytes and at least one complete byte of data must be clocked into the device before the  $\overline{CS}$  pin is deasserted, and the  $\overline{CS}$  pin must be deasserted on even byte boundaries (multiples of eight bits); otherwise, the device aborts the operation and no data are programmed into the memory array. In addition, if the address specified by A23-A0 points to a memory location within a sector that is in the protected state (see “Protect Sector” on page 27) or locked down (see “Sector Lockdown” on page 33), then the Byte/Page Program command is not executed, and the device returns to the idle state once the  $\overline{CS}$  pin has been deasserted. The WEL bit in the Status Register is reset back to the Logical 0 state if the program cycle aborts due to an incomplete address being sent, an incomplete byte of data being sent, the  $\overline{CS}$  pin being deasserted on uneven byte boundaries, or because the memory location to be programmed is protected or locked down.

While the device is programming, the Status Register can be read and indicates that the device is busy. For faster throughput, it is recommended that the Status Register be polled rather than waiting the  $t_{BP}$  or  $t_{PP}$  time to determine if the data bytes have finished programming. At some point before the program cycle completes, the WEL bit in the Status Register is reset back to the Logical 0 state.

The device also incorporates an intelligent programming algorithm that can detect when a byte location fails to program properly. If a programming error arises, it is indicated by the EPE bit in the Status Register.

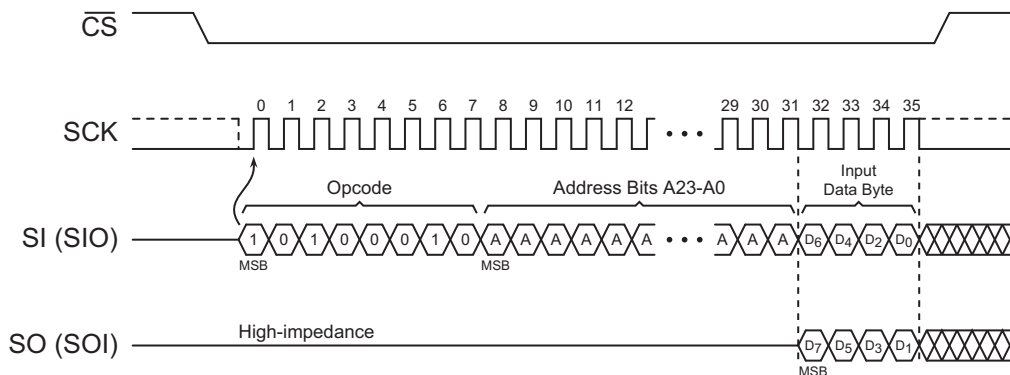


Figure 12. Dual-Input Byte Program

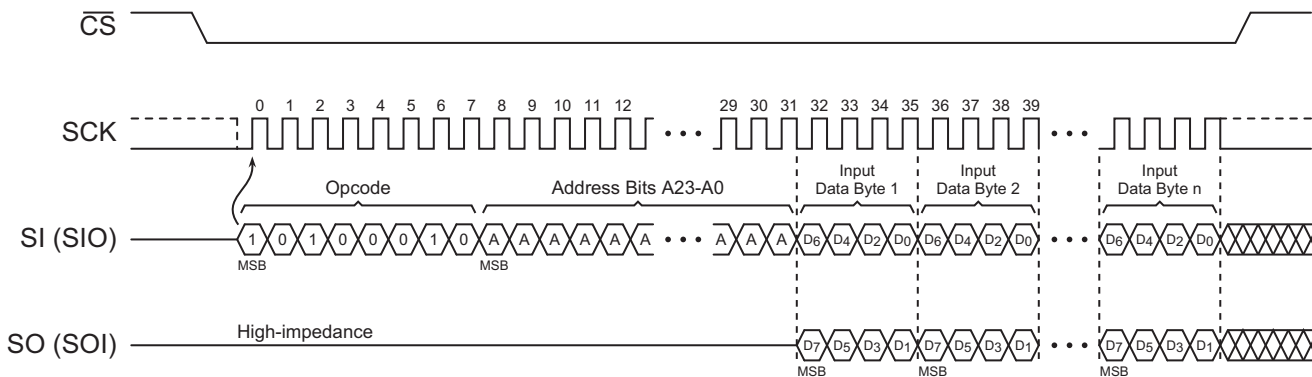


Figure 13. Dual-Input Page Program

### 8.3 Block Erase

A block of 4, 32, or 64 kB can be erased (all bits set to the Logical 1 state) in a single operation by using one of three different opcodes for the Block Erase command. An opcode of 20h is used for a 4 kB erase, an opcode of 52h is used for a 32 kB erase, and an opcode of D8h is used for a 64 kB erase. Before a Block Erase command can be started, the Write Enable command must have been previously issued to the device to set the WEL bit of the Status Register to a Logical 1 state.

To perform a Block Erase, the  $\overline{CS}$  pin must first be asserted and then the appropriate opcode (20h, 52h, or D8h) must be clocked into the device. After the opcode has been clocked in, three address bytes specifying the address within the 4, 32, or 64 kB block to be erased must be clocked in. Any additional data clocked into the device are ignored. When the  $\overline{CS}$  pin is deasserted, the device erases the appropriate block. The erasing of the block is internally self-timed and takes place in a time of  $t_{BLKE}$ .

Since the Block Erase command erases a region of bytes, the lower order address bits do not need to be decoded by the device. Therefore, for a 4 kB erase, address bits A11-A0 are ignored by the device and their values can be either a Logical 1 or 0. For a 32 kB erase, address bits A14-A0 are ignored and for a 64 kB erase, address bits A15-A0 are ignored. Despite the lower order address bits not being decoded by the device, the three complete address bytes must still be clocked into the device before the CS pin is deasserted, and the  $\overline{CS}$  pin must be deasserted on an even byte boundary (multiples of eight bits); otherwise, the device aborts the operation and no Erase operation is performed.

If the address specified by A23-A0 points to a memory location within a sector that is in the protected or locked down state, then the Block Erase command is not executed and the device returns to the idle state once the  $\overline{CS}$  pin has been deasserted.

The WEL bit in the Status Register is reset back to the Logical 0 state if the erase cycle aborts due to an incomplete address being sent, the  $\overline{CS}$  pin being deasserted on uneven byte boundaries, or because a memory location within the region to be erased is protected or locked down.

While the device is executing a successful erase cycle, the Status Register can be read and indicate that the device is busy. For faster throughput, it is recommended that the Status Register be polled rather than waiting the  $t_{BLKE}$  time to determine if the device has finished erasing. At some point before the erase cycle completes, the WEL bit in the Status Register is reset back to the Logical 0 state.

The device also incorporates an intelligent erase algorithm that can detect when a byte location fails to erase properly. If an erase error occurs, it is indicated by the EPE bit in the Status Register.

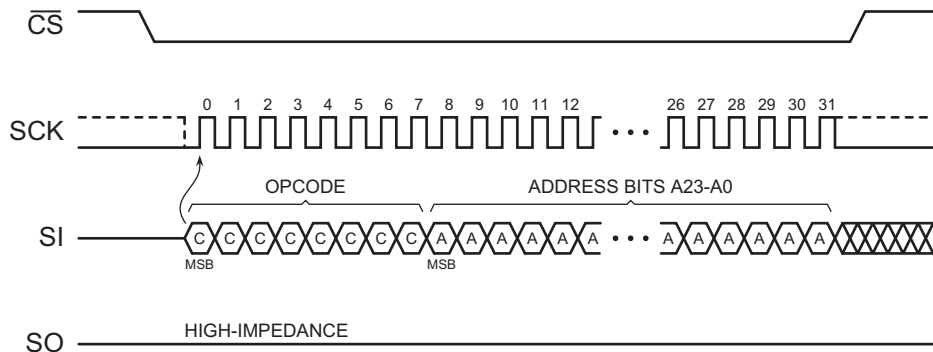


Figure 14. Block Erase

## 8.4 Chip Erase

The entire memory array can be erased in a single operation by using the Chip Erase command. Before a Chip Erase command can be started, the Write Enable command must have been previously issued to the device to set the WEL bit of the Status Register to a Logical 1 state.

Two opcodes, 60h and C7h, can be used for the Chip Erase command. There is no difference in device functionality when utilizing the two opcodes, so they can be used interchangeably. To perform a Chip Erase, one of the two opcodes (60h or C7h) must be clocked into the device. Since the entire memory array is to be erased, no address bytes need to be clocked into the device and any data clocked in after the opcode are ignored. When the  $\overline{CS}$  pin is deasserted, the device erases the entire memory array. The erasing of the device is internally self-timed and takes place in a time of  $t_{CHPE}$ .

The complete opcode must be clocked into the device before the  $\overline{CS}$  pin is deasserted, and the  $\overline{CS}$  pin must be deasserted on an even byte boundary (multiples of eight bits); otherwise, no erase is performed. In addition, if any sector of the memory array is in the protected or locked down state, then the Chip Erase command is not executed and the device returns to the idle state once the  $\overline{CS}$  pin has been deasserted. The WEL bit in the Status Register is reset back to the Logical 0 state if the  $\overline{CS}$  pin is deasserted on uneven byte boundaries or if a sector is in the protected or locked down state.

While the device is executing a successful erase cycle, the Status Register can be read and indicates that the device is busy. For faster throughput, it is recommended that the Status Register be polled rather than waiting the  $t_{CHPE}$  time to determine if the device has finished erasing. At some point before the erase cycle completes, the WEL bit in the Status Register is reset back to the Logical 0 state.

The device also incorporates an intelligent erase algorithm that can detect when a byte location fails to erase properly. If an erase error occurs, it is indicated by the EPE bit in the Status Register.

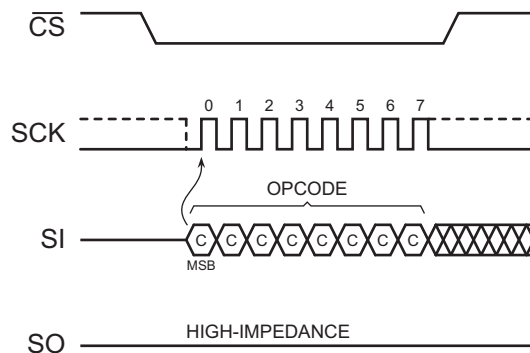


Figure 15. Chip Erase

## 8.5 Program/Erase Suspend

In some code-plus-data storage applications, it is often necessary to process certain high-level system interrupts that require relatively immediate reading of code or data from the Flash memory. In such an instance, it may not be possible for the system to wait the microseconds or milliseconds required for the Flash memory to complete a program or erase cycle. The Program/Erase Suspend command allows a program or erase operation in progress on a particular 64 kB sector of the Flash memory array to be suspended so that other device operations can be performed.

By suspending an erase operation on a particular sector, the system can perform a program or read operation within another 64 kB sector of the device. Other device operations, such as a Read Status Register, can also be performed while a program or erase operation is suspended. [Table 3](#) outlines the operations that are allowed and not allowed while a program or erase operation is suspended.

Since the need to suspend a program or erase operation is immediate, the Write Enable command does not need to be issued prior to the Program/Erase Suspend command being issued. Therefore, the Program/Erase Suspend command operates independently of the state of the WEL bit in the Status Register.

To perform a Program/Erase Suspend, the  $\overline{CS}$  pin must first be asserted and then the opcode B0h must be clocked into the device. No address bytes need to be clocked into the device, and any data clocked in after the opcode are ignored. When the  $\overline{CS}$  pin is deasserted, the program or erase operation currently in progress is suspended within a time of  $t_{SUSP}$ . The Program Suspend (PS) bit or the Erase Suspend (ES) bit in the Status Register then be set to the Logical 1 state to indicate that the program or erase operation has been suspended. In addition, the RDY/BSY bit in the Status Register indicate that the device is ready for another operation. The complete opcode must be clocked into the device before the  $\overline{CS}$  pin is deasserted, and the  $\overline{CS}$  pin must be deasserted on an even byte boundary (multiples of eight bits); otherwise, no suspend operation is performed.

Read operations are not allowed to a 64 kB sector that has had its program or erase operation suspended. If a read is attempted to a suspended sector, then the device output undefined data. Therefore, if performing a Read Array operation on an unsuspended sector, and if the device's internal address counter increments and crosses the sector boundary to a suspended sector, the device then start outputting undefined data continuously until the address counter increments and crosses a sector boundary to an unsuspended sector.

A program operation is not allowed on a sector that has been erase suspended. If a program operation is attempted on an erase suspended sector, then the program operation abort and the WEL bit in the Status Register is reset back to the Logical 0 state. Likewise, an erase operation is not allowed on a sector that has been program suspended. If attempted, the erase operation abort and the WEL bit in the Status Register is reset to a Logical 0 state.

During an Erase Suspend, a program operation to a different 64 kB sector can be started and subsequently suspended. This results in a simultaneous Erase Suspend/Program Suspend condition, which is indicated by the ES and PS bits in the Status Register being set to the Logical 1 state.

If a Reset operation (see [“Reset” on page 46](#)) is performed while a sector is erase suspended, the suspend operation abort and the contents of the block in the suspended sector are left in an undefined state. However, if a Reset is performed while a sector is program suspended, the suspend operation abort, but only the contents of the page that was being programmed and subsequently suspended is undefined. The remaining pages in the 64 kB sector retain their previous contents.

If an attempt is made to perform an operation that is not allowed while a program or erase operation is suspended, such as a Protect Sector command, then the device simply ignore the opcode and no operation is performed. The state of the WEL bit in the Status Register, as well as the SPRL (Sector Protection Registers Locked) and SLE (Sector Lockdown Enabled) bits, are not affected.

Table 3. Operations Allowed and Not Allowed During a Program/Erase Suspend

Command	Operation During Program Suspend	Operation During Erase Suspend
<b>Read Commands</b>		
Read Array (All Opcodes)	Allowed	Allowed
<b>Program and Erase Commands</b>		
Block Erase	Not Allowed	Not Allowed
Chip Erase	Not Allowed	Not Allowed
Byte/Page Program (All Opcodes)	Not Allowed	Allowed
Program/Erase Suspend	Not Allowed	Allowed
Program/Erase Resume	Allowed	Allowed
<b>Protection Commands</b>		
Write Enable	Not Allowed	Allowed
Write Disable	Not Allowed	Allowed
Protect Sector	Not Allowed	Not Allowed
Unprotect Sector	Not Allowed	Not Allowed
Global Protect/Unprotect	Not Allowed	Not Allowed
Read Sector Protection Registers	Allowed	Allowed
<b>Security Commands</b>		
Sector Lockdown	Not Allowed	Not Allowed
Freeze Sector Lockdown State	Not Allowed	Not Allowed
Read Sector Lockdown Registers	Allowed	Allowed
Program OTP Security Register	Not Allowed	Not Allowed
Read OTP Security Register	Allowed	Allowed
<b>Status Commands</b>		
Read Status Register	Allowed	Allowed
Write Status Register (All Opcodes)	Not Allowed	Not Allowed
<b>Miscellaneous Commands</b>		
Reset	Allowed	Allowed
Read Manufacturer and Device ID	Allowed	Allowed
Deep Power-Down	Not Allowed	Not Allowed
Resume from Deep Power-Down	Not Allowed	Not Allowed

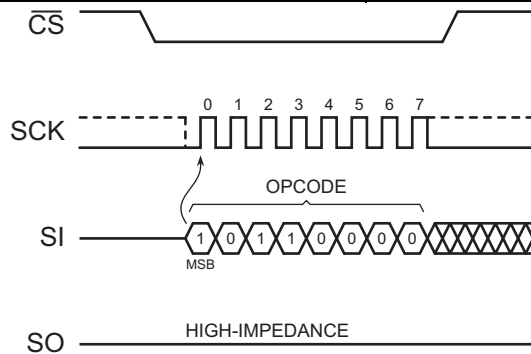


Figure 16. Program/Erase Suspend

## 8.6 Program/Erase Resume

The Program/Erase Resume command allows a suspended program or erase operation to be resumed and continue programming a Flash page or erasing a Flash memory block from where it left off. As with the Program/Erase Suspend command, the Write Enable command does not need to be issued prior to the Program/Erase Resume command being issued. Therefore, the Program/Erase Resume command operates independently of the state of the WEL bit in the Status Register.

To perform a Program/Erase Resume, the  $\overline{CS}$  pin must first be asserted and then the opcode D0h must be clocked into the device. No address bytes need to be clocked into the device, and any data clocked in after the opcode are ignored. When the  $\overline{CS}$  pin is deasserted, the program or erase operation currently suspended is resumed within a time of  $t_{RES}$ . The PS bit or the ES bit in the Status Register then be reset back to the Logical 0 state to indicate that the program or erase operation is no longer suspended. In addition, the RDY/BSY bit in the Status Register indicate that the device is busy performing a program or erase operation. The complete opcode must be clocked into the device before the  $\overline{CS}$  pin is deasserted, and the  $\overline{CS}$  pin must be deasserted on an even byte boundary (multiples of eight bits); otherwise, no resume operation is performed.

During a simultaneous Erase Suspend/Program Suspend condition, issuing the Program/Erase Resume command result in the program operation resuming first. After the program operation has been completed, the Program/Erase Resume command must be issued again in order for the erase operation to be resumed.

While the device is busy resuming a program or erase operation, any attempts at issuing the Program/Erase Suspend command are ignored. Therefore, if a resumed program or erase operation needs to be subsequently suspended again, the system must either wait the entire  $t_{RES}$  time before issuing the Program/Erase Suspend command, or it must check the status of the RDY/BSY bit or the appropriate PS or ES bit in the Status Register to determine if the previously suspended program or erase operation has resumed.

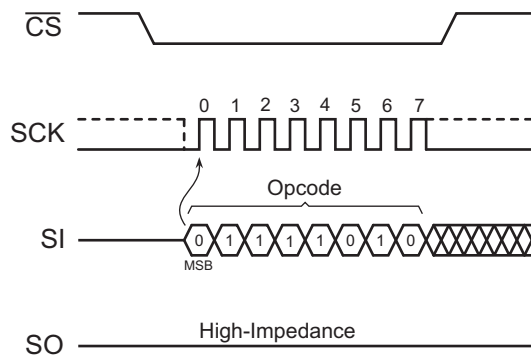


Figure 17. Program/Erase Resume



## 9. Protection Commands and Features

### 9.1 Write Enable

The Write Enable command is used to set the Write Enable Latch (WEL) bit in the Status Register to a Logical 1 state. The WEL bit must be set before a Byte/Page Program, Erase, Protect Sector, Unprotect Sector, Sector Lockdown, Freeze Sector Lockdown State, Program OTP Security Register, Write Status Register, or Write Configuration Register command can be executed. This makes the issuance of these commands a two-step process, thereby reducing the chances of a command being accidentally or erroneously executed. If the WEL bit in the Status Register is not set prior to the issuance of one of these commands, then the command is not executed.

To issue the Write Enable command, the  $\overline{CS}$  pin must first be asserted and then the opcode 06h must be clocked into the device. No address bytes need to be clocked into the device, and any data clocked in after the opcode are ignored. When the  $\overline{CS}$  pin is deasserted, the WEL bit in the Status Register is set to a Logical 1. The complete opcode must be clocked into the device before the  $\overline{CS}$  pin is deasserted, and the  $\overline{CS}$  pin must be deasserted on an even byte boundary (multiples of eight bits); otherwise, the device aborts the operation and the state of the WEL bit does not change.

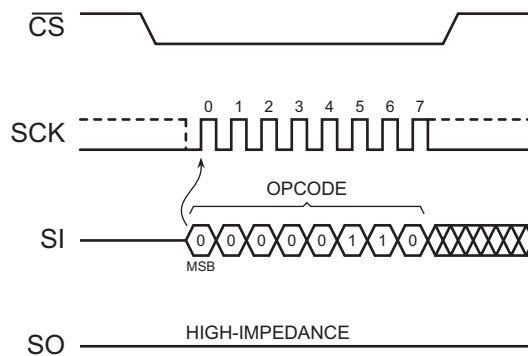


Figure 18. Write Enable

## 9.2 Write Disable

The Write Disable command is used to reset the Write Enable Latch (WEL) bit in the Status Register to the Logical 0 state. With the WEL bit reset, all Byte/Page Program, Erase, Protect Sector, Unprotect Sector, Sector Lockdown, Freeze Sector Lockdown State, Program OTP Security Register, Write Status Register, and Write Configuration Register commands are not executed. Other conditions can also cause the WEL bit to be reset. For more details, refer to the WEL bit section of the Status Register description.

To issue the Write Disable command, the  $\overline{CS}$  pin must first be asserted and then the opcode 04h must be clocked into the device. No address bytes need to be clocked into the device, and any data clocked in after the opcode are ignored. When the  $\overline{CS}$  pin is deasserted, the WEL bit in the Status Register is reset to a Logical 0. The complete opcode must be clocked into the device before the  $\overline{CS}$  pin is deasserted, and the  $\overline{CS}$  pin must be deasserted on an even byte boundary (multiples of eight bits); otherwise, the device aborts the operation and the state of the WEL bit does not change.

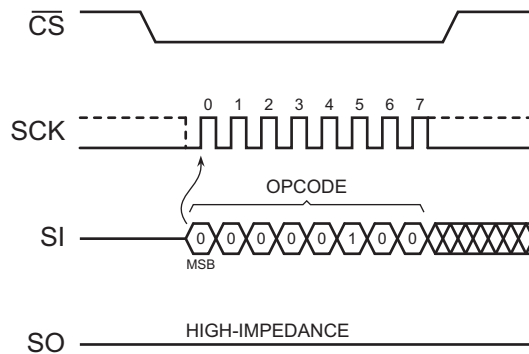


Figure 19. Write Disable

### 9.3 Protect Sector

Every physical 64 kB sector of the device has a corresponding single-bit Sector Protection Register that is used to control the software protection of a sector. Upon device power-up, each Sector Protection Register default to the Logical 1 state indicating that all sectors are protected and cannot be programmed or erased.

Issuing the Protect Sector command to a particular sector address set the corresponding Sector Protection Register to the Logical 1 state. The following table outlines the two states of the Sector Protection Registers.

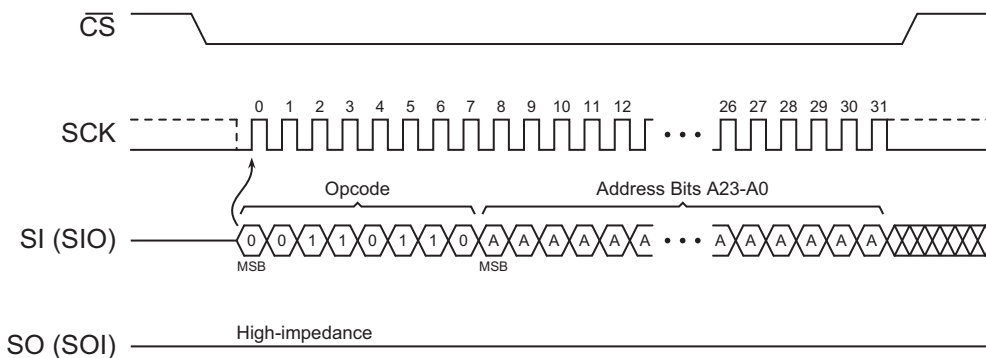
**Table 4. Sector Protection Register Values**

Value	Sector Protection Status
0	Sector is unprotected and can be programmed and erased.
1	Sector is protected and cannot be programmed or erased (the default state).

Before the Protect Sector command can be issued, the Write Enable command must have been previously issued to set the WEL bit in the Status Register to a Logical 1. To issue the Protect Sector command, the  $\overline{CS}$  pin must first be asserted, and then the opcode 36h must be clocked into the device followed by three address bytes designating any address within the sector to be protected. Any additional data clocked into the device are ignored. When the  $\overline{CS}$  pin is deasserted, the Sector Protection Register corresponding to the physical sector addressed by A23-A0 is set to the Logical 1 state and the sector itself then be protected from program and erase operations. In addition, the WEL bit in the Status Register is reset back to the Logical 0 state.

The three complete address bytes must be clocked into the device before the  $\overline{CS}$  pin is deasserted, and the  $\overline{CS}$  pin must be deasserted on an even byte boundary (multiples of eight bits); otherwise, the device abort the operation. When the device aborts the Protect Sector operation, the state of the Sector Protection Register is unchanged, and the WEL bit in the Status Register is reset to a Logical 0.

As a safeguard against accidental or erroneous protecting or unprotecting of sectors, the Sector Protection Registers can themselves be locked from updates by using the SPRL (Sector Protection Registers Locked) bit of the Status Register (see Section 11, Status Register Commands, for more details). If the Sector Protection Registers are locked, then any attempts to issue the Protect Sector command are ignored, and the device reset the WEL bit in the Status Register back to a Logical 0 and return to the idle state once the  $\overline{CS}$  pin has been deasserted.



**Figure 20. Protect Sector**

## 9.4 Unprotect Sector

Issuing the Unprotect Sector command to a particular sector address reset the corresponding Sector Protection Register to the Logical 0 state (see Table 4 for Sector Protection Register values). Every physical sector of the device has a corresponding single-bit Sector Protection Register that is used to control the software protection of a sector.

Before the Unprotect Sector command can be issued, the Write Enable command must have been previously issued to set the WEL bit in the Status Register to a Logical 1. To issue the Unprotect Sector command, the  $\overline{CS}$  pin must first be asserted and then the opcode 39h must be clocked into the device. After the opcode has been clocked in, the three address bytes designating any address within the sector to be unprotected must be clocked in. Any additional data clocked into the device after the address bytes are ignored. When the  $\overline{CS}$  pin is deasserted, the Sector Protection Register corresponding to the sector addressed by A23-A0 is reset to the Logical 0 state and the sector itself is unprotected. In addition, the WEL bit in the Status Register is reset back to the Logical 0 state.

The three complete address bytes must be clocked into the device before the  $\overline{CS}$  pin is deasserted, and the  $\overline{CS}$  pin must be deasserted on an even byte boundary (multiples of eight bits); otherwise, the device abort the operation, the state of the Sector Protection Register is unchanged, and the WEL bit in the Status Register is reset to a Logical 0.

As a safeguard against accidental or erroneous locking or unlocking of sectors, the Sector Protection Registers can themselves be locked from updates by using the SPRL (Sector Protection Registers Locked) bit of the Status Register (see Section 11, Status Register Commands, for more details). If the Sector Protection Registers are locked, then any attempts to issue the Unprotect Sector command are ignored, and the device reset the WEL bit in the Status Register back to a Logical 0 and return to the idle state once the  $\overline{CS}$  pin has been deasserted.

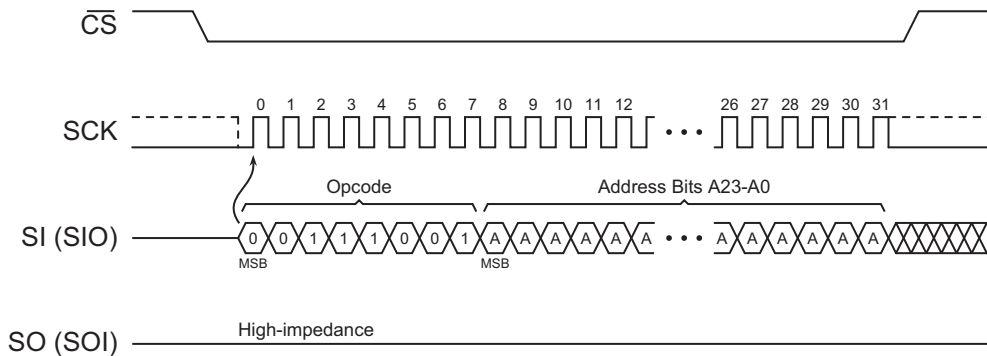


Figure 21. Unprotect Sector

## 9.5 Global Protect/Unprotect

The Global Protect and Global Unprotect features can work in conjunction with the Protect Sector and Unprotect Sector functions.

**Example:** A system can globally protect the entire memory array and then use the Unprotect Sector command to individually unprotect certain sectors and individually reprotect them later by using the Protect Sector command. Likewise, a system can globally unprotect the entire memory array and then individually protect certain sectors as needed.

Performing a Global Protect or Global Unprotect is accomplished by writing a certain combination of data to the Status Register using the Write Status Register Byte 1 command (see [“Write Status Register Byte 1” on page 44](#) for command execution details). The Write Status Register command is also used to modify the SPRL (Sector Protection Registers Locked) bit to control hardware and software locking.

To perform a Global Protect, the appropriate  $\overline{WP}$  pin and SPRL conditions must be met, and the system must write a Logical 1 to bits 5, 4, 3, and 2 of the first byte of the Status Register. Conversely, to perform a Global Unprotect, the same  $\overline{WP}$  and SPRL conditions must be met, but the system must write a Logical 0 to bits 5, 4, 3, and 2 of the first byte of the Status Register. [Table 5](#) details the conditions necessary for a Global Protect or Global Unprotect to be performed.

Sectors that have been erase or program suspended must remain in the unprotected state. If a Global Protect operation is attempted while a Sector is Erase or program suspended, the Protection operation abort, the protection states of all sectors in the Flash memory array does not change, and the WEL bit in the Status Register is reset back to a Logical 0.

Essentially, if the SPRL bit of the Status Register is in the Logical 0 state (Sector Protection Registers are not locked), then writing a 00h to the first byte of the Status Register perform a Global Unprotect without changing the state of the SPRL bit. Similarly, writing a 7Fh to the first byte of the Status Register perform a Global Protect and keep the SPRL bit in the Logical 0 state. The SPRL bit can, of course, be changed to a Logical 1 by writing an FFh if software-locking or hardware-locking is desired along with the Global Protect.

If the desire is to only change the SPRL bit without performing a Global Protect or Global Unprotect, then the system can simply write a 0Fh to the first byte of the Status Register to change the SPRL bit from a Logical 1 to a Logical 0, provided the  $\overline{WP}$  pin is deasserted. Likewise, the system can write an F0h to change the SPRL bit from a Logical 0 to a Logical 1 without affecting the current sector protection status (no changes are made to the Sector Protection Registers).

When writing to the first byte of the Status Register, bits 5, 4, 3, and 2 are not actually modified, but are decoded by the device for the purposes of the Global Protect and Global Unprotect functions. Only bit 7, the SPRL bit, actually be modified. Thus, when reading the first byte of the Status Register, bits 5, 4, 3, and 2 do not reflect the values written to them, but instead indicate the status of the  $\overline{WP}$  pin and the sector protection status. See the [“Read Status Register” on page 40](#) and [Table 12 on page 40](#) for details on the Status Register format and what values can be read for bits 5, 4, 3, and 2.

Table 5. Valid SPRL and Global Protect/Unprotect Conditions

$\overline{WP}$ State	Current SPRL Value	New Write Status Register Byte 1 data	Protection Operation	New SPRL Value
		Bit 7 6 5 4 3 2 1 0		
0	0	0 x 0 0 0 0 x x	Global Unprotect – all Sector Protection Registers reset to 0	0
		0 x 0 0 0 1 x x	No change to current protection	0
		?	No change to current protection	0
		0 x 1 1 1 0 x x	No change to current protection	0
		0 x 1 1 1 1 x x	Global Protect – all Sector Protection Registers set to 1	0
		1 x 0 0 0 0 x x	Global Unprotect – all Sector Protection Registers reset to 0	1
		1 x 0 0 0 1 x x	No change to current protection	1
		?	No change to current protection	1
1 x 1 1 1 0 x x	No change to current protection	1		
1 x 1 1 1 1 x x	Global Protect – all Sector Protection Registers set to 1	1		
0	1	x x x x x x x x	No change to the current protection level. All sectors currently protected remain protected and all sectors currently unprotected remain unprotected.  The Sector Protection Registers are hard-locked and cannot be changed when the $\overline{WP}$ pin is low and the current state of SPRL is 1. Therefore, a Global Protect/Unprotect does not occur. In addition, the SPRL bit cannot be changed (the $\overline{WP}$ pin must be high in order to change SPRL back to a 0).	
1	0	0 x 0 0 0 0 x x	Global Unprotect – all Sector Protection Registers reset to 0	0
		0 x 0 0 0 1 x x	No change to current protection	0
		?	No change to current protection	0
		0 x 1 1 1 0 x x	No change to current protection	0
		0 x 1 1 1 1 x x	Global Protect – all Sector Protection Registers set to 1	0
		1 x 0 0 0 0 x x	Global Unprotect – all Sector Protection Registers reset to 0	1
		1 x 0 0 0 1 x x	No change to current protection	1
		?	No change to current protection	1
1 x 1 1 1 0 x x	No change to current protection	1		
1 x 1 1 1 1 x x	Global Protect – all Sector Protection Registers set to 1	1		
1	1	0 x 0 0 0 0 x x	No change to the current protection level. All sectors currently protected remain protected and all sectors currently unprotected remain unprotected.	0
		0 x 0 0 0 1 x x		0
		?		0
		0 x 1 1 1 0 x x		0
		0 x 1 1 1 1 x x		0
		1 x 0 0 0 0 x x	The Sector Protection Registers are soft-locked and cannot be changed when the current state of SPRL is 1. Therefore, a Global Protect/Unprotect does not occur. However, the SPRL bit can be changed back to a 0 from a 1 since the $\overline{WP}$ pin is high. To perform a Global Protect/Unprotect, the Write Status Register command must be issued again after the SPRL bit has been changed from 1 to 0.	1
		1 x 0 0 0 1 x x		1
		?		1
1 x 1 1 1 0 x x		1		
1 x 1 1 1 1 x x		1		

## 9.6 Read Sector Protection Registers

The Sector Protection Registers can be read to determine the current software protection status of each sector. Reading the Sector Protection Registers, however, does not determine the status of the  $\overline{WP}$  pin.

To read the Sector Protection Register for a particular sector, the  $\overline{CS}$  pin must first be asserted and then the opcode 3Ch must be clocked in. Once the opcode has been clocked in, three address bytes designating any address within the sector must be clocked in. After the last address byte has been clocked in, the device begins outputting data on the SO pin during every subsequent clock cycle. The data being output are a repeating byte of either FFh or 00h to denote the value of the appropriate Sector Protection Register.

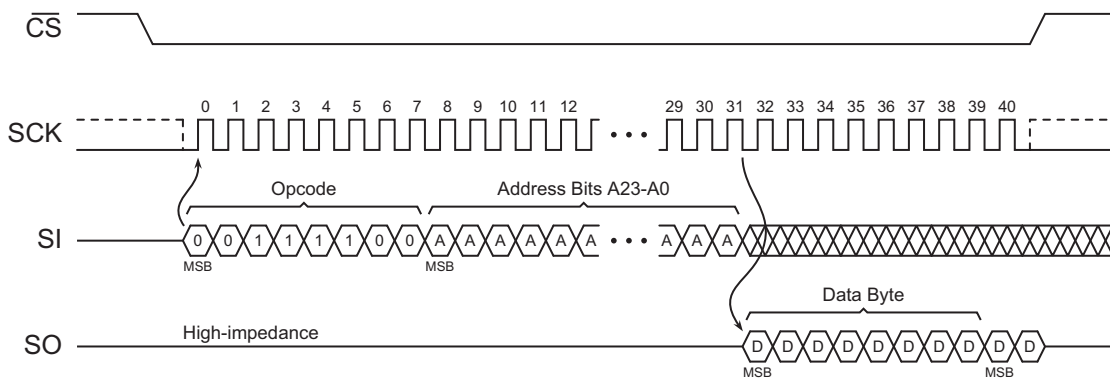
At clock frequencies above  $f_{CLK}$ , the first byte of data output is not valid. Therefore, if operating at clock frequencies above  $f_{CLK}$ , at least two bytes of data must be clocked out from the device in order to determine the correct status of the appropriate Sector Protection Register.

**Table 6. Read Sector Protection Register – Output Data**

Output Data	Sector Protection Register Value
00h	Sector Protection Register value is 0 (sector is unprotected).
FFh	Sector Protection Register value is 1 (sector is protected).

Deasserting the  $\overline{CS}$  pin terminates the read operation and put the SO pin into a high-impedance state. The  $\overline{CS}$  pin can be deasserted at any time and does not require that a full byte of data be read.

In addition to reading the individual Sector Protection Registers, the Software Protection Status (SWP) bits in the Status Register can be read to determine if all, some, or none of the sectors are software protected (refer to “[Read Status Register](#)” on page 40 for more details).



**Figure 22. Read Sector Protection Register**

## 9.7 Protected States and the Write Protect ( $\overline{WP}$ ) Pin

The  $\overline{WP}$  pin is not linked to the memory array itself and has no direct effect on the protection status or lockdown status of the memory array. Instead, the  $\overline{WP}$  pin, in conjunction with the SPRL (Sector Protection Registers Locked) bit in the Status Register, is used to control the hardware locking mechanism of the device. For hardware locking to be active, two conditions must be met: the  $\overline{WP}$  pin must be asserted and the SPRL bit must be in the Logical 1 state.

When hardware locking is active, the Sector Protection Registers are locked and the SPRL bit itself is also locked. Therefore, sectors that are protected are locked in the protected state and sectors that are unprotected are locked in the unprotected state. These states cannot be changed as long as hardware locking is active, so the Protect Sector, Unprotect Sector, and Write Status Register commands are ignored. In order to modify the protection status of a sector, the  $\overline{WP}$  pin must first be deasserted, and the SPRL bit in the Status Register must be reset back to the Logical 0 state using the Write Status Register command. When resetting the SPRL bit back to a Logical 0, it is not possible to perform a Global Protect or Global Unprotect at the same time because the Sector Protection Registers remain soft-locked until after the Write Status Register command has been executed.

If the  $\overline{WP}$  pin is permanently connected to GND, then once the SPRL bit is set to a Logical 1, the only way to reset the bit back to the Logical 0 state is to power-cycle the device. This allows a system to power up with all sectors software protected but not hardware locked. Therefore, sectors can be unprotected and protected as needed and then hardware locked at a later time by simply setting the SPRL bit in the Status Register.

When the  $\overline{WP}$  pin is deasserted, or if the  $\overline{WP}$  pin is permanently connected to  $V_{CC}$ , the SPRL bit in the Status Register can still be set to a Logical 1 to lock the Sector Protection Registers. This provides a software locking ability to prevent erroneous Protect Sector or Unprotect Sector commands from being processed. When changing the SPRL bit to a Logical 1 from a Logical 0, it is also possible to perform a Global Protect or Global Unprotect at the same time by writing the appropriate values into bits 5, 4, 3, and 2 of the first byte of the Status Register.

Tables 7 and 8 detail the various protection and locking states of the device.

**Table 7. Sector Protection Register States**

$\overline{WP}$	Sector Protection Register n[1]	Sector n[1]
X (Don't Care)	0	Unprotected
	1	Protected

Notes:

1. "n" represents a sector number.

**Table 8. Hardware and Software Locking**

$\overline{WP}$	SPRL	Locking	SPRL Change Allowed	Sector Protection Registers
0	0		Can be modified from 0 to 1	Unlocked and modifiable using the Protect and Unprotect Sector commands. Global Protect and Unprotect can also be performed.
0	1	Hardware locked	Locked	Locked in current state. Protect and Unprotect Sector commands are ignored. Global Protect and Unprotect cannot be performed.
1	0		Can be modified from 0 to 1	Unlocked and modifiable using the Protect and Unprotect Sector commands. Global Protect and Unprotect can also be performed.
1	1	Software locked	Can be modified from 1 to 0	Locked in current state. Protect and Unprotect Sector commands are ignored. Global Protect and Unprotect cannot be performed.



## 10. Security Commands

### 10.1 Sector Lockdown

Certain applications require that portions of the Flash memory array be permanently protected against malicious attempts at altering program code, data modules, security information or encryption/decryption algorithms, keys, and routines. To address these applications, the device incorporates a sector lockdown mechanism that allows any combination of individual 64 kB sectors to be permanently locked so that they become read-only. Once a sector is locked down, it can never be erased or programmed again, and it can never be unlocked from the locked-down state.

Each 64 kB physical sector has a corresponding single-bit Sector Lockdown Register that is used to control the lockdown status of that sector. These registers are nonvolatile and retain their state even after a device power cycle or Reset operation. The following table outlines the two states of the Sector Lockdown Registers.

**Table 9. Sector Lockdown Register Values**

Value	Sector Lockdown Status
0	Sector is not locked down and can be programmed and erased (the default state).
1	Sector is permanently locked down and can never be programmed or erased again.

Issuing the Sector Lockdown command to a particular sector address sets the corresponding Sector Lockdown Register to the Logical 1 state. Each Sector Lockdown Register can only be set once; therefore, once set to the Logical 1 state, a Sector Lockdown Register cannot be reset back to the Logical 0 state.

Before the Sector Lockdown command can be issued, the Write Enable command must have been previously issued to set the WEL bit in the Status Register to a Logical 1. In addition, the Sector Lockdown Enabled (SLE) bit in the Status Register must have also been previously set to the Logical 1 state by using the Write Status Register Byte 2 command (see [“Write Status Register Byte 2”](#) on page 45). To issue the Sector Lockdown command, the  $\overline{CS}$  pin must first be asserted and then the opcode 33h must be clocked into the device followed by three address bytes designating any address within the 64 kB sector to be locked down. After the three address bytes have been clocked in, a confirmation byte of D0h must also be clocked in immediately following the three address bytes. Any additional data clocked into the device after the first byte of data are ignored. When the  $\overline{CS}$  pin is deasserted, the Sector Lockdown Register corresponding to the sector addressed by A23-A0 is set to the Logical 1 state, and the sector itself is then permanently locked down from program and erase operations within a time of  $t_{LOCK}$ . In addition, the WEL bit in the Status Register is reset back to the Logical 0 state.

The three complete address bytes and the correct confirmation byte value of D0h must be clocked into the device before the  $\overline{CS}$  pin is deasserted, and the  $\overline{CS}$  pin must be deasserted on an even byte boundary (multiples of eight bits); otherwise, the device aborts the operation. When the device aborts the Sector Lockdown operation, the state of the corresponding Sector Lockdown Register, as well as the SLE bit in the Status Register, are unchanged; however, the WEL bit in the Status Register is reset to a Logical 0.

As a safeguard against accidental or erroneous locking down of sectors, the Sector Lockdown command can be enabled and disabled as needed by using the SLE bit in the Status Register. In addition, the current sector lockdown state can be frozen so that no further modifications to the Sector Lockdown Registers can be made (see [“Freeze Sector Lockdown State”](#) on page 35). If the Sector Lockdown command is disabled, or if the sector lockdown state is frozen, then any attempts to issue the Sector Lockdown command are ignored and the device resets the WEL bit in the Status Register back to a Logical 0 and return to the idle state once the  $\overline{CS}$  pin has been deasserted.

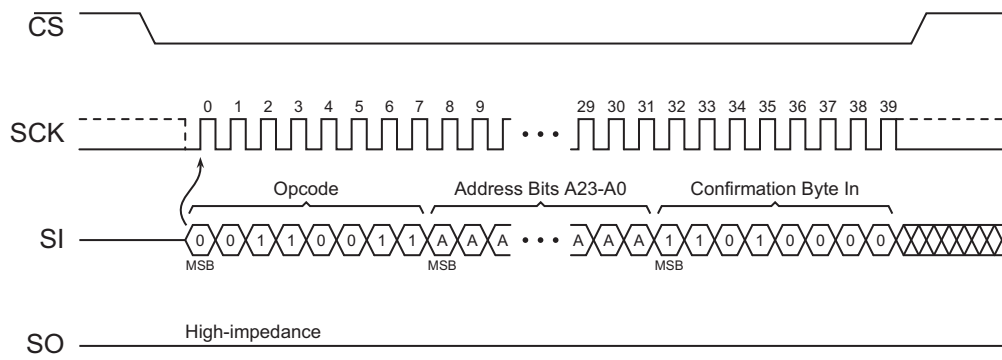


Figure 23. Sector Lockdown

## 10.2 Freeze Sector Lockdown State

The current sector lockdown state can be permanently frozen so that no further modifications to the Sector Lockdown Registers can be made; therefore, the Sector Lockdown command is permanently disabled and no additional sectors can be locked down aside from those already locked down. Any attempts to issue the Sector Lockdown command after the sector lockdown state has been frozen are ignored.

Before the Freeze Sector Lockdown State command can be issued, the Write Enable command must have been previously issued to set the WEL bit in the Status Register to a Logical 1. In addition, the Sector Lockdown Enabled (SLE) bit in the Status Register must have also been previously set to the Logical 1 state. To issue the Freeze Sector Lockdown State command, the  $\overline{CS}$  pin must first be asserted and then the opcode 34h must be clocked into the device, followed by three command-specific address bytes of 55AA40h. After the three address bytes have been clocked in, a confirmation byte of D0h must be clocked in immediately following the three address bytes. Any additional data clocked into the device are ignored. When the  $\overline{CS}$  pin is deasserted, the current sector lockdown state is permanently frozen within a time of  $t_{LOCK}$ . In addition, the WEL bit in the Status Register is reset back to the Logical 0 state, and the SLE bit is permanently reset to a Logical 0 to indicate that the Sector Lockdown command is permanently disabled.

The three complete and correct address bytes and the confirmation byte must be clocked into the device before the  $\overline{CS}$  pin is deasserted, and the  $\overline{CS}$  pin must be deasserted on an even byte boundary (multiples of eight bits); otherwise, the device aborts the operation. When the device aborts the Freeze Sector Lockdown State operation, the WEL bit in the Status Register is reset to a Logical 0; however, the state of the SLE bit is unchanged.

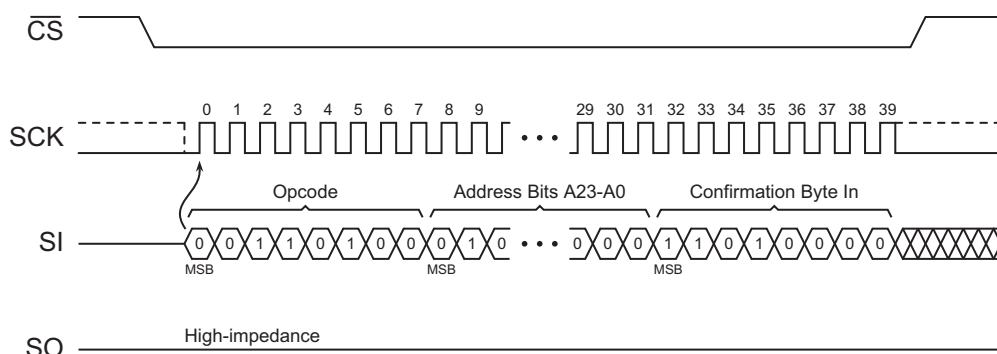


Figure 24. Freeze Sector Lockdown State

### 10.3 Read Sector Lockdown Registers

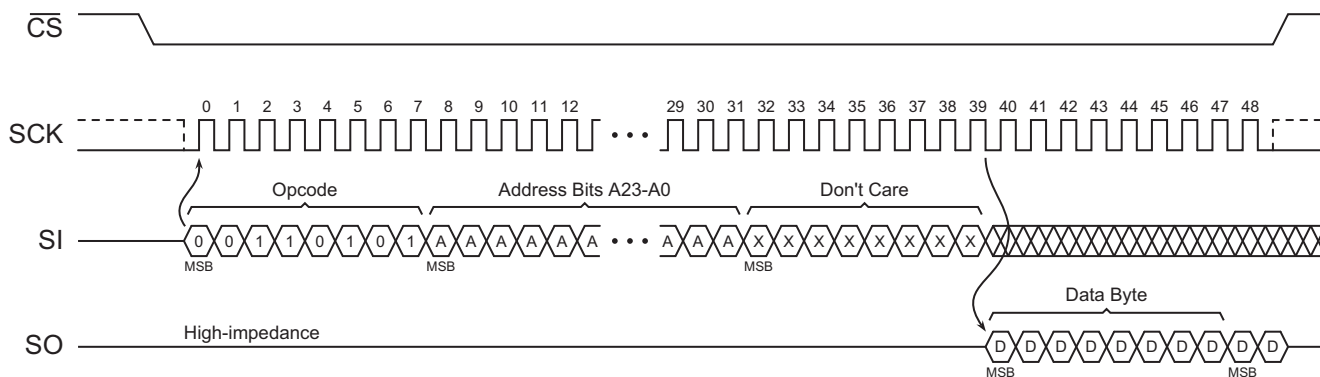
The Sector Lockdown Registers can be read to determine the current lockdown status of each physical 64 kB sector. To read the Sector Lockdown Register for a particular 64 kB sector, the  $\overline{CS}$  pin must first be asserted and then the opcode 35h must be clocked in. Once the opcode has been clocked in, three address bytes designating any address within the 64 kB sector must be clocked in. After the address bytes have been clocked in, data are output on the SO pin during every subsequent clock cycle. The data being output are a repeating byte of either FFh or 00h to denote the value of the appropriate Sector Lockdown Register.

At clock frequencies above  $f_{CLK}$ , the first byte of data output is not valid. Therefore, if operating at clock frequencies above  $f_{CLK}$ , at least two bytes of data must be clocked out from the device in order to determine the correct status of the appropriate Sector Lockdown Register.

**Table 10. Read Sector Lockdown Register – Output Data**

Output Data	Sector Lockdown Register Value
00h	Sector Lockdown Register value is 0 (sector is not locked down).
FFh	Sector Lockdown Register value is 1 (sector is permanently locked down).

Deasserting the  $\overline{CS}$  pin terminates the read operation and put the SO pin into a high-impedance state. The  $\overline{CS}$  pin can be deasserted at any time and does not require that a full byte of data be read.



**Figure 25. Read Sector Lockdown Register**

## 10.4 Program OTP Security Register

The device contains a specialized OTP (One-Time Programmable) Security Register that can be used for purposes such as unique device serialization, system-level Electronic Serial Number (ESN) storage, locked key storage, etc. The OTP Security Register is independent of the main Flash memory array and is comprised of a total of 128 bytes of memory divided into two portions. The first 64 bytes (byte locations 0 through 63) of the OTP Security Register are allocated as a one-time user-programmable space. Once these 64 bytes have been programmed, they cannot be erased or reprogrammed. The remaining 64 bytes of the OTP Security Register (byte locations 64 through 127) are factory programmed by Renesas Electronics and contains a unique value for each device. The factory programmed data is fixed and cannot be changed.

**Table 11. OTP Security Register**

Security Register Byte Number									
0	1	...	62	63	64	65	...	126	127
One-Time User Programmable					Renesas Electronics Factory Programmed				

The user-programmable portion of the OTP Security Register does not need to be erased before it is programmed. In addition, the Program OTP Security Register command operates on the entire 64-byte, user-programmable portion of the OTP Security Register at one time. Once the user-programmable space has been programmed with any number of bytes, the user-programmable space cannot be programmed again. Therefore, it is not possible to program only the first two bytes of the register and then program the remaining 62 bytes at a later time.

Before the Program OTP Security Register command can be issued, the Write Enable command must have been previously issued to set the WEL bit in the Status Register to a Logical 1. To program the OTP Security Register, the  $\overline{CS}$  pin must first be asserted and then the opcode 9Bh must be clocked into the device, followed by the three address bytes denoting the location of the first byte of the OTP Security Register to begin programming at. Since the size of the user-programmable portion of the OTP Security Register is 64 bytes, the upper order address bits do not need to be decoded by the device. Therefore, address bits A23-A6 are ignored by the device and their values can be either a Logical 1 or 0. After the address bytes have been clocked in, data can then be clocked into the device and stored in the internal buffer.

If the starting memory address denoted by A23-A0 does not start at the beginning of the OTP Security Register memory space (A5-A0 are not all 0), then special circumstances regarding which OTP Security Register locations are to be programmed applies. In this situation, any data sent to the device that goes beyond the end of the 64-byte user-programmable space wraps around back to the beginning of the OTP Security Register. In addition, if more than 64 bytes of data are sent to the device, then only the last 64 bytes sent are latched into the internal buffer.

**Example:** If the starting address denoted by A23-A0 is 00003Eh, and three bytes of data are sent to the device, then the first two bytes of data are programmed at OTP Security Register addresses 00003Eh and 00003Fh while the last byte of data is programmed at address 000000h. The remaining bytes in the OTP Security Register (addresses 000001h through 00003Dh) are not programmed and remain in the erased state (FFh).

When the  $\overline{CS}$  pin is deasserted, the device takes the data stored in the internal buffer and program it into the appropriate OTP Security Register locations based on the starting address specified by A23-A0 and the number of data bytes sent to the device. If fewer than 64 bytes of data are sent to the device, then the remaining bytes within the OTP Security Register are not programmed and remain in the erased state (FFh). The programming of the data bytes is internally self-timed takes place in a time of  $t_{OTP}$ . It is not possible to suspend the programming of the OTP Security Register.

The three address bytes and at least one complete byte of data must be clocked into the device before the  $\overline{CS}$  pin is deasserted, and the  $\overline{CS}$  pin must be deasserted on even byte boundaries (multiples of eight bits); otherwise, the device aborts the operation and the user-programmable portion of the OTP Security Register is not programmed. The WEL bit in the Status Register is reset back to the Logical 0 state if the OTP Security Register program cycle

aborts due to an incomplete address being sent, an incomplete byte of data being sent, the  $\overline{CS}$  pin being deasserted on uneven byte boundaries, or because the user-programmable portion of the OTP Security Register was previously programmed.

While the device is programming the OTP Security Register, the Status Register can be read and indicates that the device is busy. For faster throughput, it is recommended that the Status Register be polled rather than waiting the  $t_{OTP}$  time to determine if the data bytes have finished programming. At some point before the OTP Security Register programming completes, the WEL bit in the Status Register is reset back to the Logical 0 state.

If the device is powered down during the OTP Security Register program cycle, then the contents of the 64-byte, user-programmable portion of the OTP Security Register cannot be guaranteed and cannot be programmed again.

The Program OTP Security Register command utilizes the 256-byte internal buffer for processing. Therefore, the contents of the buffer is altered from its previous state when this command is issued.

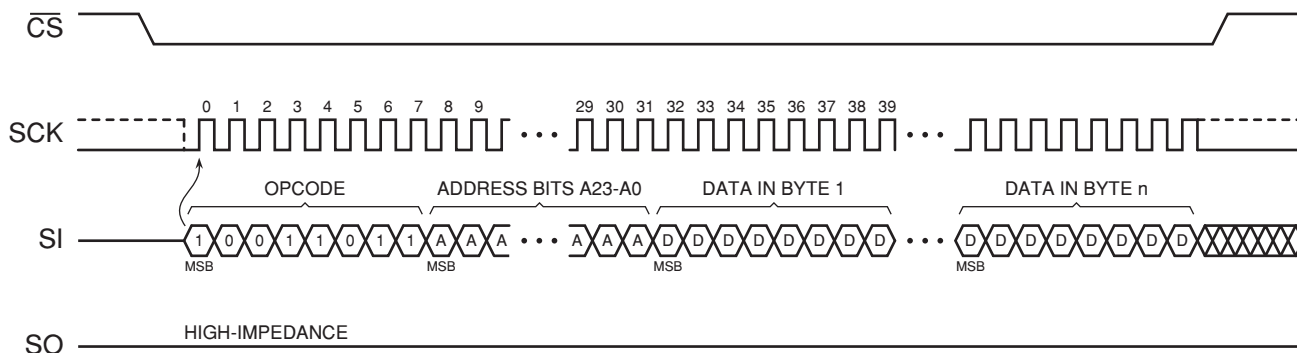


Figure 26. Program OTP Security Register

## 10.5 Read OTP Security Register

The OTP Security Register can be sequentially read in a similar fashion to the Read Array operation up to the maximum clock frequency specified by  $f_{MAX}$ . To read the OTP Security Register, the  $\overline{CS}$  pin must first be asserted and then the opcode 77h must be clocked into the device. After the opcode has been clocked in, the three address bytes must be clocked in to specify the starting address location of the first byte to read within the OTP Security Register. Following the three address bytes, two dummy bytes must be clocked into the device before data can be output.

After the three address bytes and the dummy bytes have been clocked in, additional clock cycles result in OTP Security Register data being output on the SO pin. When the last byte (00007Fh) of the OTP Security Register has been read, the device continues reading from the beginning of the register (000000h). No delays are incurred when wrapping around from the end of the register to the beginning of the register.

Deasserting the  $\overline{CS}$  pin terminates the read operation and put the SO pin into a high-impedance state. The  $\overline{CS}$  pin can be deasserted at any time and does not require that a full byte of data be read.

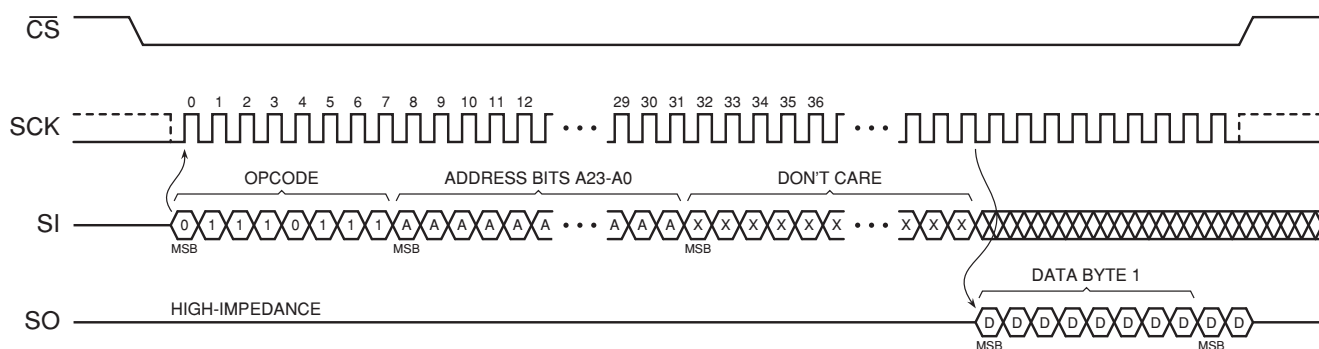


Figure 27. Read OTP Security Register

## 11. Status Register Commands

### 11.1 Read Status Register

The two-byte Status Register can be read to determine the device's ready/busy status, as well as the status of many other functions such as hardware locking and software protection. The Status Register can be read at any time, including during an internally self-timed program or erase operation.

To read the Status Register, the  $\overline{CS}$  pin must first be asserted and then the opcode 05h must be clocked into the device. After the opcode has been clocked in, the device begins outputting Status Register data on the SO pin during every subsequent clock cycle. After the second byte of the Status Register has been clocked out, the sequence repeats itself, starting again with the first byte of the Status Register, as long as the  $\overline{CS}$  pin remains asserted and the clock pin is being pulsed. The data in the Status Register is constantly being updated, so each repeating sequence can output new data. The RDY/BSY status is available for both bytes of the Status Register and is updated for each byte.

At clock frequencies above  $f_{CLK}$ , the first two bytes of data output from the Status Register are not valid.

Therefore, if operating at clock frequencies above  $f_{CLK}$ , at least four bytes of data must be clocked out from the device in order to read the correct values of both bytes of the Status Register.

Deasserting the  $\overline{CS}$  pin terminates the Read Status Register operation and put the SO pin into a high-impedance state. The  $\overline{CS}$  pin can be deasserted at any time and does not require that a full byte of data be read.

**Table 12. Status Register Format – Byte 1**

Bit <sup>[1]</sup>	Name		Type <sup>[2]</sup>	Description	
7	SPRL	Sector Protection Registers Locked	R/W	0	Sector Protection Registers are unlocked (default)
				1	Sector Protection Registers are locked
6	RES	Reserved for future use	R	0	Reserved for future use
5	EPE	Erase/Program Error	R	0	Erase or program operation was successful
				1	Erase or program error detected
4	WPP	Write Protect ( $\overline{WP}$ ) Pin Status	R	0	$\overline{WP}$ is asserted
				1	$\overline{WP}$ is deasserted
3:2	SWP	Software Protection Status	R	00	All sectors are software unprotected (all Sector Protection Registers are 0)
				01	Some sectors are software protected. Read individual Sector Protection Registers to determine which sectors are protected.
				10	Reserved for future use
				11	All sectors are software protected (all Sector Protection Registers are 1 – default)
1	WEL	Write Enable Latch Status	R	0	Device is not Write Enabled (default)
				1	Device is Write Enabled
0	RDY/BSY	Ready/Busy Status	R	0	Device is ready
				1	Device is busy with an internal operation

1. Only bit 7 of Status Register Byte 1 is modified when using the Write Status Register Byte 1 command.
2. R/W = Readable and Writeable  
R = Readable only



Table 13. Status Register Format – Byte 2

Bit <sup>[1]</sup>	Name		Type <sup>[2]</sup>	Description	
7	RES	Reserved for future use	R	0	Reserved for future use
6	RES	Reserved for future use	R	0	Reserved for future use
5	RES	Reserved for future use	R	0	Reserved for future use
4	RSTE	Reset Enabled	R/W	0	Reset command is disabled (default)
				1	Reset command is enabled
3	SLE	Sector Lockdown Enabled	R/W	0	Sector Lockdown and Freeze Sector Lockdown State commands are disabled (default)
				1	Sector Lockdown and Freeze Sector Lockdown State commands are enabled
2	PS	Program Suspend Status	R	0	No sectors are program suspended (default)
				1	A sector is program suspended
1	ES	Erase Suspend Status	R	0	No sectors are erase suspended (default)
				1	A sector is erase suspended
0	RDY/BSY	Ready/Busy Status	R	0	Device is ready
				1	Device is busy with an internal operation

1. Only bits 4 and 3 of Status Register Byte 2 are modified when using the Write Status Register Byte 2 command.
2. R/W = Readable and Writeable  
R = Readable only

### 11.1.1 SPRL Bit

The SPRL bit is used to control whether the Sector Protection Registers can be modified or not. When the SPRL bit is in the Logical 1 state, all Sector Protection Registers are locked and cannot be modified with the Protect Sector and Unprotect Sector commands (the device ignores these commands). In addition, the Global Protect and Global Unprotect features cannot be performed. Any sectors that are presently protected remain protected and any sectors that are presently unprotected remain unprotected.

When the SPRL bit is in the Logical 0 state, all Sector Protection Registers are unlocked and can be modified (the Protect Sector and Unprotect Sector commands, as well as the Global Protect and Global Unprotect features, are processed as normal). The SPRL bit defaults to the Logical 0 state after device power-up. The Reset command has no effect on the SPRL bit.

The SPRL bit can be modified freely whenever the  $\overline{WP}$  pin is deasserted. However, if the  $\overline{WP}$  pin is asserted, then the SPRL bit can only be changed from a Logical 0 (Sector Protection Registers are unlocked) to a Logical 1 (Sector Protection Registers are locked). In order to reset the SPRL bit back to a Logical 0 using the Write Status Register Byte 1 command, the  $\overline{WP}$  pin has to first be deasserted.

The SPRL bit is the only bit of Status Register Byte 1 that can be user modified via the Write Status Register Byte 1 command.

### 11.1.2 EPE Bit

The EPE bit indicates whether the last erase or program operation completed successfully or not. If at least one byte during the erase or program operation did not erase or program properly, then the EPE bit is set to the Logical 1 state. The EPE bit is not set if an erase or program operation aborts for any reason such as an attempt to erase or program a protected region or a locked down sector, an attempt to erase or program a suspended sector, or if the WEL bit is not set prior to an erase or program operation. The EPE bit is updated after every erase and program operation.

### 11.1.3 WPP Bit

The WPP bit can be read to determine if the  $\overline{WP}$  pin has been asserted or not.

### 11.1.4 SWP Bits

The SWP bits provide feedback on the software protection status for the device. There are three possible combinations of the SWP bits that indicate whether none, some, or all of the sectors have been protected using the Protect Sector command or the Global Protect feature. If the SWP bits indicate that some of the sectors have been protected, then the individual Sector Protection Registers can be read with the Read Sector Protection Registers command to determine which sectors are in fact protected.

### 11.1.5 WEL Bit

The WEL bit indicates the current status of the internal Write Enable Latch. When the WEL bit is in the Logical 0 state, the device does not accept any Byte/Page Program, Erase, Protect Sector, Unprotect Sector, Sector Lockdown, Freeze Sector Lockdown State, Program OTP Security Register, Write Status Register, or Write Configuration Register commands. The WEL bit defaults to the Logical 0 state after a device Power-up or Reset operation. In addition, the WEL bit is reset to the Logical 0 state automatically under the following conditions:

- Write Disable operation completes successfully
- Write Status Register operation completes successfully or aborts
- Write Configuration Register operation completes successfully or aborts
- Protect Sector operation completes successfully or aborts
- Unprotect Sector operation completes successfully or aborts
- Sector Lockdown operation completes successfully or aborts
- Freeze Sector Lockdown State operation completes successfully or aborts
- Program OTP Security Register operation completes successfully or aborts
- Byte/Page Program operation completes successfully or aborts
- Block Erase operation completes successfully or aborts
- Chip Erase operation completes successfully or aborts
- Hold condition aborts

If the WEL bit is in the Logical 1 state, it is not reset to a Logical 0 if an operation aborts due to an incomplete or unrecognized opcode being clocked into the device before the  $\overline{CS}$  pin is deasserted. In order for the WEL bit to be reset when an operation aborts prematurely, the entire opcode for a Byte/Page Program, Erase, Protect Sector, Unprotect Sector, Sector Lockdown, Freeze Sector Lockdown State, Program OTP Security Register, Write Status Register, or Write Configuration Register command must have been clocked into the device.

### 11.1.6 RSTE Bit

The RSTE bit is used to enable or disable the Reset command. When the RSTE bit is in the Logical 0 state (the default state after power-up), the Reset command is disabled and any attempts to reset the device using the Reset command are ignored. When the RSTE bit is in the Logical 1 state, the Reset command is enabled.

The RSTE bit retains its state as long as power is applied to the device. Once set to the Logical 1 state, the RSTE bit remains in that state until it is modified using the Write Status Register Byte 2 command or until the device has been power cycled. The Reset command itself does not change the state of the RSTE bit.

### 11.1.7 SLE Bit

The SLE bit is used to enable and disable the Sector Lockdown and Freeze Sector Lockdown State commands. When the SLE bit is in the Logical 0 state (the default state after power-up), the Sector Lockdown and Freeze Sector Lockdown commands are disabled. If the Sector Lockdown and Freeze Sector Lockdown commands are disabled, then any attempts to issue the commands are ignored. This provides a safeguard for these commands against accidental or erroneous execution. When the SLE bit is in the Logical 1 state, the Sector Lockdown and Freeze Sector Lockdown State commands are enabled.

Unlike the WEL bit, the SLE bit does not automatically reset after certain device operations. Therefore, once set, the SLE bit remains in the Logical 1 state until it is modified using the Write Status Register Byte 2 command or until the device has been power cycled. The Reset command has no effect on the SLE bit.

If the Freeze Sector Lockdown State command has been issued, then the SLE bit is permanently reset in the Logical 0 state to indicate that the Sector Lockdown command has been disabled.

### 11.1.8 PS Bit

The PS bit indicates whether or not a sector is in the Program Suspend state.

### 11.1.9 ES Bit

The ES bit indicates whether or not a sector is in the Erase Suspend state.

### 11.1.10 RDY/BSY Bit

The RDY/BSY bit is used to determine whether or not an internal operation, such as a program or erase, is in progress. To poll the RDY/BSY bit to detect the completion of a program or erase cycle, new Status Register data must be continually clocked out of the device until the state of the RDY/BSY bit changes from a Logical 1 to a Logical 0.

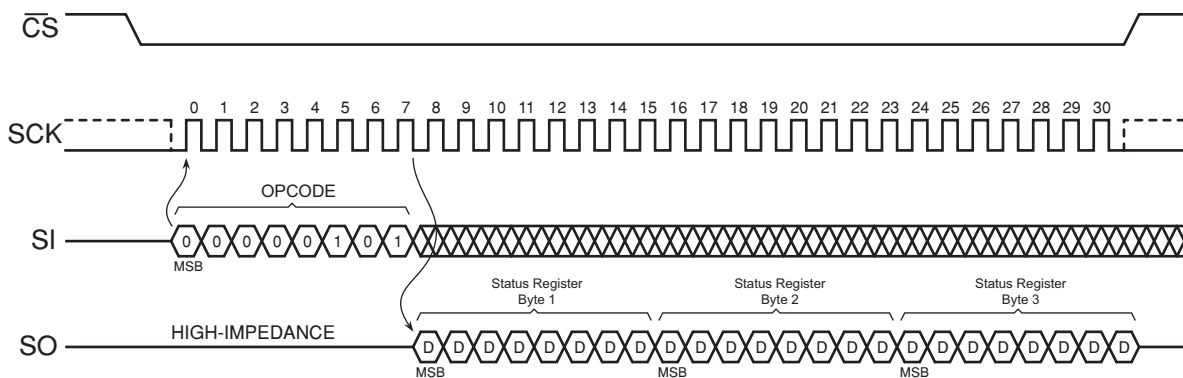


Figure 28. Read Status Register

## 11.2 Write Status Register Byte 1

The Write Status Register Byte 1 command is used to modify the SPRL bit of the Status Register and/or to perform a Global Protect or Global Unprotect operation. Before the Write Status Register Byte 1 command can be issued, the Write Enable command must have been previously issued to set the WEL bit in the Status Register to a Logical 1.

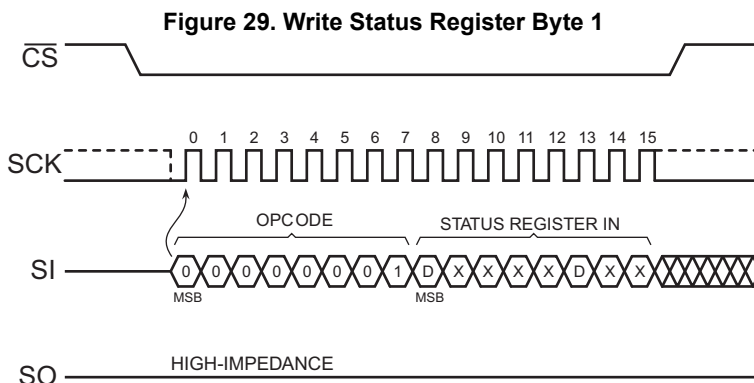
To issue the Write Status Register Byte 1 command, the  $\overline{CS}$  pin must first be asserted and then the opcode 01h must be clocked into the device followed by one byte of data. The one byte of data consists of the SPRL bit value, a don't-care bit, four data bits to denote whether a Global Protect or Unprotect must be performed, and two additional don't-care bits (see Table 14). Any additional data bytes that are sent to the device is ignored. When the  $\overline{CS}$  pin is deasserted, the SPRL bit in the Status Register is modified, and the WEL bit in the Status Register is reset back to a Logical 0. The values of bits 5, 4, 3, and 2 and the state of the SPRL bit before the Write Status Register Byte 1 command was executed (the prior state of the SPRL bit) determine whether or not a Global Protect or Global Unprotect is performed. See “Global Protect/Unprotect” on page 29 for more details.

The complete one byte of data must be clocked into the device before the  $\overline{CS}$  pin is deasserted, and the  $\overline{CS}$  pin must be deasserted on even byte boundaries (multiples of eight bits); otherwise, the device aborts the operation, the state of the SPRL bit does not change, no potential Global Protect or Unprotect is performed, and the WEL bit in the Status Register is reset back to the Logical 0 state.

If the  $\overline{WP}$  pin is asserted, then the SPRL bit can only be set to a Logical 1. If an attempt is made to reset the SPRL bit to a Logical 0 while the  $\overline{WP}$  pin is asserted, then the Write Status Register Byte 1 command is ignored, and the WEL bit in the Status Register is reset back to the Logical 0 state. In order to reset the SPRL bit to a Logical 0, the  $\overline{WP}$  pin must be deasserted.

Table 14. Write Status Register Byte 1 Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPRL	X	Global Protect/Unprotect				X	X



### 11.3 Write Status Register Byte 2

The Write Status Register Byte 2 command is used to modify the RSTE and SLE bits of the Status Register. Using the Write Status Register Byte 2 command is the only way to modify the RSTE and SLE bits in the Status Register during normal device operation, and the SLE bit can only be modified if the sector lockdown state has not been frozen. Before the Write Status Register Byte 2 command can be issued, the Write Enable command must have been previously issued to set the WEL bit in the Status Register to a Logical 1.

To issue the Write Status Register Byte 2 command, the  $\overline{CS}$  pin must first be asserted, and then the opcode 31h must be clocked into the device followed by one byte of data. The one byte of data consists of three don't-care bits, the RSTE bit value, the SLE bit value, and three additional don't-care bits (see Table 15). Any additional data bytes sent to the device are ignored. When the  $\overline{CS}$  pin is deasserted, the RSTE and SLE bits in the Status Register are modified, and the WEL bit in the Status Register is reset back to a Logical 0. The SLE bit is only modified if the Freeze Sector Lockdown State command has not been previously issued.

The complete one byte of data must be clocked into the device before the  $\overline{CS}$  pin is deasserted, and the  $\overline{CS}$  pin must be deasserted on even byte boundaries (multiples of eight bits); otherwise, the device aborts the operation, the state of the RSTE and SLE bits does not change, and the WEL bit in the Status Register is reset back to the Logical 0 state.

Table 15. Write Status Register Byte 2 Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	RSTE	SLE	X	X	X

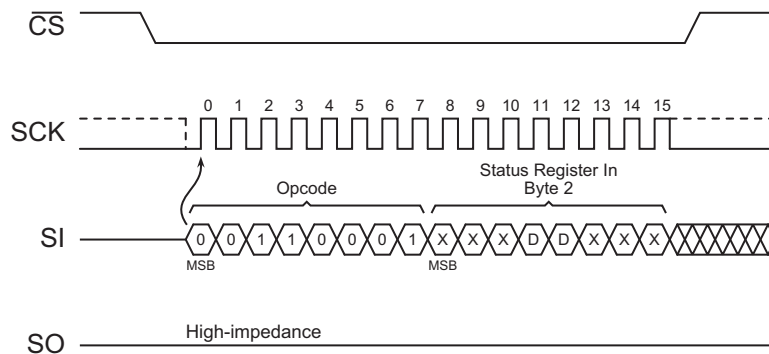


Figure 30. Write Status Register Byte 2

## 12. Other Commands and Functions

### 12.1 Reset

In some applications, it can be necessary to prematurely terminate a program or erase cycle rather than wait the hundreds of microseconds or milliseconds necessary for the program or erase operation to complete normally. The Reset command allows a program or erase operation in progress to be ended abruptly and returns the device to an idle state. Since the need to reset the device is immediate, the Write Enable command does not need to be issued prior to the Reset command. Therefore, the Reset command operates independently of the state of the WEL bit in the Status Register.

The Reset command can be executed only if the command has been enabled by setting the Reset Enabled (RSTE) bit in the Status Register to a Logical 1. If the Reset command has not been enabled (the RSTE bit is in the Logical 0 state), then any attempts at executing the Reset command are ignored.

To perform a Reset, the  $\overline{CS}$  pin must first be asserted, and then the opcode F0h must be clocked into the device. No address bytes need to be clocked in, but a confirmation byte of D0h must be clocked into the device immediately after the opcode. Any additional data clocked into the device after the confirmation byte are ignored. When the  $\overline{CS}$  pin is deasserted, the program or erase operation currently in progress is terminated within a time of  $t_{RST}$ . Since the program or erase operation may not complete before the device is reset, the contents of the page being programmed or the block being erased cannot be guaranteed to be valid.

The Reset command has no effect on the states of the Sector Protection Registers, the Sector Lockdown Registers, the Configuration Register, or the SPRL, RSTE, and SLE bits in the Status Register. The WEL, PS, and ES bits of the Status Register, however, are reset back to their default states. If a Reset operation is performed while a sector is erase suspended, the suspend operation aborts, and the contents of the block being erased in the suspended sector are left in an undefined state. If a Reset is performed while a sector is program suspended, the suspend operation aborts, and the contents of the page that was being programmed and subsequently suspended are undefined. The remaining pages in the 64 kB sector retain their previous contents.

The complete opcode and confirmation byte must be clocked into the device before the  $\overline{CS}$  pin is deasserted, and the  $\overline{CS}$  pin must be deasserted on an even byte boundary (multiples of eight bits); otherwise, no Reset operation is performed.

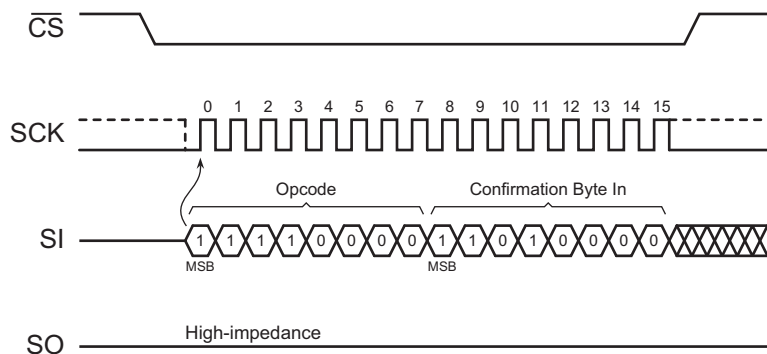


Figure 31. Reset

## 12.2 Read Manufacturer and Device ID

Identification information can be read from the device to enable systems to electronically query and identify the device while it is in the system. The identification method and the command opcode comply with the JEDEC standard for “Manufacturer and Device ID Read Methodology for SPI Compatible Serial Interface Memory Devices”. The type of information that can be read from the device includes the JEDEC-defined Manufacturer ID, the vendor-specific Device ID, and the vendor-specific Extended Device Information.

The Read Manufacturer and Device ID command is limited to a maximum clock frequency of  $f_{CLK}$ . Since not all Flash devices are capable of operating at very high clock frequencies, applications must be designed to read the identification information from the devices at a reasonably low clock frequency to ensure that all devices to be used in the application can be identified properly. Once the identification process is complete, the application can then increase the clock frequency to accommodate specific Flash devices that are capable of operating at the higher clock frequencies.

To read the identification information, the  $\overline{CS}$  pin must first be asserted and then the opcode 9Fh must be clocked into the device. After the opcode has been clocked in, the device begins outputting the identification data on the SO pin during the subsequent clock cycles. The first byte to be output is the Manufacturer ID, followed by two bytes of Device ID information. The fourth byte output is the Extended Device Information (EDI) String Length, which is 01h indicating that one byte of EDI data follows. After the one byte of EDI data is output, the SO pin goes into a high-impedance state; therefore, additional clock cycles have no effect on the SO pin and no data are output. As indicated in the JEDEC standard, reading the EDI String Length and any subsequent data is optional.

Deasserting the  $\overline{CS}$  pin terminates the Manufacturer and Device ID Read operation and put the SO pin into a high-impedance state. The  $\overline{CS}$  pin can be deasserted at any time and does not require that a full byte of data be read.

**Table 16. Manufacturer and Device ID Information**

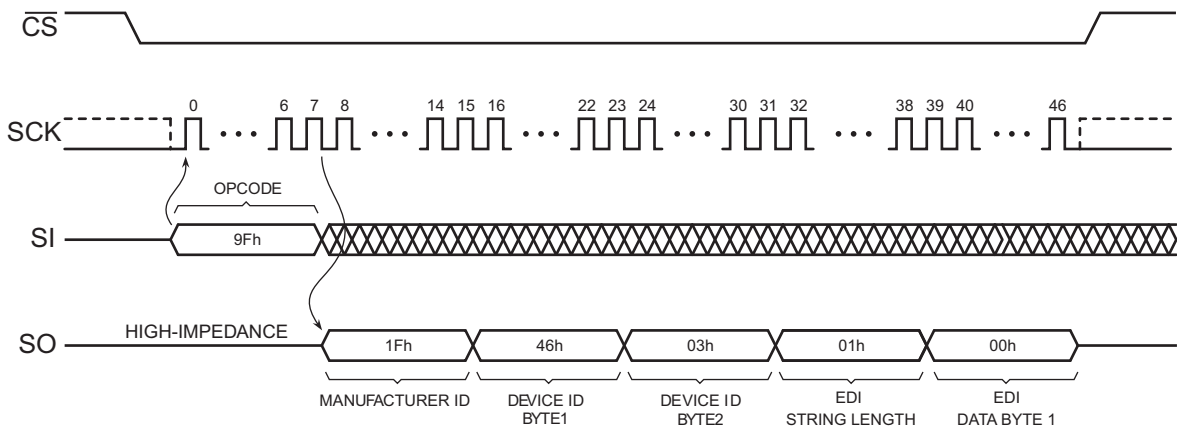
Byte No.	Data Type	Value
1	Manufacturer ID	1Fh
2	Device ID (Byte 1)	46h
3	Device ID (Byte 2)	03h
4	[Optional to Read] Extended Device Information (EDI) String Length	01h
5	[Optional to Read] EDI Byte 1	00h


**Table 17. Manufacturer and Device ID Details**

Data Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex Value	Details
Manufacturer ID	JEDEC Assigned Code								1Fh	JEDEC code: 0001 1111 (1Fh for Renesas Electronics)
	0	0	0	1	1	1	1	1		
Device ID (Byte 1)	Family Code			Density Code					46h	Family code: 010 (SPI or Dual-I/O) Density code: 00110 (16-Mbit)
	0	1	0	0	0	1	1	0		
Device ID (Byte 2)	Sub Code			Product Variant					03h	Sub code: 000 (Standard Series) Product variant: 00011
	0	0	0	0	0	0	1	1		

**Table 18. EDI Data**

Byte Number	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex Value	Details
1	RFU			Device Revision					00h	RFU: Reserved for future use Device revision: 00000 (Initial version)
	0	0	0	0	0	0	0	0		



Note: Each transition  shown for SI and SO represents one byte (8 bits)

**Figure 32. Read Manufacturer and Device ID**



### 12.3 Deep Power-Down

During normal operation, the device is placed in the standby mode to consume less power as long as the  $\overline{CS}$  pin remains deasserted and no internal operation is in progress. The Deep Power-Down command offers the ability to place the device into an even lower power consumption state called the Deep Power-Down mode.

When the device is in the Deep Power-Down mode, all commands including the Read Status Register command are ignored with the exception of the Resume from Deep Power-Down command. Since all commands are ignored, the mode can be used as an extra protection mechanism against program and erase operations.

Entering the Deep Power-Down mode is accomplished by simply asserting the  $\overline{CS}$  pin, clocking in the opcode B9h, and then deasserting the  $\overline{CS}$  pin. Any additional data clocked into the device after the opcode are ignored. When the  $\overline{CS}$  pin is deasserted, the device enters the Deep Power-Down mode within the maximum time of  $t_{EDPD}$ .

The complete opcode must be clocked in before the  $\overline{CS}$  pin is deasserted, and the  $\overline{CS}$  pin must be deasserted on an even byte boundary (multiples of eight bits); otherwise, the device aborts the operation and returns to the standby mode once the  $\overline{CS}$  pin is deasserted. In addition, the device defaults to the standby mode after a power cycle.

The Deep Power-Down command is ignored if an internally self-timed operation such as a program or erase cycle is in progress. The Deep Power-Down command must be reissued after the internally self-timed operation has been completed in order for the device to enter the Deep Power-Down mode.

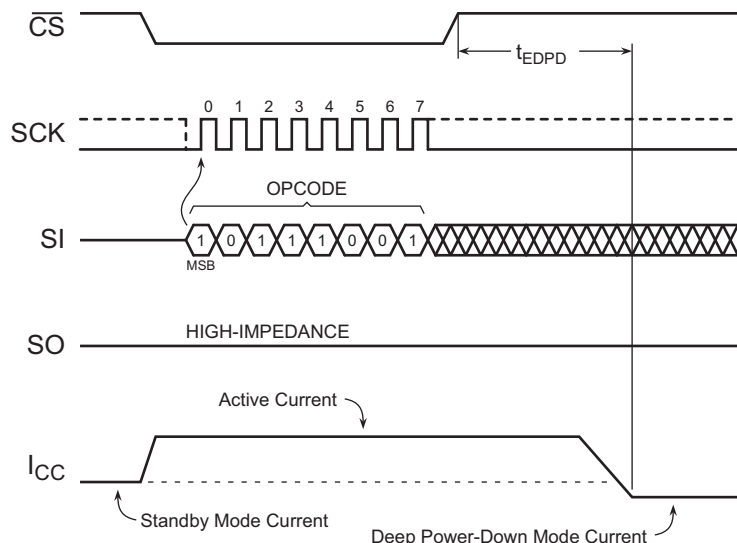


Figure 33. Deep Power-Down

## 12.4 Resume from Deep Power-Down

In order to exit the Deep Power-Down mode and resume normal device operation, the Resume from Deep Power-Down command must be issued. The Resume from Deep Power-Down command is the only command that the device recognizes while in the Deep Power-Down mode.

To resume from the Deep Power-Down mode, the  $\overline{CS}$  pin must first be asserted and then the opcode ABh must be clocked into the device. Any additional data clocked into the device after the opcode are ignored. When the  $\overline{CS}$  pin is deasserted, the device exits the Deep Power-Down mode and return to the standby mode within the maximum time of  $t_{RDPD}$ . After the device has returned to the standby mode, normal command operations such as Read Array can be resumed.

If the complete opcode is not clocked in before the  $\overline{CS}$  pin is deasserted, or if the  $\overline{CS}$  pin is not deasserted on an even byte boundary (multiples of eight bits), then the device aborts the operation and return to the Deep Power-Down mode.

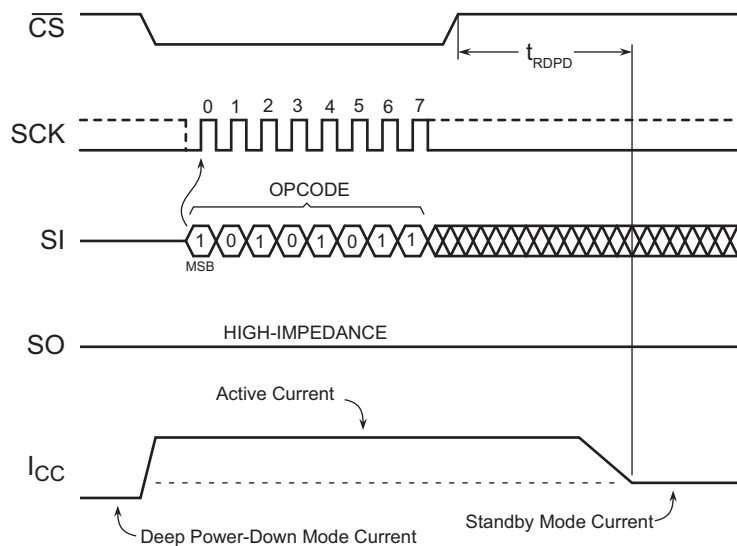


Figure 34. Resume from Deep Power-Down

## 12.5 Hold

The  $\overline{\text{HOLD}}$  pin is used to pause the serial communication with the device without having to stop or reset the clock sequence. The Hold mode, however, does not have an affect on any internally self-timed operations such as a program or erase cycle. Therefore, if an erase cycle is in progress, asserting the  $\overline{\text{HOLD}}$  pin does not pause the operation and the erase cycle continues until it is finished.

The Hold mode can only be entered while the  $\overline{\text{CS}}$  pin is asserted. The Hold mode is activated simply by asserting the  $\overline{\text{HOLD}}$  pin during the SCK low pulse. If the  $\overline{\text{HOLD}}$  pin is asserted during the SCK high pulse, then the Hold mode won't be started until the beginning of the next SCK low pulse. The device remains in the Hold mode as long as the  $\overline{\text{HOLD}}$  pin and  $\overline{\text{CS}}$  pin are asserted.

While in the Hold mode, the SO pin is in a high-impedance state. In addition, both the SI pin and the SCK pin are ignored. The  $\overline{\text{WP}}$  pin, however, can still be asserted or deasserted while in the Hold mode.

To end the Hold mode and resume serial communication, the  $\overline{\text{HOLD}}$  pin must be deasserted during the SCK low pulse. If the  $\overline{\text{HOLD}}$  pin is deasserted during the SCK high pulse, then the Hold mode won't end until the beginning of the next SCK low pulse.

If the  $\overline{\text{CS}}$  pin is deasserted while the  $\overline{\text{HOLD}}$  pin is still asserted, then any operation that may have been started is aborted and the device resets the WEL bit in the Status Register back to the Logical 0 state.

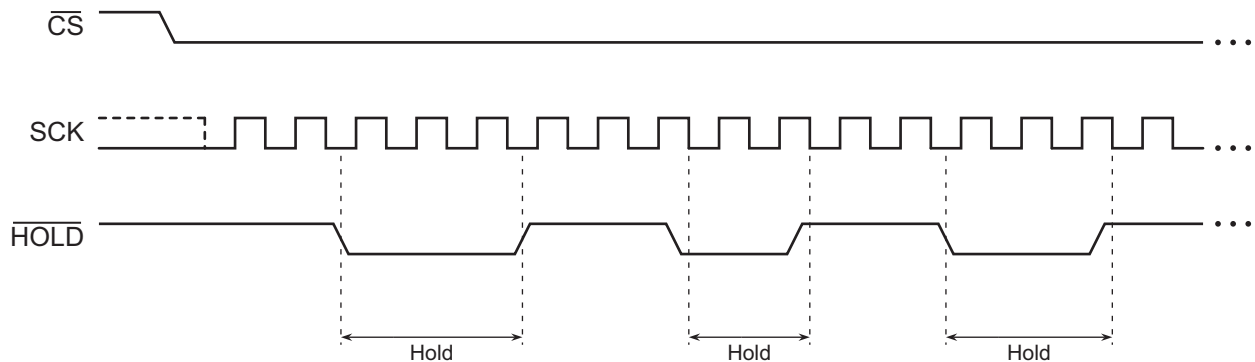


Figure 35. Hold Mode

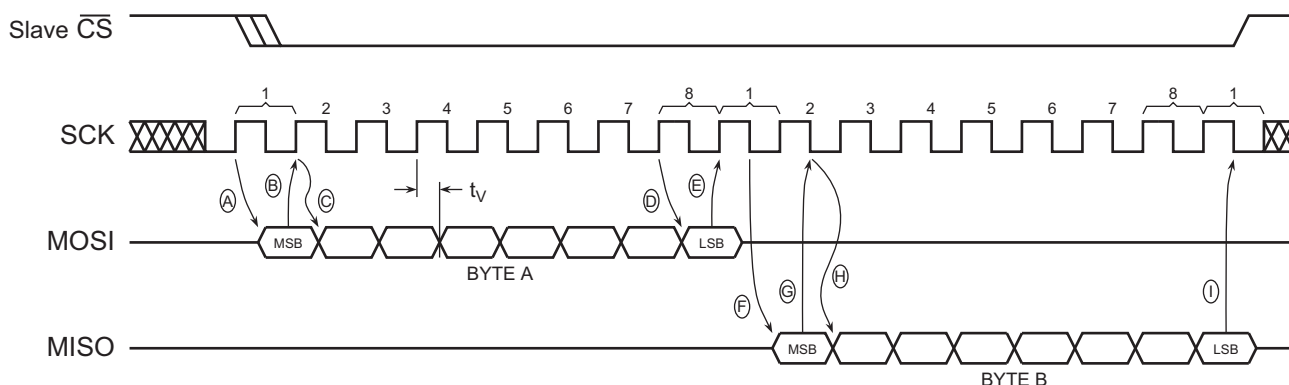
### 13. RapidS Implementation

To implement RapidS and operate at clock frequencies higher than what can be achieved in a viable SPI implementation, a full clock cycle can be used to transmit data back and forth across the serial bus. The AT25DL161 is designed to always clock its data out on the falling edge of the SCK signal and clock data in on the rising edge of SCK.

For full clock cycle operation to be achieved, when the AT25DL161 is clocking data out on the falling edge of SCK, the host controller must wait until the next falling edge of SCK to latch the data in. Similarly, the host controller must clock its data out on the rising edge of SCK in order to give the AT25DL161 a full clock cycle to latch the incoming data in on the next rising edge of SCK.

Implementing RapidS allows a system to run at higher clock frequencies since a full clock cycle is used to accommodate a device’s clock-to-output time, input setup time, and associated rise/fall times.

**Example:** If the system clock frequency is 100 MHz (10ns cycle time) with a 50% duty cycle, and the host controller has an input setup time of 2ns, then a standard SPI implementation would require that the slave device be capable of outputting its data in less than 3ns to meet the 2ns host controller setup time [(10ns x 50%) – 2ns] not accounting for rise/fall times. In an SPI Mode 0 or 3 implementation, the SPI Master is designed to clock in data on the next immediate rising edge of SCK after the SPI slave has clocked its data out on the preceding falling edge. This essentially makes SPI a half-clock cycle protocol and requires extremely fast clock-to-output times and input setup times in order to run at high clock frequencies. With a RapidS implementation of this example, however, the full 10ns cycle time is available which gives the slave device up to 8ns, not accounting for rise/fall times, to clock its data out. Likewise, with RapidS, the host controller has more time available to output its data to the slave since the slave device would be clocking that data in a full clock cycle later.



MOSI = Master Out, Slave In      MISO = Master In, Slave Out  
 The **Master** is the ASIC/MCU and the **Slave** is the memory device.

The **Master** always clocks data **out on the rising edge** of SCK and always clocks data **in on the falling edge** of SCK.  
 The **Slave** always clocks data **out on the rising edge** of SCK and always clocks data **in on the falling edge** of SCK.

- A. **Master** clocks **out** first bit of BYTE A on the **rising edge** of SCK.
- B. **Slave** clocks **in** first bit of BYTE A on the next **rising edge** of SCK.
- C. Master clocks out second bit of BYTE A on the same rising edge of SCK.
- D. Last bit of BYTE A is clocked out from the Master.
- E. Last bit of BYTE A is clocked into the slave.
- F. Slave clocks out first bit of BYTE B.
- G. Master clocks in first bit of BYTE B.
- H. Slave clocks out second bit of BYTE B.
- I. Master clocks in last bit of BYTE B.

Figure 36. RapidS Operation

## 14. Electrical Specifications

### 14.1 Absolute Maximum Ratings\*

Temperature under Bias . . . . . -55 °C to +125 °C	*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” can cause permanent damage to the device. Functional operation of the device at these ratings or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability. Voltage extremes referenced in the “Absolute Maximum Ratings” are intended to accommodate short duration undershoot/overshoot conditions, and does not imply or guarantee functional device operation at these levels for any extended period of time.
Storage Temperature. . . . . -65 °C to +150 °C	
All input voltages (including NC pins) with respect to ground. . . . . -0.6 V to +4.1 V	
All output voltages with respect to ground. . . . . -0.6 V to $V_{CC} + 0.5$ V	

### 14.2 DC and AC Operating Range

Parameter		AT25DL161
Operating Temperature (case)	Industrial	-40 °C to +85 °C
	Extended	-40 °C to +105 °C
$V_{CC}$ Power Supply		1.65 V to 1.95 V
Retention <sup>1</sup>		20 years

1. Represents typical value based on equivalent operation derived from Arrhenius calculations under post cycling high temperature conditions; not indicative of performance at constant device operation life at 105 °C.

## 14.3 DC Characteristics

Table 19. DC Characteristics (-40 °C to +85 °C)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{SB}$	Standby Current	$\overline{CS}, \overline{WP}, \overline{HOLD} = V_{CC}$ , all inputs at CMOS levels		25	35	$\mu A$
$I_{DPD}$	Deep Power-Down Current	$\overline{CS}, \overline{WP}, \overline{HOLD} = V_{CC}$ , all inputs at CMOS levels		8	10	$\mu A$
$I_{CC1}$	Active Current, Read Operation	$f = 100 \text{ MHz}; I_{OUT} = 0 \text{ mA};$ $\overline{CS} = V_{IL}, V_{CC} = \text{Max}$		14	20	mA
		$f = 85 \text{ MHz}; I_{OUT} = 0 \text{ mA};$ $\overline{CS} = V_{IL}, V_{CC} = \text{Max}$		14	20	
		$f = 66 \text{ MHz}; I_{OUT} = 0 \text{ mA};$ $\overline{CS} = V_{IL}, V_{CC} = \text{Max}$		13	18	
		$f = 50 \text{ MHz}; I_{OUT} = 0 \text{ mA};$ $\overline{CS} = V_{IL}, V_{CC} = \text{Max}$		13	17	
		$f = 33 \text{ MHz}; I_{OUT} = 0 \text{ mA};$ $\overline{CS} = V_{IL}, V_{CC} = \text{Max}$		12	16	
		$f = 20 \text{ MHz}; I_{OUT} = 0 \text{ mA};$ $\overline{CS} = V_{IL}, V_{CC} = \text{Max}$		10	15	
$I_{CC2}$	Active Current, Program Operation	$\overline{CS} = V_{CC}, V_{CC} = \text{Max}$		17	22	mA
$I_{CC3}$	Active Current, Erase Operation	$\overline{CS} = V_{CC}, V_{CC} = \text{Max}$		14	22	mA
$I_{LI}$	Input Leakage Current	$V_{IN} = \text{CMOS levels}$			1	$\mu A$
$I_{LO}$	Output Leakage Current	$V_{OUT} = \text{CMOS levels}$			1	$\mu A$
$V_{IL}$	Input Low Voltage				$0.2 \times V_{CC}$	V
$V_{IH}$	Input High Voltage		$0.8 \times V_{CC}$			V
$V_{OL}$	Output Low Voltage	$I_{OL} = 1.6 \text{ mA}; V_{CC} = \text{Min}$			0.2	V
$V_{OH}$	Output High Voltage	$I_{OH} = -100 \mu A; V_{CC} = \text{Min}$	$V_{CC} - 0.2 \text{ V}$			V

Table 20. DC Characteristics (-40 °C to +105 °C)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{SB}$	Standby Current	$\overline{CS}, \overline{WP}, \overline{HOLD} = V_{CC}$ , all inputs at CMOS levels		30	45 <sup>1</sup>	$\mu A$
$I_{DPD}$	Deep Power-Down Current	$\overline{CS}, \overline{WP}, \overline{HOLD} = V_{CC}$ , all inputs at CMOS levels		8	10	$\mu A$
$I_{CC1}$	Active Current, Read Operation	$f = 100 \text{ MHz}; I_{OUT} = 0 \text{ mA};$ $\overline{CS} = V_{IL}, V_{CC} = \text{Max}$		16	22	mA
		$f = 85 \text{ MHz}; I_{OUT} = 0 \text{ mA};$ $\overline{CS} = V_{IL}, V_{CC} = \text{Max}$		15	22	
		$f = 66 \text{ MHz}; I_{OUT} = 0 \text{ mA};$ $\overline{CS} = V_{IL}, V_{CC} = \text{Max}$		15	20	
		$f = 50 \text{ MHz}; I_{OUT} = 0 \text{ mA};$ $\overline{CS} = V_{IL}, V_{CC} = \text{Max}$		13	18	
		$f = 33 \text{ MHz}; I_{OUT} = 0 \text{ mA};$ $\overline{CS} = V_{IL}, V_{CC} = \text{Max}$		13	17	
		$f = 20 \text{ MHz}; I_{OUT} = 0 \text{ mA};$ $\overline{CS} = V_{IL}, V_{CC} = \text{Max}$		11	16	
$I_{CC2}$	Active Current, Program Operation	$\overline{CS} = V_{CC}, V_{CC} = \text{Max}$		17	22	mA
$I_{CC3}$	Active Current, Erase Operation	$\overline{CS} = V_{CC}, V_{CC} = \text{Max}$		14	22	mA
$I_{LI}$	Input Leakage Current	$V_{IN} = \text{CMOS levels}$			1	$\mu A$
$I_{LO}$	Output Leakage Current	$V_{OUT} = \text{CMOS levels}$			1	$\mu A$
$V_{IL}$	Input Low Voltage				$0.2 \times V_{CC}$	V
$V_{IH}$	Input High Voltage		$0.8 \times V_{CC}$			V
$V_{OL}$	Output Low Voltage	$I_{OL} = 1.6 \text{ mA}; V_{CC} = \text{Min}$			0.2	V
$V_{OH}$	Output High Voltage	$I_{OH} = -100 \mu A; V_{CC} = \text{Min}$	$V_{CC} - 0.2 \text{ V}$			V

1. Industrial temperature limit is 35  $\mu A$ .

## 14.4 AC Characteristics

Table 21. AC Characteristics (-40 °C to +85 °C and -40 °C to +105 °C)

Symbol	Parameter	Min	Max	Units
$f_{MAX}$	Maximum clock frequency for all operations – RapidS operation only (excluding 03h, 0Bh, 3Bh, and 9Fh opcodes)		100	MHz
$f_{CLK}$	Maximum clock frequency for all operations (excluding 03h opcode)		85	MHz
$f_{RDLF}$	Maximum clock frequency for 03h opcode (Read Array – Low Frequency)		40	MHz
$f_{RDDO}$	Maximum clock frequency for 3Bh opcode (Dual-Output Read)		66	MHz
$t_{CLKH}$	Clock High Time	4.3		ns
$t_{CLKL}$	Clock Low Time	4.3		ns
$t_{CLKR}^{[1]}$	Clock Rise Time, Peak-to-peak (Slew Rate)	0.1		V/ns
$t_{CLKF}^{[1]}$	Clock Fall Time, Peak-to-peak (Slew Rate)	0.1		V/ns
$t_{CSH}$	Chip Select High Time	30		ns
$t_{CSLS}$	Chip Select Low Setup Time (Relative to Clock)	5		ns
$t_{CSLH}$	Chip Select Low Hold Time (Relative to Clock)	5		ns
$t_{CSHS}$	Chip Select High Setup Time (Relative to Clock)	5		ns
$t_{CSHH}$	Chip Select High Hold Time (Relative to Clock)	5		ns
$t_{DS}$	Data in Setup Time	2		ns
$t_{DH}$	Data in Hold Time	1		ns
$t_{DIS}^{[1]}$	Output Disable Time		5	ns
$t_V^{[2]}$	Output Valid Time		Industrial 5 Extended 6	ns
$t_{OH}$	Output Hold Time	2		ns
$t_{HLS}$	$\overline{HOLD}$ Low Setup Time (Relative to Clock)	5		ns
$t_{HLH}$	$\overline{HOLD}$ Low Hold Time (Relative to Clock)	5		ns
$t_{HHS}$	$\overline{HOLD}$ High Setup Time (Relative to Clock)	5		ns
$t_{HHH}$	$\overline{HOLD}$ High Hold Time (Relative to Clock)	5		ns
$t_{HLQZ}^{[1]}$	$\overline{HOLD}$ Low to Output High-Z		5	ns
$t_{HHQX}^{[1]}$	$\overline{HOLD}$ High to Output Low-Z		5	ns
$t_{WPS}^{[1][3]}$	Write Protect Setup Time	20		ns
$t_{WPH}^{[1][3]}$	Write Protect Hold Time	100		ns
$t_{SECP}^{[1]}$	Sector Protect Time (from Chip Select High)		20	ns
$t_{SECUP}^{[1]}$	Sector Unprotect Time (from Chip Select High)		20	ns
$t_{LOCK}^{[1]}$	Sector Lockdown and Freeze Sector Lockdown State Time (from Chip Select High)		200	$\mu$ s
$t_{EDPD}^{[1]}$	Chip Select High to Deep Power-Down		3	$\mu$ s
$t_{RDPD}^{[1]}$	Chip Select High to Standby Mode		35	$\mu$ s
$t_{RST}$	Reset Time		30	$\mu$ s

1. Not 100% tested (value guaranteed by design and characterization).
2. 15 pF load at frequencies above 70 MHz; otherwise, 30 pF.
3. Only applicable as a constraint for the Write Status Register Byte 1 command when SPRL = 1.



## 14.5 Program and Erase Characteristics

Table 22. Program and Erase Characteristics (-40 °C to +85 °C and -40 °C to +105 °C)

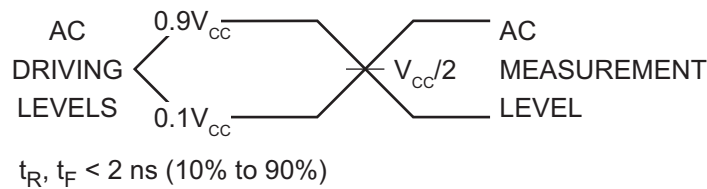
Symbol	Parameter	Min	Typ	Max	Units
$t_{pp}^{[1]}$	Page Program Time (256 bytes)		1.0	3.0	ms
$t_{BP}$	Byte Program Time		8		$\mu$ s
$t_{BLKE}^{[2]}$	Block Erase Time	4 kB	50	200	ms
		32 kB	250	600	
		64 kB	550	950	
$t_{CHPE}^{[1][2]}$	Chip Erase Time		16	28	sec
$t_{SUSP}$	Suspend Time	Program	10	20	$\mu$ s
		Erase	25	40	
$t_{RES}$	Resume Time	Program	10	20	$\mu$ s
		Erase	12	20	
$t_{OTPP}^{[1]}$	OTP Security Register Program Time		200	500	$\mu$ s
$t_{WRSR}^{[2]}$	Write Status Register Time			200	ns

1. Maximum values indicate worst-case performance after 100,000 erase/program cycles.
2. Not 100% tested (value guaranteed by design and characterization).

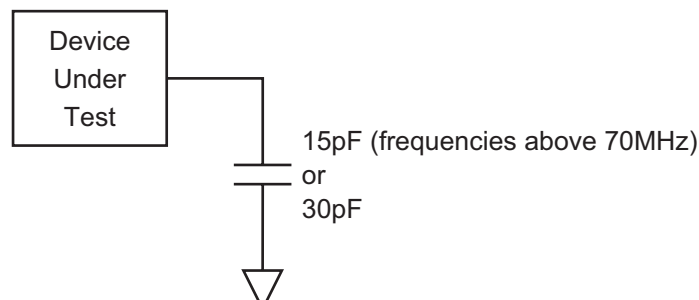
## 14.6 Power-up Conditions

Symbol	Parameter	Min	Max	Units
$t_{VCSL}$	Minimum $V_{CC}$ to Chip Select Low Time	70		$\mu$ s
$t_{PUW}$	Power-up Device Delay Before Program or Erase Allowed		10	ms
$V_{POR}$	Power-on Reset Voltage	1.2	1.55	V

## 14.7 Input Test Waveforms and Measurement Levels



## 14.8 Output Test Load



## 15. AC Waveforms

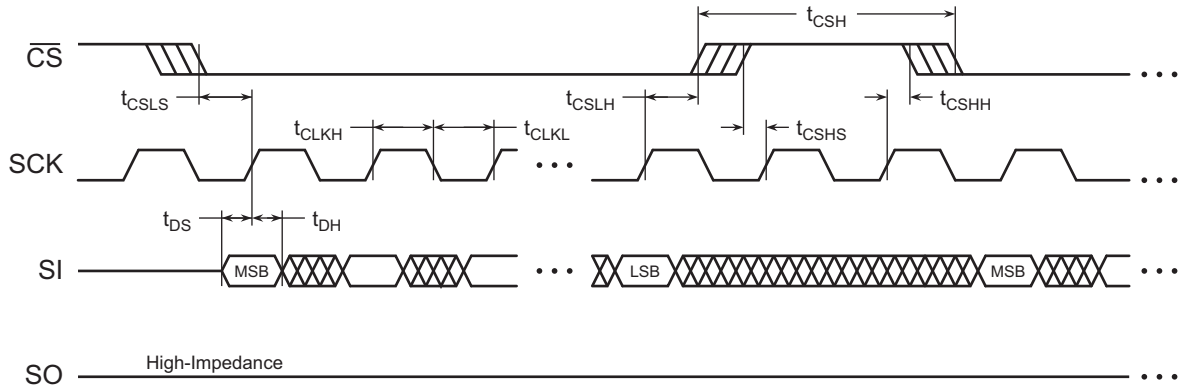


Figure 37. Serial Input Timing

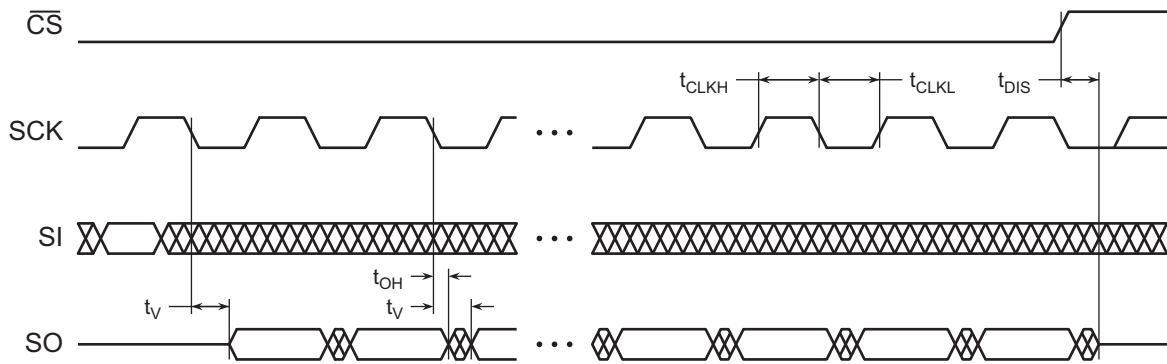


Figure 38. Serial Output Timing

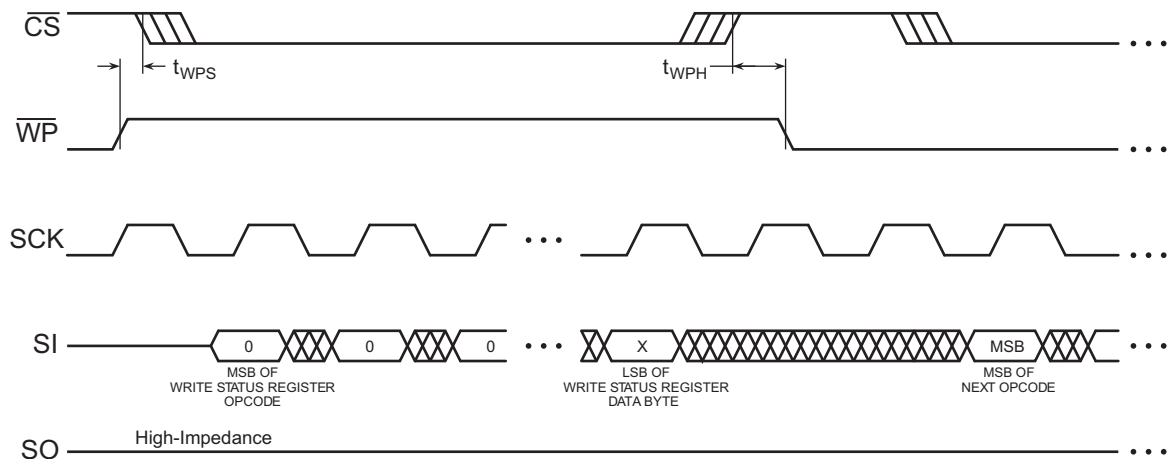


Figure 39.  $\overline{WP}$  Timing for Write Status Register Byte 1 Command When SPRL = 1

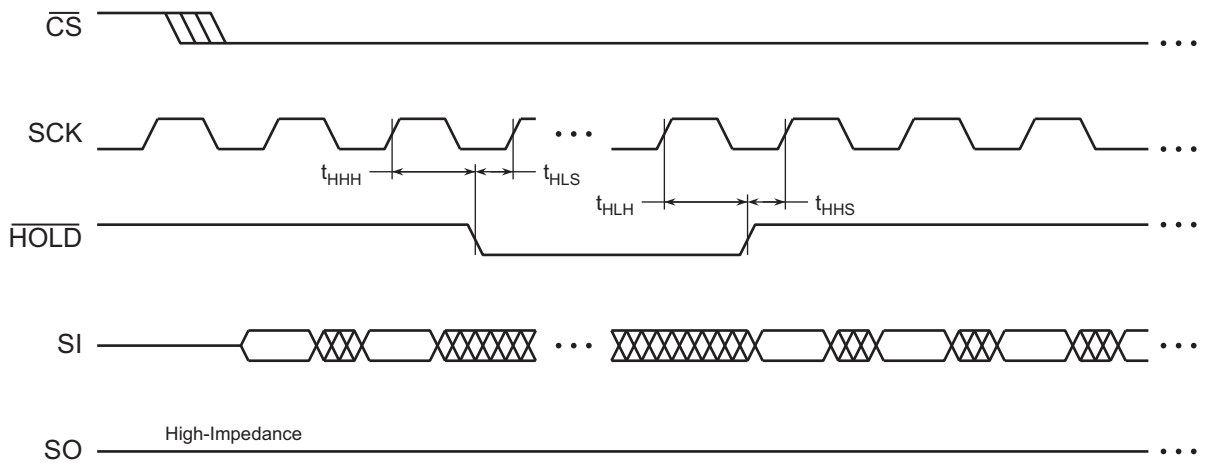


Figure 40.  $\overline{\text{HOLD}}$  Timing – Serial Input

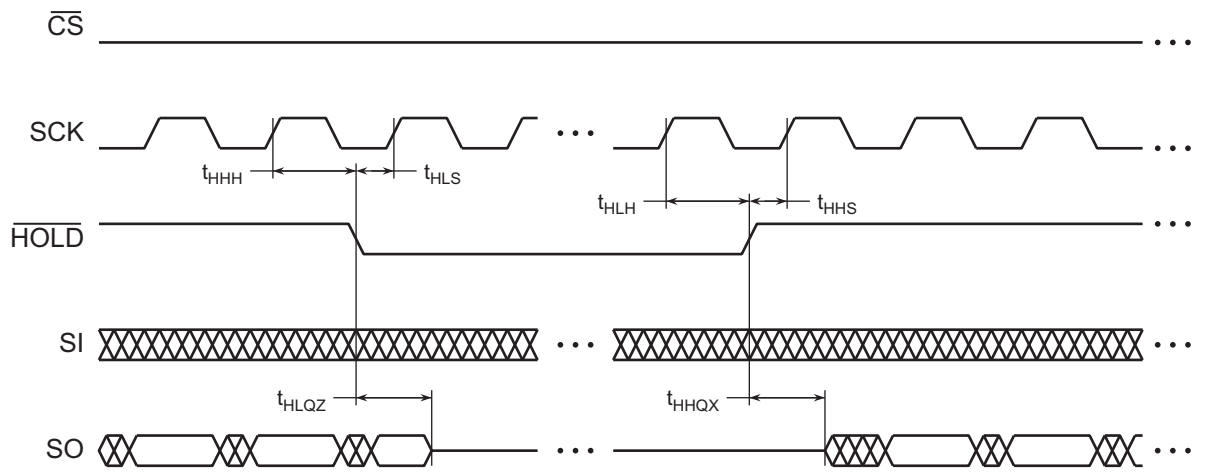
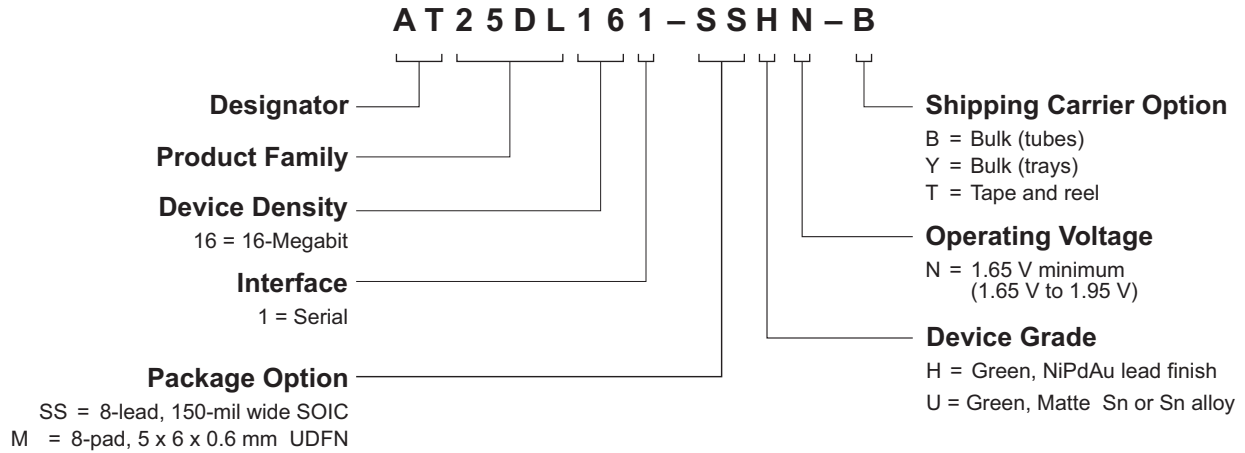


Figure 41.  $\overline{\text{HOLD}}$  Timing – Serial Output

## 16. Ordering Information

### 16.1 Ordering Code Detail



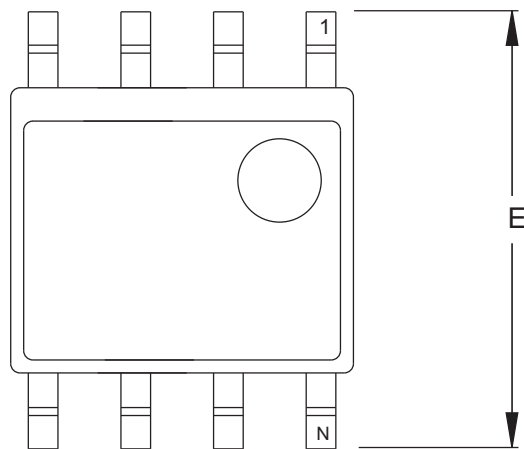
### 16.2 Green Package Options (Pb/halide-free/RoHS-compliant)

Ordering Codes <sup>1</sup>	Package	Lead (Pad) Finish	Operating Voltage	Max. Freq. (MHz)	Operation Range
AT25DL161-SSHNB AT25DL161-SSHNT	8-lead 150-mil, Plastic, Gull Wing, Small Outline	NiPdAu	1.65 V to 1.95 V	100	Industrial (-40 °C to +85 °C)
AT25DL161-MHNY AT25DL161-MHNT	8-pad (5 x 6 x 0.6 mm body), Thermally Enhanced Plastic Ultra Thin Dual Flat No-lead				
AT25DL161-SSHNGA-T AT25DL161-SSHNGA-B	8-lead 150-mil, Plastic, Gull Wing, Small Outline				Extended (-40 °C to +105 °C)

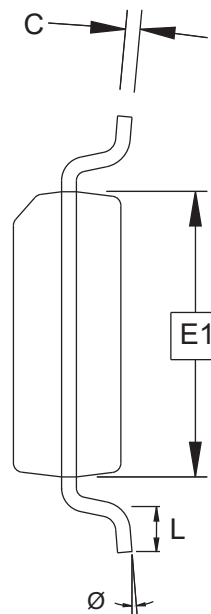
1. The shipping carrier option code is not marked on the devices.

## 17. Packaging Information

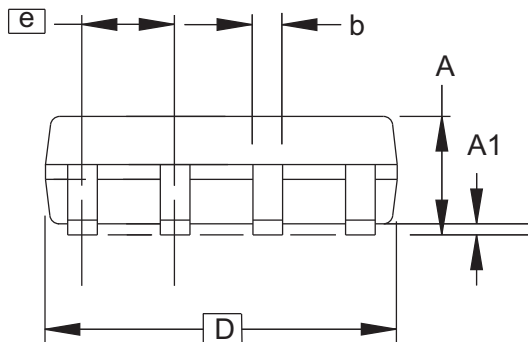
### 17.1 8-Lead, 150-mil JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

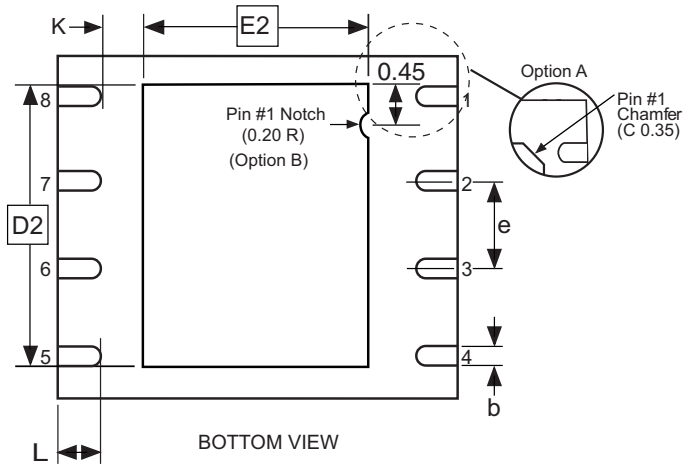
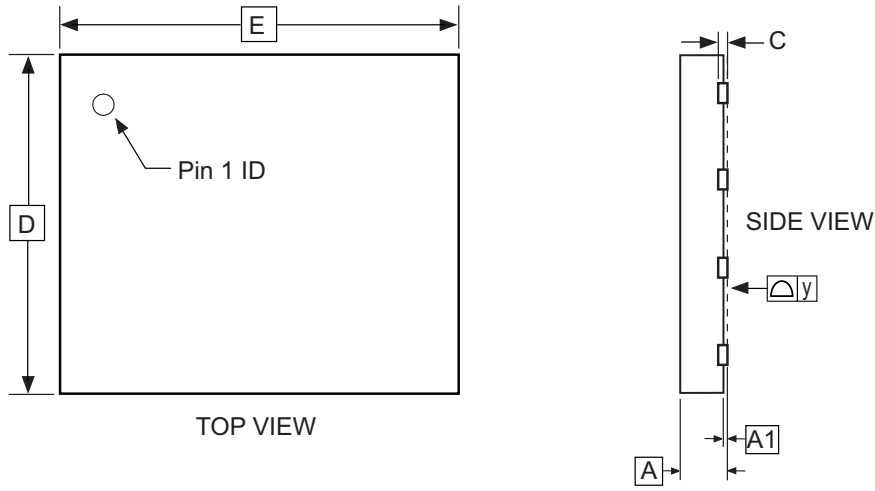
Notes: This drawing is for general information only.  
Refer to JEDEC Drawing MS-012, Variation AA  
for proper dimensions, tolerances, datums, etc.

COMMON DIMENSIONS  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	1.60	1.75	
A1	0.10	0.18	0.25	
b	0.31	0.43	0.51	
C	0.17	0.22	0.25	
D	4.80	4.83	5.05	
E1	3.81	3.90	3.99	
E	5.79	6.00	6.20	
e	1.27 BSC			
L	0.40	0.60	1.27	
Ø	0°	3.75	8°	

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### 17.2 8-Pad, 5 x 6 x 0.6 mm UDFN



COMMON DIMENSIONS  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.45	0.55	0.60	
A1	0.00	0.02	0.05	
b	0.35	0.40	0.48	
C	0.152 REF			
D	4.90	5.00	5.10	
D2	3.80	4.00	4.20	
E	5.90	6.00	6.10	
E2	3.20	3.40	3.60	
e	1.27			
L	0.50	0.60	0.75	
y	0.00	-	0.08	
K	0.20	-	-	

Notes: 1. This package conforms to JEDEC reference MO-229, Saw Singulation.  
2. The terminal #1 ID is a Laser-marked Feature.



## 18. Revision History

Doc. Rev.	Date	Comments
8795A	03/2012	Initial document release.
8795B	05/2012	Decreased $I_{DD}$ maximum from 14 $\mu$ A to 10 $\mu$ A. Decreased $F_{RDDO}$ maximum from 85 $\mu$ A to 66 $\mu$ A. Various typographical edits throughout document.
8795C	09/2012	Removed preliminary status. Add WLCSP package drawing. Updated template and Adesto logo.
8795D	12/2012	Update to Adesto.
8795E	12/2012	Add labels to pins in dBGA package.
8795F	1/2013	Remove die size from daBGA package.
8795G	5/2017	Removed WLCSP package.
8795H	11/2017	Added patent information.
8795I	04/2021	Added nominal values to package drawing in section 17.1.
8795J	02/2022	Changed company logo to Renesas.
8795K	11/2022	Applied new corporate template to document. Integrated the AT25DL161-8795B-HR Addendum into this document.
8795L	9/2023	Corrected Figure 32.

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