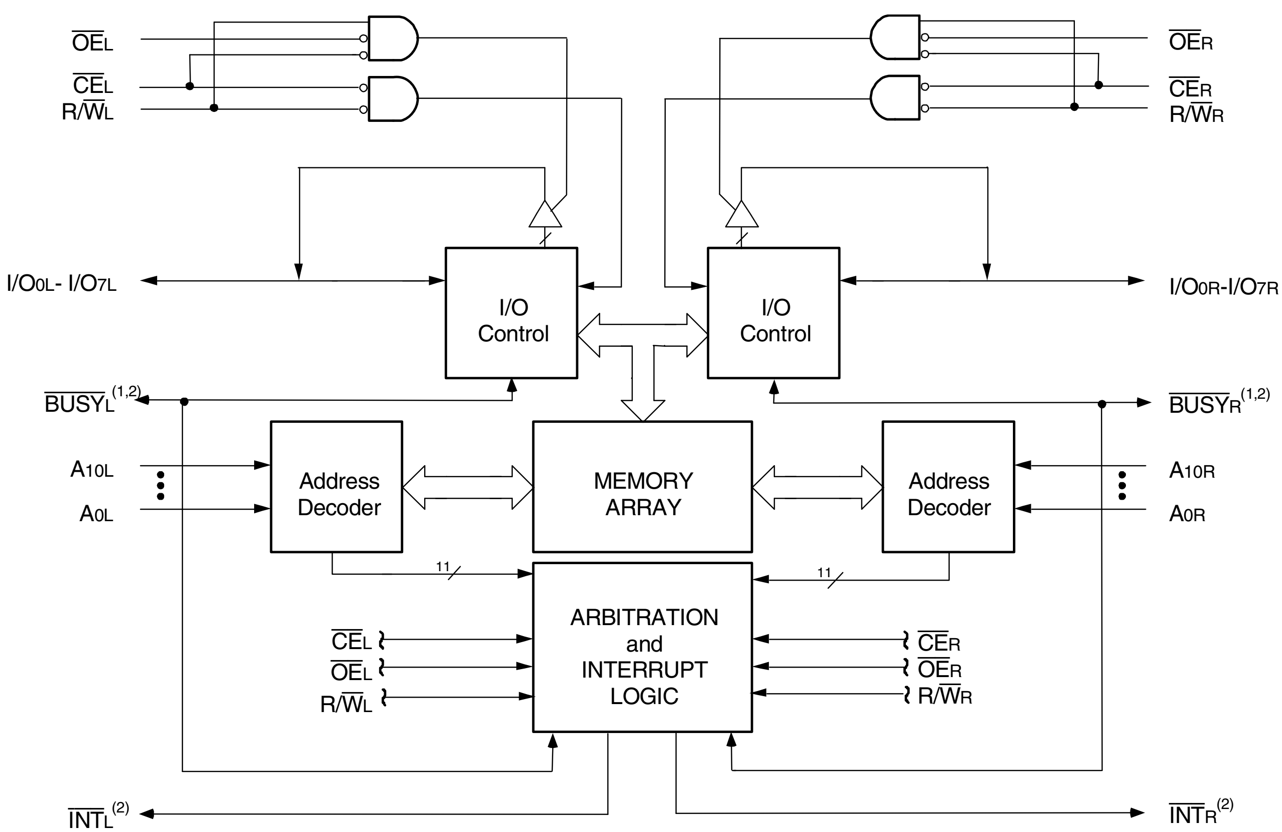
HIGH SPEED 2K X 8 DUAL-PORT STATIC RAM WITH INTERRUPTS

71321SA/LA
71421SA/LA

Features

- **High-speed access**
  - *Commercial: 20/35/55ns (max.)*
  - *Industrial: 25/55ns (max.)*
- **Low-power operation**
  - *IDT71321/IDT71421SA*
    Active: 325mW (typ.)
    Standby: 5mW (typ.)
  - *IDT71321/421LA*
    Active: 325mW (typ.)
    Standby: 1mW (typ.)
- **Two $\overline{\text{INT}}$ flags for port-to-port communications**
- **MASTER IDT71321 easily expands data bus width to 16-or-more-bits using SLAVE IDT71421**
- **On-chip port arbitration logic (IDT71321 only)**
- **$\overline{\text{BUSY}}$ output flag on IDT71321; $\overline{\text{BUSY}}$ input on IDT71421**
- **Fully asynchronous operation from either port**
- **Battery backup operation – 2V data retention (LA only)**
- **TTL-compatible, single 5V ±10% power supply**
- **Available in 52-Pin PLCC, 52-Pin STQFP, 64-Pin TQFP, and 64-Pin STQFP**
- **Industrial temperature range (–40°C to +85°C) is available for selected speeds**
- **Green parts available, see ordering information**

Functional Block Diagram



2691 drw 01

NOTES:
1. IDT71321 (MASTER): $\overline{\text{BUSY}}$ is open drain output and requires pullup resistor of 270Ω.
   IDT71421 (SLAVE): $\overline{\text{BUSY}}$ is input.
2. Open drain output: requires pullup resistor of 270Ω.

SEPTEMBER 2019

Description

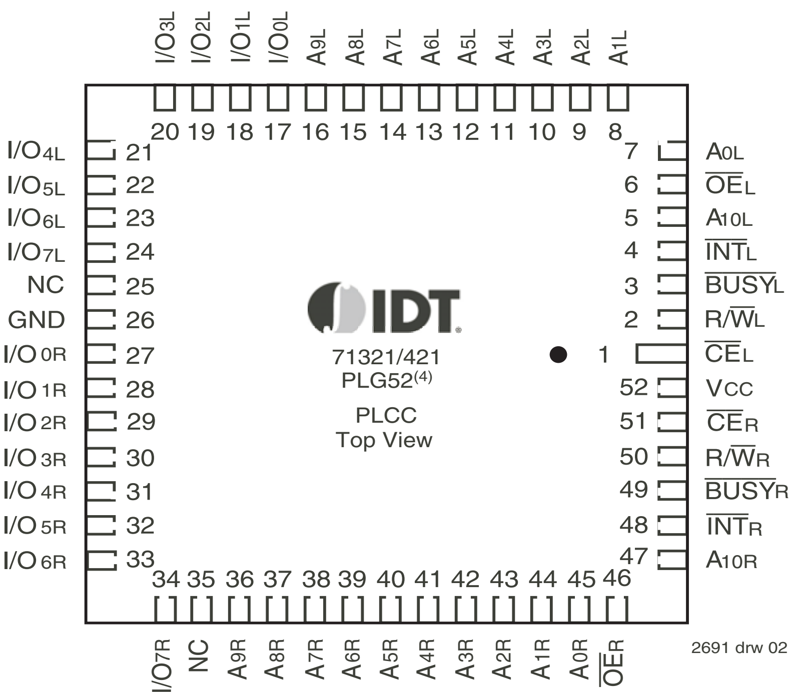
The IDT71321/IDT71421 are high-speed 2K x 8 Dual-Port Static RAMs with internal interrupt logic for interprocessor communications. The IDT71321 is designed to be used as a stand-alone 8-bit Dual-Port Static RAM or as a "MASTER" Dual-Port Static RAM together with the IDT71421 "SLAVE" Dual-Port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE Dual-Port Static RAM approach in 16-or-more-bit memory system applications results in full speed, error-free operation without the need for additional discrete logic.

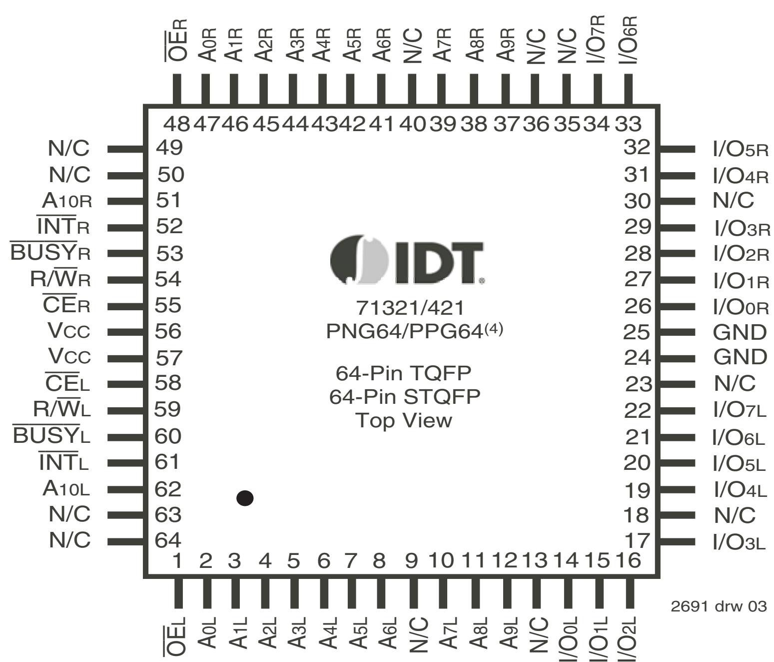
Both devices provide two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on chip circuitry of each port to enter a very low standby power mode.

Fabricated using CMOS high-performance technology, these devices typically operate on only 325mW of power. Low-power (LA) versions offer battery backup data retention capability, with each Dual-Port typically consuming 200µW from a 2V battery.

The IDT71321/IDT71421 devices are packaged in 52-pin PLCC, 52-pin STQFP, 64-pin TQFP, and 64-pin STQFP.

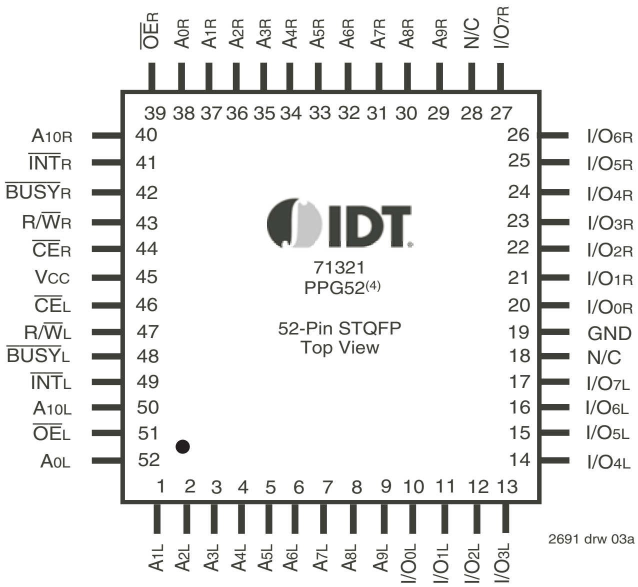
Pin Configurations(1,2,3)





NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. PLG52 package body is approximately .75 in x .75 in x .17 in.
   PNG64 package body is approximately 14mm x 14mm x 1.4mm.
   PPG64 package body is approximately 10mm x 10mm x 1.4mm.
4. This package code is used to reference the package diagram.

Pin Configurations (continued)[1,2,3]



NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. PPG52 package body is approximately 10mm x 10mm x 1.4mm.
4. This package code is used to reference the package diagram.

Capacitance[1]
(TA = +25°C, f = 1.0MHz) TQFP Only

Symbol	Parameter	Conditions[2]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	10	pF

2691 tbl 00

NOTES:
1. This parameter is determined by device characterization but is not production tested.
2. 3dv references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

Absolute Maximum Ratings[1]

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
I_{OUT}	DC Output Current	50	mA

2691 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of $V_{TERM} \geq V_{CC}$ + 10%.

Recommended Operating Temperature and Supply Voltage[1,2]

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

2691 tbl 02

NOTES:
1. This is the parameter T_A. This is the "instant on" case temperature.
2. Industrial temperature: for specific speeds, packages and powers contact your sales office.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0[2]	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

2691 tbl 03

NOTES:
1. V_{IL} (min.) = -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 10%.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[1,4] (V_{CC} = 5.0V ± 10%)

					71321X20 71421X20 Com'l Only		71321X25 71421X25 Com'l & Ind		
Symbol	Parameter	Test Condition	Version		Typ.	Max.	Typ.	Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IL}, Outputs Disabled $f = f_{MAX}$[2]	COM'L	SA LA	110 110	250 200	110 110	220 170	mA
			IND	SA LA	— —	— —	110 110	270 220	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IH} $f = f_{MAX}$[2]	COM'L	SA LA	30 30	65 45	30 30	65 45	mA
			IND	SA LA	— —	— —	30 30	75 55	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[5] Active Port Outputs Disabled, $f = f_{MAX}$[2]	COM'L	SA LA	65 65	165 125	65 65	150 115	mA
			IND	SA LA	— —	— —	65 65	170 140	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ - 0.2V, $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, f = 0[3]	COM'L	SA LA	1.0 0.2	15 5	1.0 0.2	15 5	mA
			IND	SA LA	— —	— —	1.0 0.2	30 10	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}_{"A"} \leq$ 0.2V and $\overline{CE}_{"B"} \geq V_{CC}$ - 0.2V[5] $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Disabled, $f = f_{MAX}$[2]	COM'L	SA LA	60 60	155 115	60 60	145 105	mA
			IND	SA LA	— —	— —	60 60	165 130	

2691 tbl 04a

					71321X35 71421X35 Com'l Only		71321X55 71421X55 Com'l & Ind		
Symbol	Parameter	Test Condition	Version		Typ.	Max.	Typ.	Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IL}, Outputs Disabled $f = f_{MAX}$[2]	COM'L	SA LA	80 80	165 120	65 65	155 110	mA
			IND	SA LA	— —	— —	65 65	190 140	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IH} $f = f_{MAX}$[2]	COM'L	SA LA	25 25	65 45	20 20	65 35	mA
			IND	SA LA	— —	— —	20 20	70 50	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[5] Active Port Outputs Disabled, $f = f_{MAX}$[2]	COM'L	SA LA	50 50	125 90	40 40	110 75	mA
			IND	SA LA	— —	— —	40 40	125 90	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ - 0.2V, $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, f = 0[3]	COM'L	SA LA	1.0 0.2	15 4	1.0 0.2	15 4	mA
			IND	SA LA	— —	— —	1.0 0.2	30 10	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}_{"A"} \leq$ 0.2V and $\overline{CE}_{"B"} \geq V_{CC}$ - 0.2V[5] $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Disabled, $f = f_{MAX}$[2]	COM'L	SA LA	45 45	110 85	40 40	100 70	mA
			IND	SA LA	— —	— —	40 40	110 85	

2691 tbl 04b

NOTES:
1. 'X' in part numbers indicates power rating (SA or LA).
2. At $f = f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of $1/t_{RC}$, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
3. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
4. V_{CC} = 5V, T_A=+25°C for Typ and is not production tested. $V_{CC\ DC}$ = 100mA (Typ)
5. Port "A" may be either left or right port. Port "B" is opposite from port "A".

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	71321SA 71421SA		71321LA 71421LA		Unit
			Min.	Max.	Min.	Max.	
$\lvert I_{LI} \rvert$	Input Leakage Current[1]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\lvert I_{LO} \rvert$	Output Leakage Current[1]	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}, V_{CC} - 5.5V	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O_0-I/O_7)	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$/$\overline{INT}$)	I_{OL} = 16mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2691 tbl 05

NOTE:
1. At Vcc ≤ 2.0V leakages are undefined.

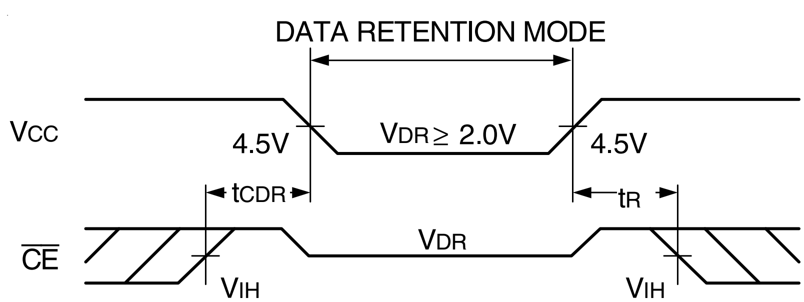
Data Retention Characteristics (LA Version Only)

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			2.0	—	—	V
I_{CCDR}	Data Retention Current	V_{CC} = 2.0V, $\overline{CE}$ ≥ V_{CC} - 0.2V	COM'L	—	100	1500	µA
		V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V	IND	—	100	4000	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

2691 tbl 06

NOTES:
1. V_{CC} = 2V, T_A = +25°C, and is not production tested.
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not production tested.

Data Retention Waveform



2691 drw 04

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1,2 and 3

2691 tbl 07

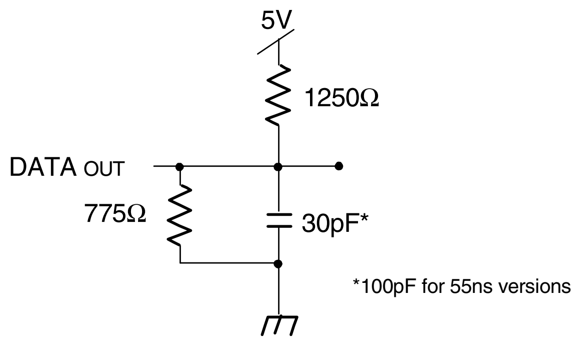


Figure 1. AC Output Test Load

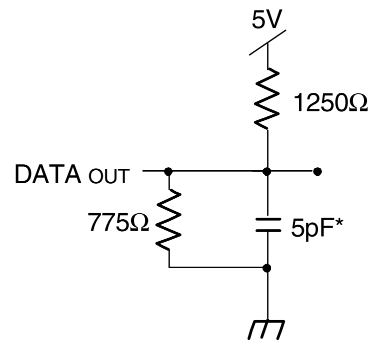
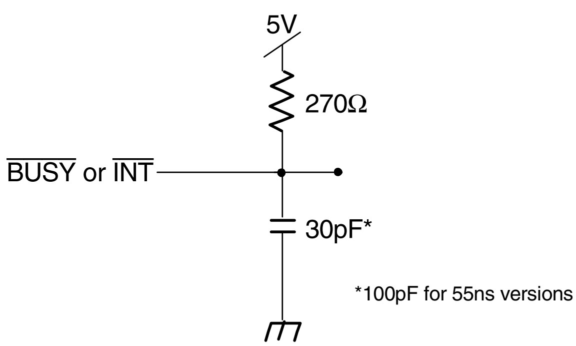


Figure 2. Output Test Load
(for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})
* Including scope and jig.



2691 drw 05

Figure 3. $\overline{\text{BUSY}}$ and $\overline{\text{INT}}$
AC Output Test Load

AC Electrical Characteristics Over the Operating Temperature Supply Voltage Range(2)

Symbol	Parameter	71321X20 71421X20 Com'l Only		71321X25 71421X25 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	20	—	25	—	ns
t_{AA}	Address Access Time	—	20	—	25	ns
t_{ACE}	Chip Enable Access Time	—	20	—	25	ns
t_{AOE}	Output Enable Access Time	—	11	—	12	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	ns
t_{LZ}	Output Low-Z Time(1,3)	0	—	0	—	ns
t_{HZ}	Output High-Z Time(1,3)	—	10	—	10	ns
t_{PU}	Chip Enable to Power Up Time(3)	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time(3)	—	20	—	25	ns

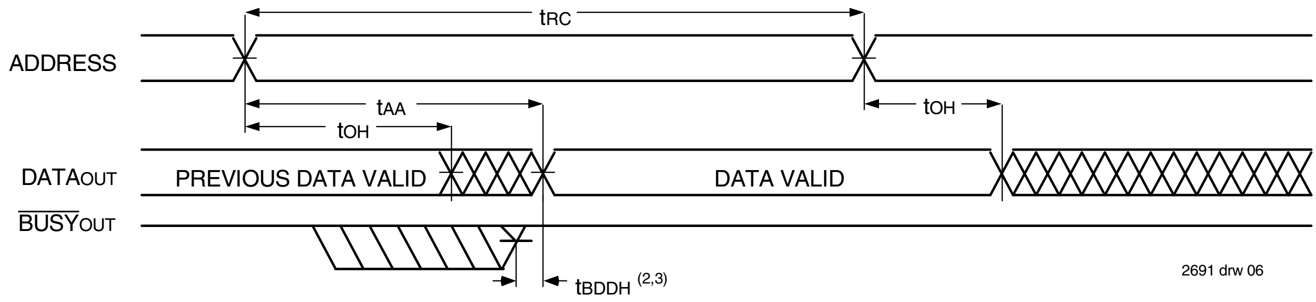
2691 tbl 08a

Symbol	Parameter	71321X35 71421X35 Com'l Only		71321X55 71421X55 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	35	—	55	—	ns
t_{AA}	Address Access Time	—	35	—	55	ns
t_{ACE}	Chip Enable Access Time	—	35	—	55	ns
t_{AOE}	Output Enable Access Time	—	20	—	25	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	ns
t_{LZ}	Output Low-Z Time(1,3)	0	—	5	—	ns
t_{HZ}	Output High-Z Time(1,3)	—	15	—	25	ns
t_{PU}	Chip Enable to Power Up Time(3)	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time(3)	—	35	—	50	ns

2691 tbl 08b

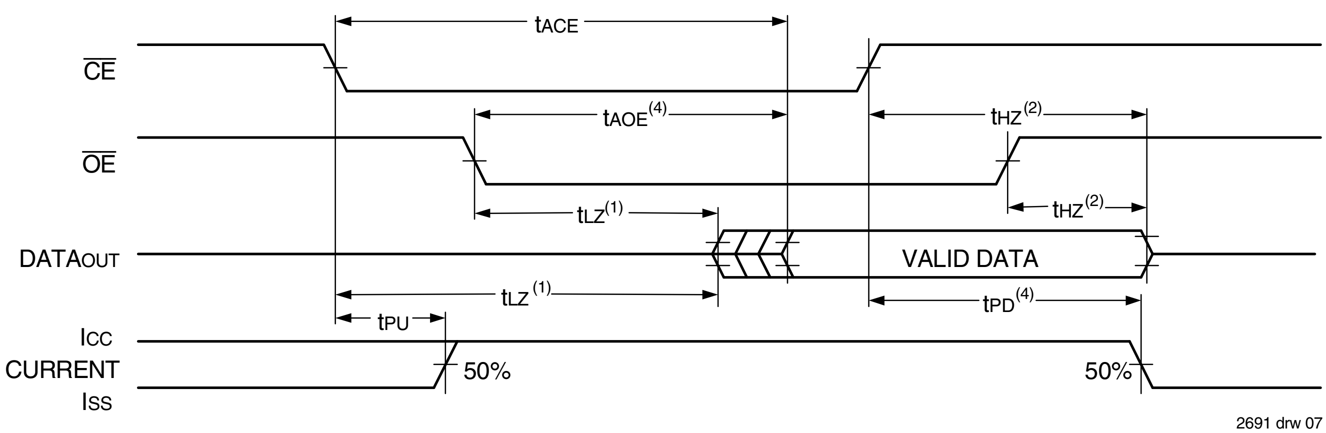
NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage Output Test Load (Figure 2).
2. 'X' in part numbers indicates power rating (SA or LA).
3. This parameter is guaranteed by device characterization, but is not production tested.

Timing Waveform of Read Cycle No. 1, Either Side(1)



NOTES:
1. R/$\overline{W}$ = VIH, $\overline{CE}$ = VIL, and is $\overline{OE}$ = VIL. Address is valid prior to the coincidental with $\overline{CE}$ transition LOW.
2. tBDD delay is required only in the case where the opposite port is completing a write operation to the same address location. For simultaneous read operations $\overline{BUSY}$ has no relationship to valid output data.
3. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA, and tBDD.

Timing Waveform of Read Cycle No. 2, Either Side (3)



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first, $\overline{OE}$ or $\overline{CE}$.
3. R/$\overline{W}$ = VIH and $\overline{OE}$ = VIL, and the address is valid prior to or coincidental with $\overline{CE}$ transition LOW.
4. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA, and tBDD.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[4]

Symbol	Parameter	71321X20 71421X20 Com'l Only Min.	71321X20 71421X20 Com'l Only Max.	71321X25 71421X25 Com'l & Ind Min.	71321X25 71421X25 Com'l & Ind Max.	Unit
WRITE CYCLE						
t_{WC}	Write Cycle Time[2]	20	—	25	—	ns
t_{EW}	Chip Enable to End-of-Write	15	—	20	—	ns
t_{AW}	Address Valid to End-of-Write	15	—	20	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	ns
t_{WP}	Write Pulse Width[3]	15	—	15	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	10	—	12	—	ns
t_{HZ}	Output High-Z Time[1]	—	10	—	10	ns
t_{DH}	Data Hold Time	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z[1]	—	10	—	10	ns
t_{OW}	Output Active from End-of-Write[1]	0	—	0	—	ns

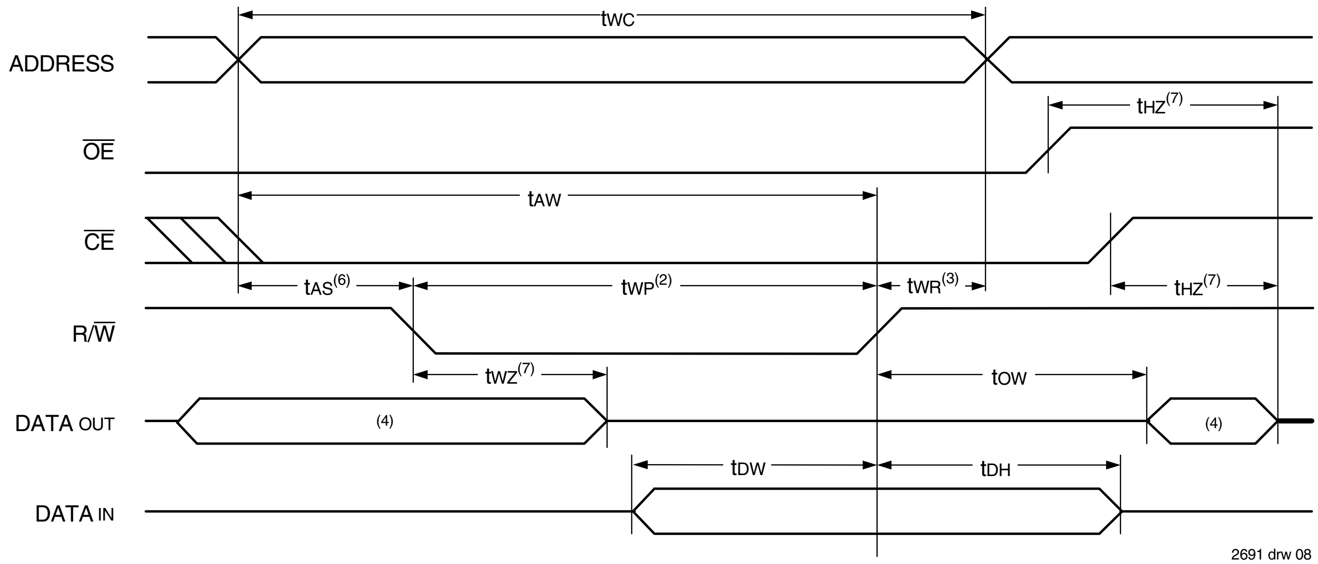
2691 tbl 09a

Symbol	Parameter	71321X35 71421X35 Com'l Only Min.	71321X35 71421X35 Com'l Only Max.	71321X55 71421X55 Com'l & Ind Min.	71321X55 71421X55 Com'l & Ind Max.	Unit
WRITE CYCLE						
t_{WC}	Write Cycle Time[2]	35	—	55	—	ns
t_{EW}	Chip Enable to End-of-Write	30	—	40	—	ns
t_{AW}	Address Valid to End-of-Write	30	—	40	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	ns
t_{WP}	Write Pulse Width[3]	25	—	30	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	15	—	20	—	ns
t_{HZ}	Output High-Z Time[1]	—	15	—	25	ns
t_{DH}	Data Hold Time	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z[1]	—	15	—	30	ns
t_{OW}	Output Active from End-of-Write[1]	0	—	0	—	ns

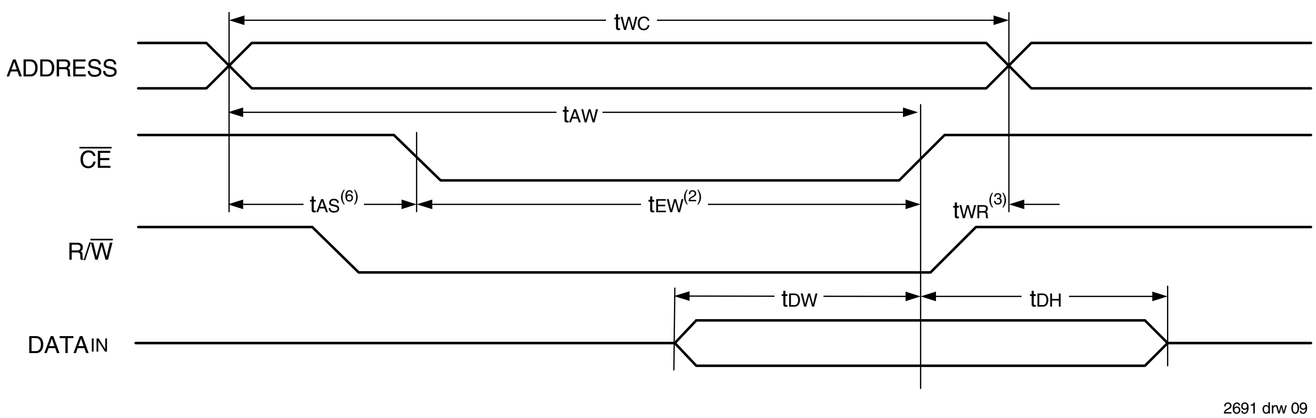
2691 tbl 09b

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2). This parameter is guaranteed by device characterization but is not production tested.
2. For Master/Slave combination, $t_{WC} = t_{BAA} + t_{WP}$, since $R/\overline{W} = V_{IL}$ must occur after t_{BAA} .
3. If $\overline{OE}$ is LOW during a $R/\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or ($t_{WZ} + t_{DW}$) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $R/\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
4. 'X' in part numbers indicates power rating (SA or LA).

Timing Waveform of Write Cycle No. 1, (R/$\overline{W}$ Controlled Timing)(1,5,8)



Timing Waveform of Write Cycle No. 2, ($\overline{CE}$ Controlled Timing)(1,5)



NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of $\overline{CE}$ = V_{IL} and R/W= V_{IL}.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
7. This parameter is determined to be device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(6)

Symbol	Parameter	71321X20 71421X20 Com'l Only Min.	Max.	71321X25 71421X25 Com'l & Ind Min.	Max.	Unit
$\overline{BUSY}$ TIMING (For MASTER 71321)						
t_{BAA}	$\overline{BUSY}$ Access Time from Address	—	20	—	20	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address	—	20	—	20	ns
t_{BAC}	$\overline{BUSY}$ Access Time from Chip Enable	—	20	—	20	ns
t_{BDC}	$\overline{BUSY}$ Disable Time from Chip Enable	—	20	—	20	ns
t_{WH}	Write Hold After $\overline{BUSY}$(5)	12	—	15	—	ns
t_{WDD}	Write Pulse to Data Delay(1)	—	50	—	50	ns
t_{DDD}	Write Data Valid to Read Data Delay(1)	—	35	—	35	ns
t_{APS}	Arbitration Priority Set-up Time(2)	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data(3)	—	25	—	35	ns
$\overline{BUSY}$ INPUT TIMING (For SLAVE 71421)						
t_{WB}	Write to $\overline{BUSY}$ Input(4)	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$(5)	12	—	15	—	ns
t_{WDD}	Write Pulse to Data Delay(1)	—	40	—	50	ns
t_{DDD}	Write Data Valid to Read Data Delay(1)	—	30	—	35	ns

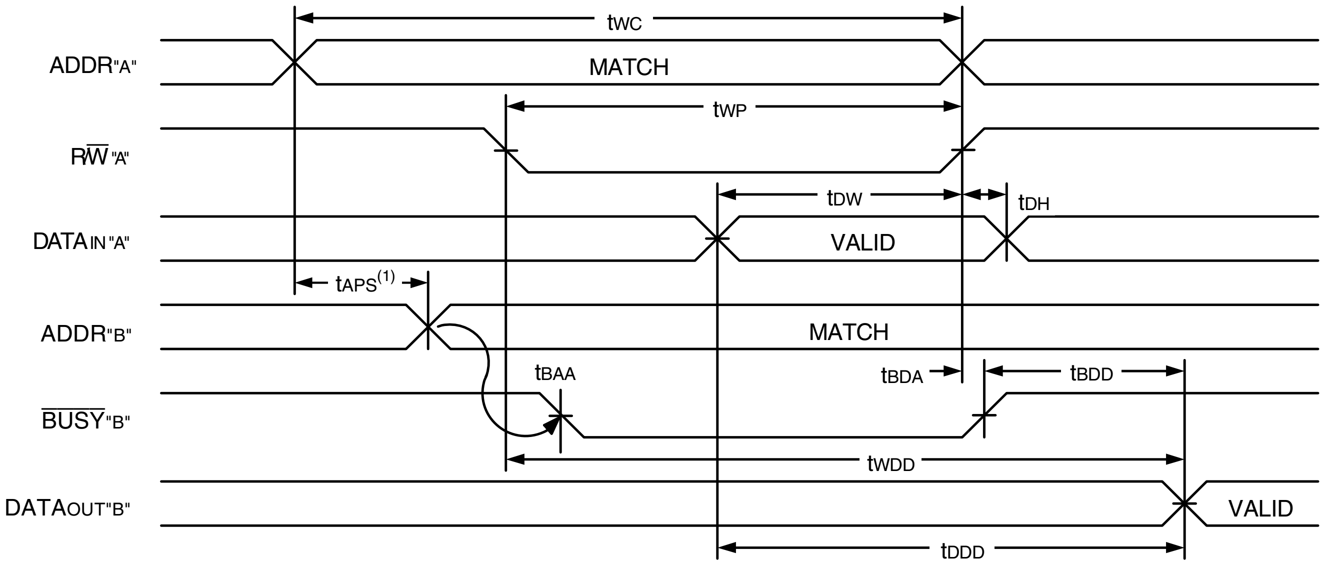
2691 tbl 10a

Symbol	Parameter	71321X35 71421X35 Com'l Only Min.	Max.	71321X55 71421X55 Com'l & Ind Min.	Max.	Unit
$\overline{BUSY}$ TIMING (For MASTER 71321)						
t_{BAA}	$\overline{BUSY}$ Access Time from Address	—	20	—	30	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address	—	20	—	30	ns
t_{BAC}	$\overline{BUSY}$ Access Time from Chip Enable	—	20	—	30	ns
t_{BDC}	$\overline{BUSY}$ Disable Time from Chip Enable	—	20	—	30	ns
t_{WH}	Write Hold After $\overline{BUSY}$(5)	20	—	20	—	ns
t_{WDD}	Write Pulse to Data Delay(1)	—	60	—	80	ns
t_{DDD}	Write Data Valid to Read Data Delay(1)	—	35	—	55	ns
t_{APS}	Arbitration Priority Set-up Time(2)	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data(3)	—	35	—	50	ns
$\overline{BUSY}$ INPUT TIMING (For SLAVE 71421)						
t_{WB}	Write to $\overline{BUSY}$ Input(4)	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$(5)	20	—	20	—	ns
t_{WDD}	Write Pulse to Data Delay(1)	—	60	—	80	ns
t_{DDD}	Write Data Valid to Read Data Delay(1)	—	35	—	55	ns

2691 tbl 10b

NOTES:
1. Port-to-port delay through RAM cells from the writing port to the reading port, refer to “Timing Waveform of Write with Port-to-Port Read and BUSY."
2. To ensure that the earlier of the two ports wins.
3. t_{BDD} is a calculated parameter and is the greater of 0, $t_{WDD} – t_{WP}$ (actual) or $t_{DDD} – t_{DW}$ (actual).
4. To ensure that a write cycle is inhibited on port "B" during contention on port "A".
5. To ensure that a write cycle is completed on port "B" after contention on port "A".
6. 'X' in part numbers indicates power rating (SA or LA)..

Timing Waveform of Write with Port-to-Port Read and $\overline{\text{BUSY}}$(2,3,4)



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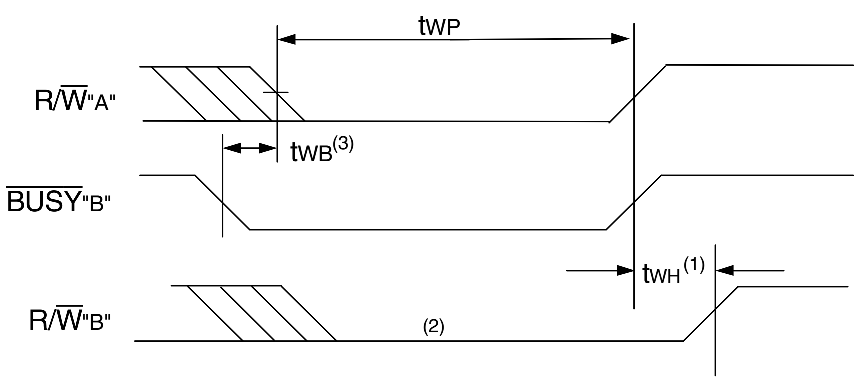
NOTES:
1. To ensure that the earlier of the two ports wins. tAPS is ignored for Slave (IDT71421).
2. $\overline{\text{CE}}$L = $\overline{\text{CE}}$R = VIL
3. $\overline{\text{OE}}$ = VIL for the reading port.
4. All timing is the same for the left and right ports. Port "A" may be either the left or right port. Port "B" is opposite from port "A".

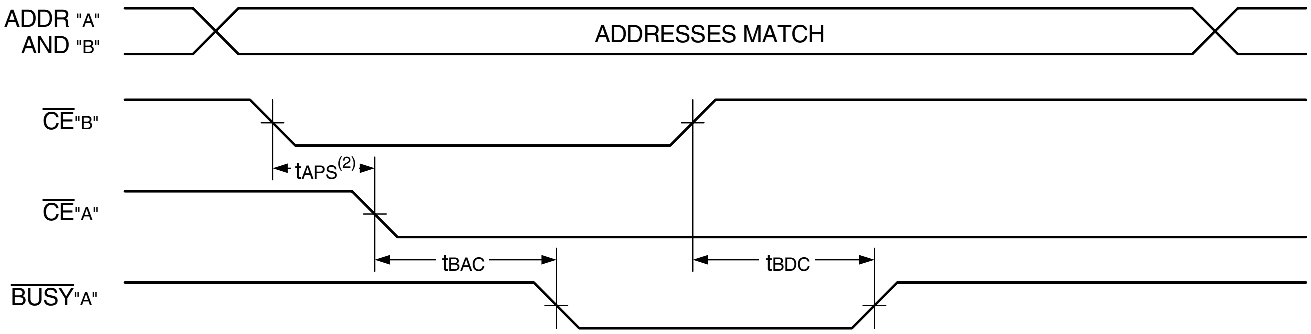
Timing Waveform of Write with $\overline{\text{BUSY}}$(4)



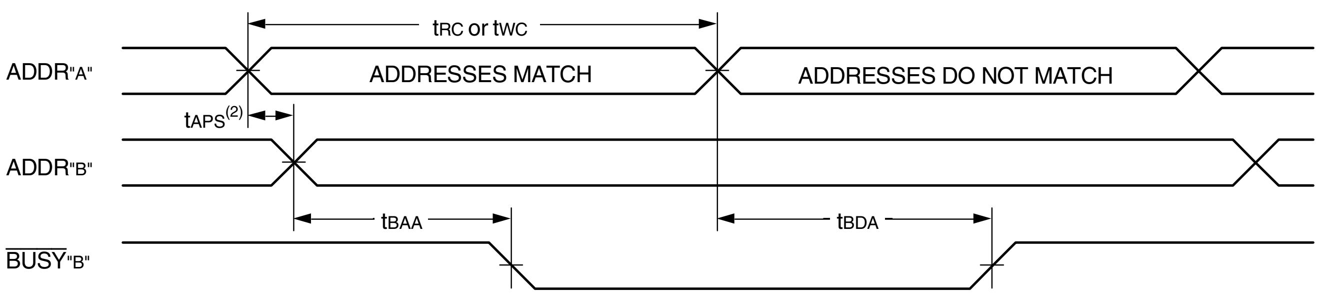
2691 drw 11

NOTES:
1. tWH must be met for both $\overline{\text{BUSY}}$ input (IDT71421, slave) or output (IDT71321, Master).
2. $\overline{\text{BUSY}}$ is asserted on port "B" blocking R/$\overline{\text{W}}$"B", until $\overline{\text{BUSY}}$"B" goes HIGH.
3. tWB is only for the slave version (IDT71421).
4. All timing is the same for the left and right ports. Port "A" may be either the left or right port. Port "B" is opposite from port "A".

Timing Waveform of $\overline{\text{BUSY}}$ Arbitration Controlled by $\overline{\text{CE}}$ Timing(1)



Timing Waveform of $\overline{\text{BUSY}}$ Arbitration Controlled by Address Match Timing(1)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
2. If t_{APS} is not satisfied, the $\overline{\text{BUSY}}$ will be asserted on one side or the other, but there is no guarantee on which side $\overline{\text{BUSY}}$ will be asserted (IDT71321 only).

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(1)

		71321X20 71421X20 Com'l Only		71321X25 71421X25 Com'l & Ind		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
INTERRUPT TIMING						
t_{AS}	Address Set-up Time	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	20	—	25	ns
t_{INR}	Interrupt Reset Time	—	20	—	25	ns

2691 tbl 11a

NOTE:
1. 'X' in part numbers indicates power rating (SA or LA).

AC Electrical Characteristics Over the Operating Temperature Supply Voltage Range(1)

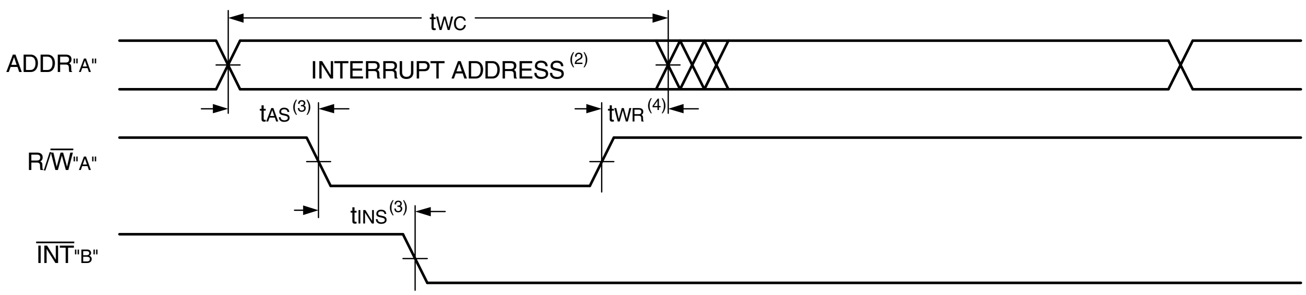
		71321X35 71421X35 Com'l Only		71321X55 71421X55 Com'l & Ind		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
INTERRUPT TIMING						
tAS	Address Set-up Time	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	ns
tINS	Interrupt Set Time	—	25	—	45	ns
tINR	Interrupt Reset Time	—	25	—	45	ns

2691 tbl 11b

NOTE:
1. 'X' in part numbers indicates power rating (SA or LA).

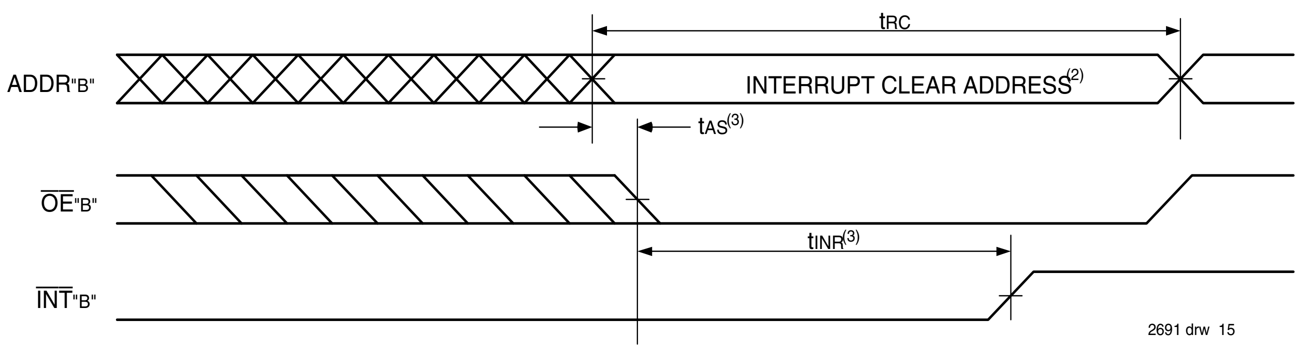
Timing Waveform of Interrupt Mode(1)

Set INT



2691 drw 14

Clear INT



2691 drw 15

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
2. See Interrupt Truth Table.
3. Timing depends on which enable signal (CE or R/W) is asserted last.
4. Timing depends on which enable signal (CE or R/W) is de-asserted first.

Truth Tables

Truth Table I. Non-Contention Read/Write Control[4]

Left or Right Port[1]				Function
$R/\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	
X	H	X	Z	Port Disabled and in Power-Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L = V_{IH}$, Power-Down Mode, I_{SB1} or I_{SB3}
L	L	X	$DATA_{IN}$	Data on Port Written Into Memory[2]
H	L	L	$DATA_{OUT}$	Data in Memory Output on Port[3]
H	L	H	Z	High Impedance Outputs

2691 tbl 12

NOTES:
1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$.
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. 'H' = V_{IH}, 'L' = V_{IL}, 'X' = DON'T CARE, 'Z' = HIGH IMPEDANCE

Truth Table II. Interrupt Flag[1,4]

Left Port					Right Port					Function
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{10L}-A_{0L}$	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{10R}-A_{0R}$	$\overline{INT}_R$	
L	L	X	7FF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	7FF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	7FE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	7FE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

2691 tbl 13

NOTES:
1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R = V_{IH}$
2. If $\overline{BUSY}_L = V_{IL}$, then No Change.
3. If $\overline{BUSY}_R = V_{IL}$, then No Change.
4. 'H' = HIGH, 'L' = LOW, 'X' = DON'T CARE

Truth Table III — Address $\overline{BUSY}$ Arbitration

Inputs			Outputs		Function
$\overline{CE}_L$	$\overline{CE}_R$	$A_{0L}-A_{10L}$ $A_{0R}-A_{10R}$	$\overline{BUSY}_L$[1]	$\overline{BUSY}_R$[1]	
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit[3]

2691 tbl 14

NOTES:
1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs for IDT71321 (Master). Both are inputs for IDT71421 (Slave). $\overline{BUSY}_X$ outputs on the IDT71321 are open drain, not push-pull outputs. On slaves the $\overline{BUSY}_X$ input internally inhibits writes.
2. 'L' if the inputs to the opposite port were stable prior to the address and enable inputs of this port. 'H' if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = LOW will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs can not be LOW simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving LOW regardless of actual logic level on the pin.

Functional Description

The IDT71321/IDT71421 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT71321/IDT71421 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE} = V_{IH}$). When a port is enabled, access to the entire memory array is permitted.

Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 7FE (HEX), where a write is defined as the $\overline{CE}_R = R/\overline{W}_R = V_{IL}$, per Truth Table II. The left port clears the interrupt by accessing address location 7FE when $\overline{CE}_L = \overline{OE}_L = V_{IL}$, R/W is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location 7FF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must access the memory location 7FF. The message (8 bits) at 7FE or 7FF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 7FE and 7FF are not used as mail boxes, but as part of the random access memory. Refer to Truth Table II for the interrupt operation.

Busy Logic

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "Busy". The $\overline{BUSY}$ pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of $\overline{BUSY}$ Logic is not required or desirable for all applications. In some cases it may be useful to logically OR the $\overline{BUSY}$ outputs together and use any $\overline{BUSY}$ indication as an interrupt source to flag the event of an illegal or illogical operation. In slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins HIGH. If desired, unintended write operations can be prevented to a port by tying the $\overline{BUSY}$ pin for that port LOW.

The $\overline{BUSY}$ outputs on the IDT71321 (Master) are open drain type outputs and require open drain resistors to operate. If these SRAMs are being expanded in depth, then the $\overline{BUSY}$ indication for the resulting array does not require the use of an external AND gate.

Width Expansion with Busy Logic Master/Slave Arrays

When expanding an SRAM array in width while using $\overline{BUSY}$ logic, one master part is used to decide which side of the SRAM array will receive a $\overline{BUSY}$ indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the $\overline{BUSY}$ signal as a write inhibit signal. Thus on the IDT71321/IDT71421 SRAMs the $\overline{BUSY}$ pin is an output if the part is Master (IDT71321), and the $\overline{BUSY}$ pin is an input if the part is a Slave (IDT71421) as shown in Figure 3.

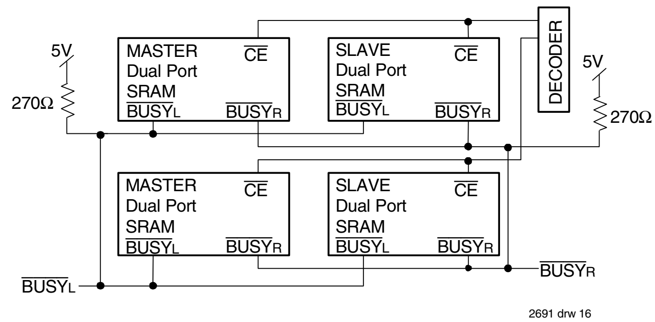


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT71321 (Master) and (Slave) IDT71421 SRAMs.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating $\overline{BUSY}$ on one side of the array and another master indicating $\overline{BUSY}$ on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The $\overline{BUSY}$ arbitration, on a Master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a $\overline{BUSY}$ flag to be output from the master before the actual write pulse can be initiated with either the R/$\overline{W}$ signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

Ordering Information

XXXX	A	999	A	A	A	A
Device Type	Power	Speed	Package		Process/ Temperature Range	

(last A)	Blank	Tube or Tray
	8	Tape and Reel
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	I(1)	Industrial (-40°C to +85°C)
(A)	G	Green
Package	J	52-pin PLCC (PLG52)
	PF	64-pin TQFP (PNG64)
	PP	52-pin STQFP (PPG52)
	TF	64-pin STQFP (PPG64)
Speed (Speed in nanoseconds)	20	Commercial Only
	25	Industrial Only
	35	Commercial Only
	55	Commercial & Industrial
Power	LA	Low Power
	SA	Standard Power
Device Type	71321	16K (2K x 8-Bit) MASTER Dual-Port SRAM w/ Interrupt
	71421	16K (2K x 8-Bit) SLAVE Dual-Port SRAM w/ Interrupt

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NOTES:
1. Contact your sales office for industrial temperature range availability in other speeds, packages and powers.
   LEAD FINISH (SnPb) parts are Obsolete. Product Discontinuation Notice - PDN# SP-17-02
   Note that information regarding recently obsoleted parts are included in this datasheet for customer convenience.

Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
20	71321LA20JG	PLG52	PLCC	C
	71321LA20JG8	PLG52	PLCC	C
	71321LA20PFG	PNG64	TQFP	C
	71321LA20PFG8	PNG64	TQFP	C
	71321LA20TFG	PPG64	TQFP	C
	71321LA20TFG8	PPG64	TQFP	C
25	71321LA25JGI	PLG52	PLCC	I
	71321LA25JGI8	PLG52	PLCC	I
	71321LA25PFGI	PNG64	TQFP	I
	71321LA25PFGI8	PNG64	TQFP	I
	71321LA25TFGI	PPG64	TQFP	I
	71321LA25TFGI8	PPG64	TQFP	I
55	71321LA55PPGI	PPG52	TQFP	I
	71321LA55PPGI8	PPG52	TQFP	I
	71321LA55TFG	PPG64	TQFP	C
	71321LA55TFG8	PPG64	TQFP	C

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
35	71321SA35TFG	PPG64	TQFP	C
	71321SA35TFG8	PPG64	TQFP	C
55	71321SA55JG	PLG52	PLCC	C
	71321SA55JG8	PLG52	PLCC	C

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
20	71421LA20JG	PLG52	PLCC	C
	71421LA20JG8	PLG52	PLCC	C
	71421LA20PFG	PNG64	TQFP	C
	71421LA20PFG8	PNG64	TQFP	C
25	71421LA25PFGI	PNG64	TQFP	I
	71421LA25PFGI8	PNG64	TQFP	I

Datasheet Document History

03/24/99:		Initiated datasheet document history
		Converted to new format
		Cosmetic typographical corrections
	Pages 2 & 3	Added additional notes to pin configurations
06/07/99:		Changed drawing format
11/10/99:		Replaced IDT logo
08/23/01:	Page 3	Increased storage temperature parameters
		Clarified T_A parameter
	Page 4	DC Electrical parameters–changed wording from "open" to "disabled"
	Page 16	Fixed part numbers in "Width Expansion" paragraph
		Changed ±500mV to 0mV in notes
	Page 4	Industrial temperature range offering added to DC Electrical Characteristics for 25ns and removed for 35ns
	Page 7 & 9	Industrial temperature range added to AC Electrical Characteristics for 25ns
	Page 17	Industrial offering removed for 35ns ordering information
01/17/06:	Page 1	Added green availability to features
	Page 17	Added green indicator to ordering information
	Page 1 & 17	Replaced old IDT™ with new IDT™ logo
08/25/06:	Page 14	Changed $\overline{INT}$"A" to $\overline{INT}$"B" in the CLEAR $\overline{INT}$ drawing in the Timing Waveform of Interrupt Mode
10/29/08:	Page 17	Removed "IDT" from orderable part number
09/10/12:	Page 1 & 2	52-pin STQFP added to the features and description
	Page 3	PP52-1 pin configuration added
	Page 9	Typo corrected
	Page 17	Added T&R indicator and PP52-1 package information to the ordering information
06/10/16:	Page 2	Changed diagram for the J52 pin configuration by rotating package pin labels and pin numbers 90 degrees clockwise to reflect pin1 orientation and added pin 1 dot at pin 1
		Removed J52 chamfers and aligned the top and bottom pin labels in the standard direction
		Changed diagram for the PN64/PP64 pin configuration by rotating package pin labels and pin numbers 90 degrees counter clockwise to reflect pin 1 orientation and added pin 1 dot at pin 1
	Page 3	PP52 pin configuration. Added the IDT logo, changed the text to be in alignment with new diagram marking specs
		Removed footnote 5 and its references
	Pages 2 & 17	In pin configuration footnotes and in the Ordering Information: The package codes J52-1, PN64-1, PP64-1 and PP52-1 changed to J52, PN64, PP64 & PP52 respectively to match standard package codes
02/20/18:		Product Discontinuation Notice - PDN# SP-17-02
		Last time buy expires June 15, 2018
09/24/19:	Pages 1 & 17	Deleted obsolete Commercial 25ns speed grade
	Pages 2 & 3	Updated package codes
	Page 3	Rotated PPG52 STQFP pin configuration to accurately reflect pin 1 orientation
	Page 5	Typo corrected in the Data Retention Characteristics table 06
	Page 17	Added Orderable Part Information

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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