FUJITSU SEMICONDUCTOR
MEMORY SOLUTION DATA SHEET

DS501-00011-9v1-E

Memory FeRAM

256 K (32 K × 8) Bit

MB85R256F

■ DESCRIPTIONS

The MB85R256F is an FeRAM (Ferroelectric Random Access Memory) chip in a configuration of 32,768 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.

The MB85R256F is able to retain data without using a back-up battery, as is needed for SRAM.

The memory cells used in the MB85R256F can be used for 10^{12} read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E^2PROM.

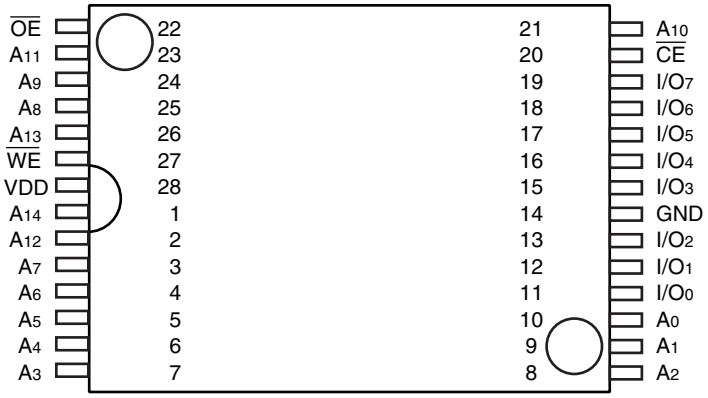
The MB85R256F uses a pseudo - SRAM interface.

■ FEATURES

- Bit configuration : 32,768 words × 8 bits
- Read/write endurance : 10^{12} times / byte
- Data retention : 10 years (+ 85 °C), 95 years (+ 55 °C), over 200 years (+ 35 °C)
- Operating power supply voltage : 2.7 V to 3.6 V
- Low power consumption : Operating power supply current 5 mA (Typ)
  Standby current 5 μA (Typ)
- Operation ambient temperature range: − 40 °C to + 85 °C
- Package : 28-pin plastic TSOP
  RoHS compliant

2023.06

■ PIN ASSIGNMENTS

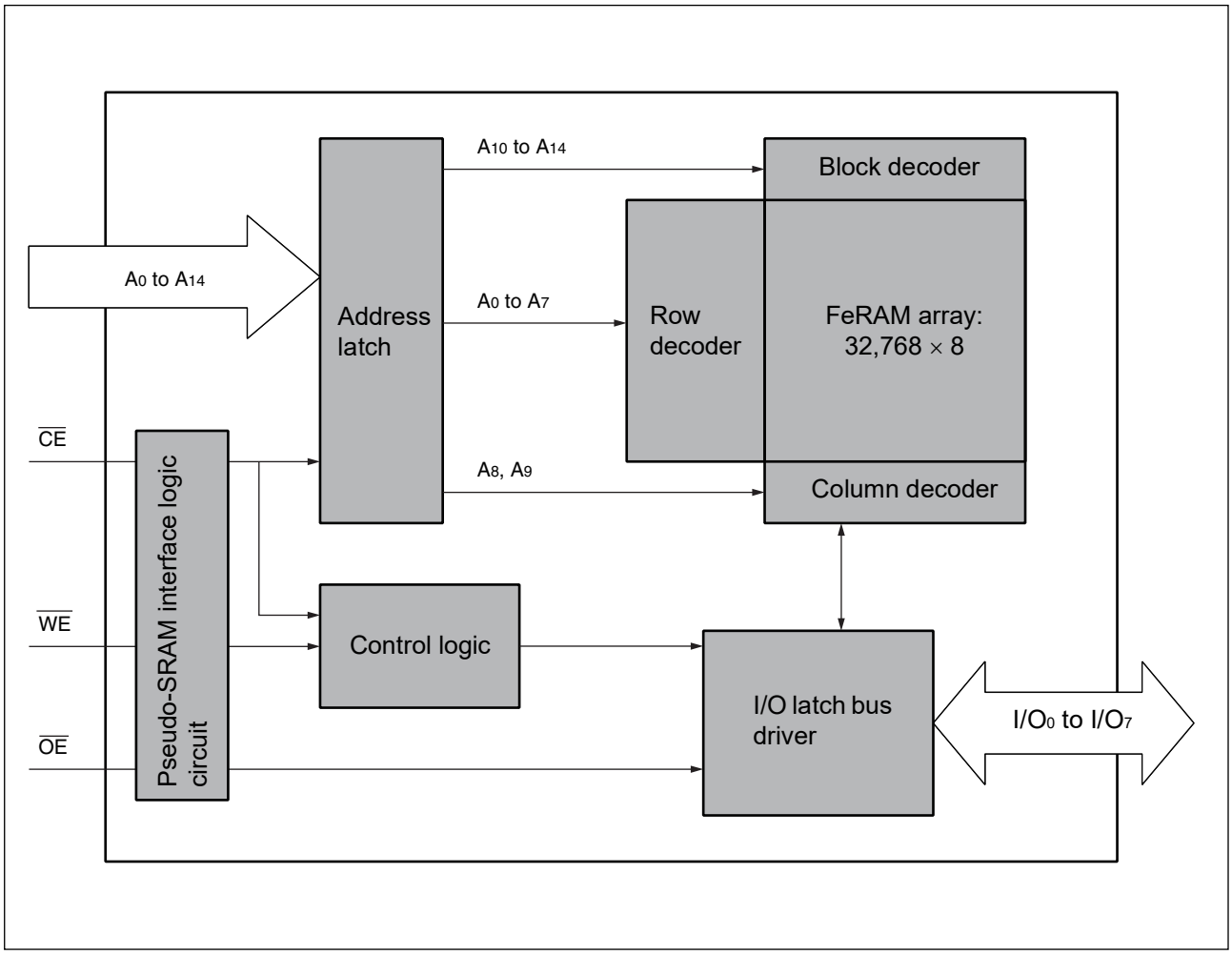


(28-pin plastic TSOP)

■ PIN FUNCTIONAL DESCRIPTIONS

Pin no.	Pin name	Functional description
1 to 10, 21, 23 to 26	A_0 to A_{14}	Address input pins
11 to 13, 15 to 19	I/O_0 to I/O_7	Data input/output pins
20	$\overline{CE}$	Chip enable input pin
27	$\overline{WE}$	Write Enable input pin
22	$\overline{OE}$	Output enable input pin
28	VDD	Supply Voltage pin
14	GND	Ground pin

■ BLOCK DIAGRAM



■ FUNCTION LIST

Operation mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O0 to I/O7	Power supply current
Standby precharge	H	×	×	Hi-Z	Standby (I_{SB})
	×	L	L		
	×	H	H		
Latch address	L	↓	↓	—	—
	↓	H	L		
	↓	L	H		
Write	L	L	H	Data input	Operation (I_{DD})
Read	L	H	L	Data output	

H: High level, L: Low level, × : can be either H, L, ↓ or ↑, Hi-Z: High impedance, ↓ : Latch address at falling edge

■ ABSOLUTE MAXIMUM RANGES

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	− 0.5	+ 4.0	V
Input voltage*	V_{IN}	− 0.5	V_{DD} + 0.5	V
Output voltage*	V_{OUT}	− 0.5	V_{DD} + 0.5	V
Operation ambient temperature	T_A	− 40	+ 85	°C
Storage temperature	Tstg	− 55	+ 125	°C

* : These parameters are based on the condition that V_{SS} is 0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage*1	V_{DD}	2.7	3.3	3.6	V
Operation ambient temperature*2	T_A	− 40	—	+ 85	°C

*1 : These parameters are based on the condition that V_{SS} is 0 V.

*2 : Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{DD}	—	—	10	μA
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{DD}, $\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}	—	—	10	μA
Operating power supply current*1	I_{DD}	$\overline{CE}$ = 0.2 V, Other inputs = V_{DD} − 0.2 V/0.2 V, t_{RC} (Min), Iout = 0 mA	—	5	10	mA
Standby current*2	I_{SB}	$\overline{CE}$, $\overline{WE}$, $\overline{OE}$ ≥ V_{DD}	—	5	50	μA
High level input voltage	V_{IH}	V_{DD} = 2.7 V to 3.6 V	V_{DD} × 0.8	—	V_{DD} + 0.5 (≤ 4.0)	V
Low level input voltage	V_{IL}	V_{DD} = 2.7 V to 3.6 V	− 0.5	—	+ 0.6	V
High level output voltage	V_{OH}	I_{OH} = − 2.0 mA	V_{DD} × 0.8	—	—	V
Low level output voltage	V_{OL}	I_{OL} = 2.0 mA	—	—	0.4	V

*1: During the measurement of I_{DD}, the Address and Data In were taken to only change once per active cycle. Iout: output current

*2: All pins other than setting pins shall be input at the CMOS level voltages such as H ≥ V_{DD}, L ≤ 0 V.

2. AC Characteristics

• AC Characteristics Test Condition

Power supply voltage : 2.7 V to 3.6 V

Operation ambient temperature: − 40 °C to + 85 °C

Input voltage amplitude : 0.3 V to 2.7 V

Input rising time : 10 ns

Input falling time : 10 ns

Input evaluation level : $V_{DD}/2$

Output evaluation level : $V_{DD}/2$

Output Load Capacitance: 100 pF

(1) Read cycle

Parameter	Symbol	Value		Unit
		Min	Max	
Read cycle time	t_{RC}	150	—	ns
$\overline{CE}$ active time	t_{CA}	70	500	
Read pulse width	t_{RP}	70	500	
Precharge time	t_{PC}	80	—	
Address setup time	t_{AS}	0	—	
Address hold time	t_{AH}	25	—	
$\overline{CE}$ access time	t_{CE}	—	70	
$\overline{OE}$ access time	t_{OE}	—	70	
$\overline{CE}$ output floating time	t_{HZ}	—	25	
$\overline{OE}$ output floating time	t_{OHZ}	—	25	

(2) Write cycle

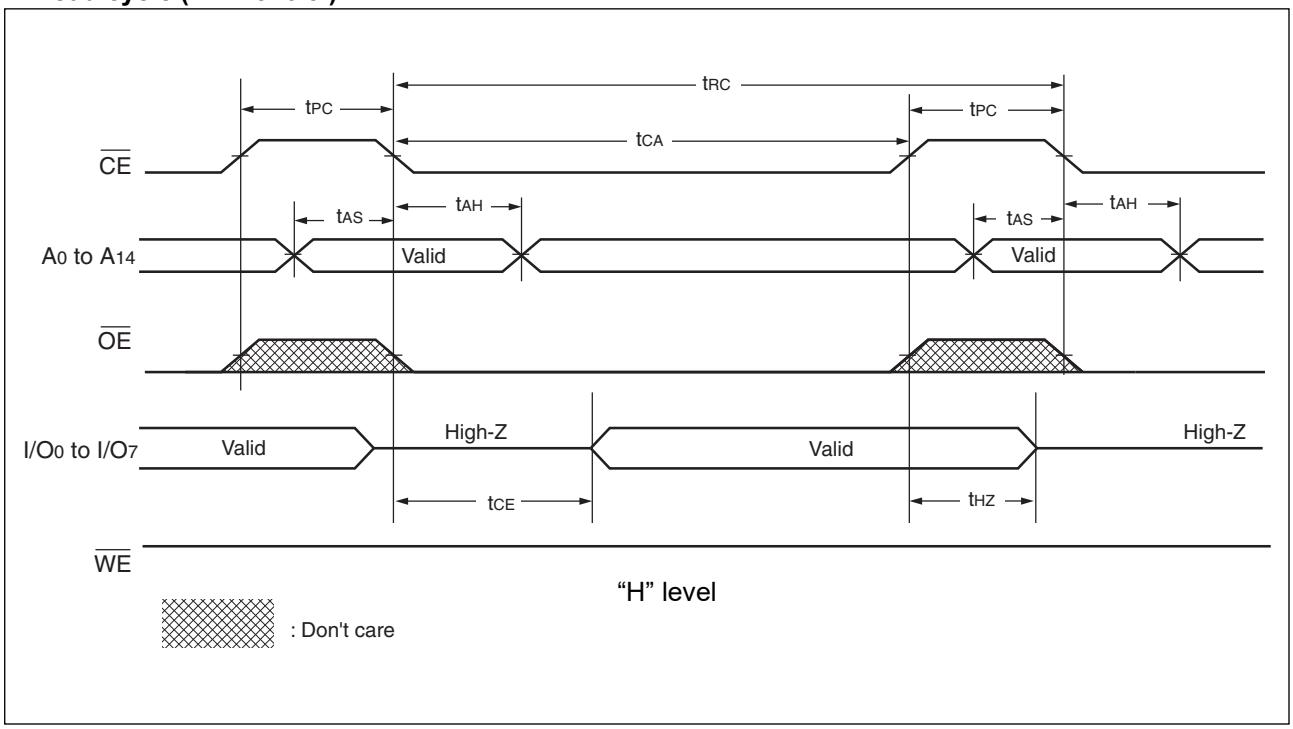
Parameter	Symbol	Value		Unit
		Min	Max	
Write cycle time	t_{WC}	150	—	ns
$\overline{CE}$ active time	t_{CA}	70	500	
Write pulse width	t_{WP}	70	500	
Precharge time	t_{PC}	80	—	
Address setup time	t_{AS}	0	—	
Address hold time	t_{AH}	25	—	
Data setup time	t_{DS}	50	—	
Data hold time	t_{DH}	0	—	

3. Pin Capacitance

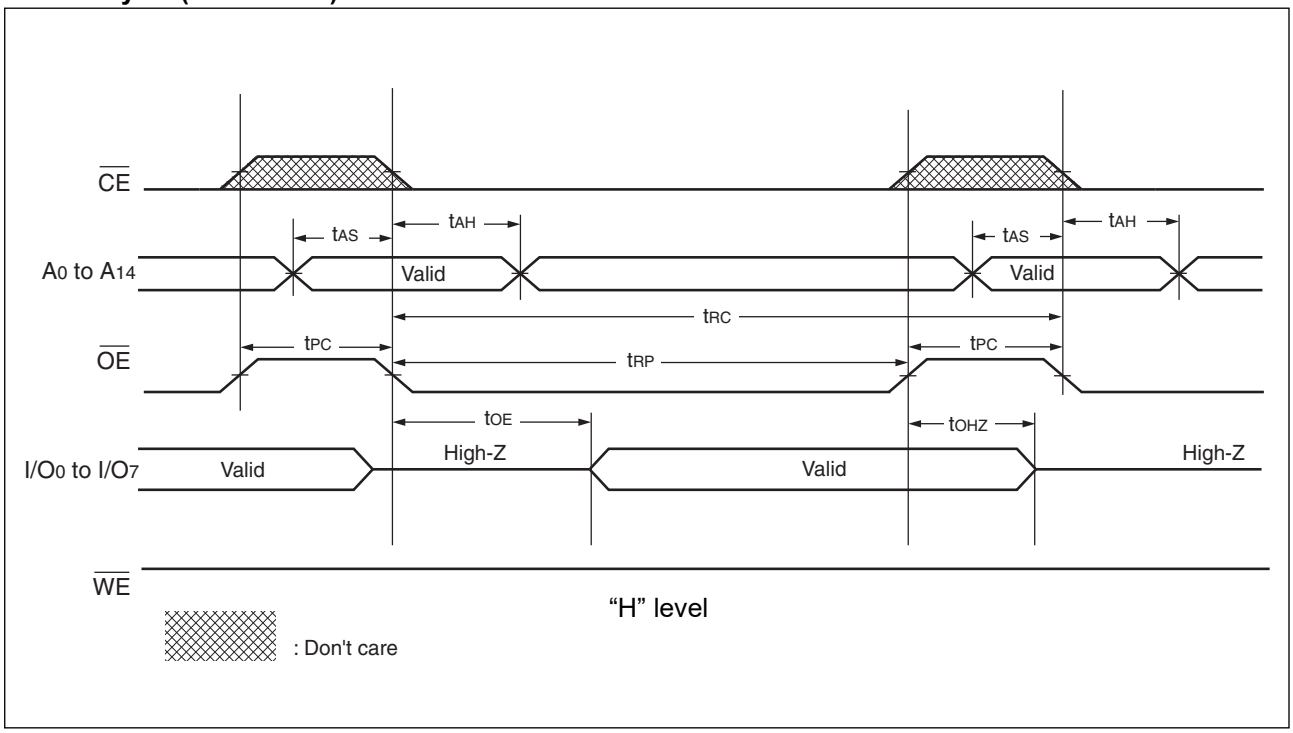
Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Input capacitance	C_{IN}	$V_{DD} = V_{IN} = V_{OUT} = 0$ V, f = 1 MHz, $T_A = +25$ °C	—	—	10	pF
Output capacitance	C_{OUT}		—	—	10	pF

■ TIMING DIAGRAM

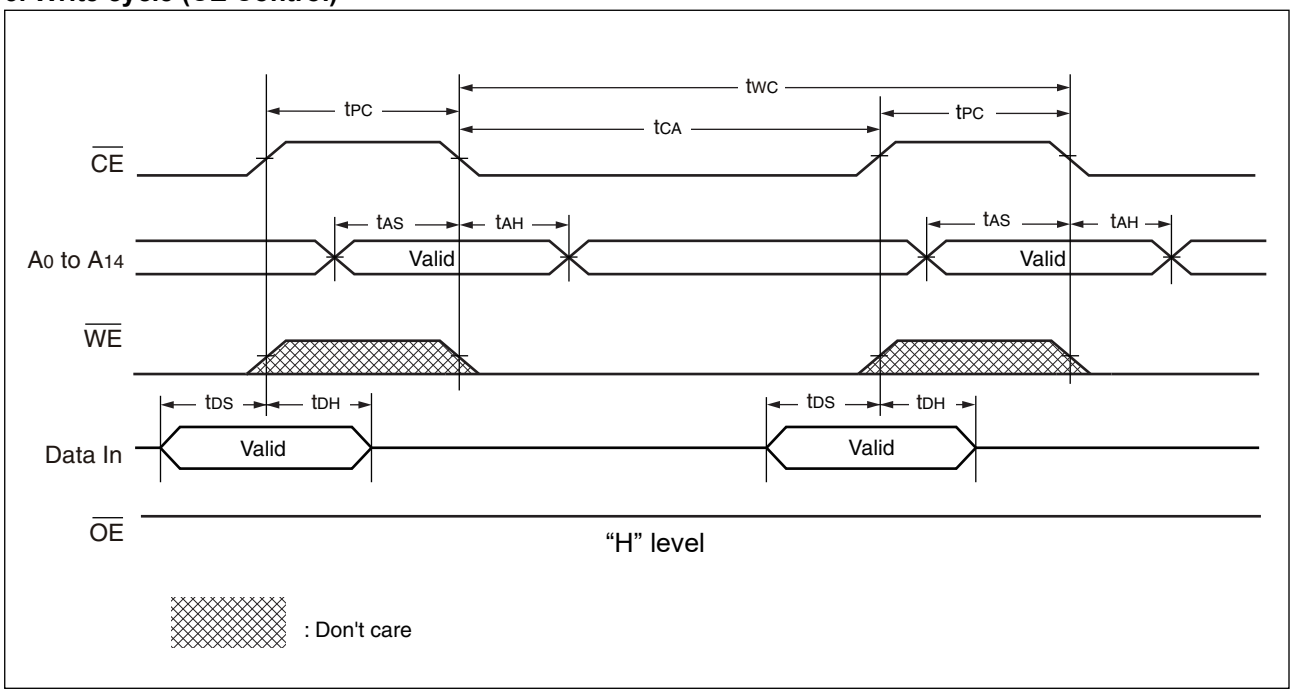
1. Read cycle ($\overline{CE}$ Control)



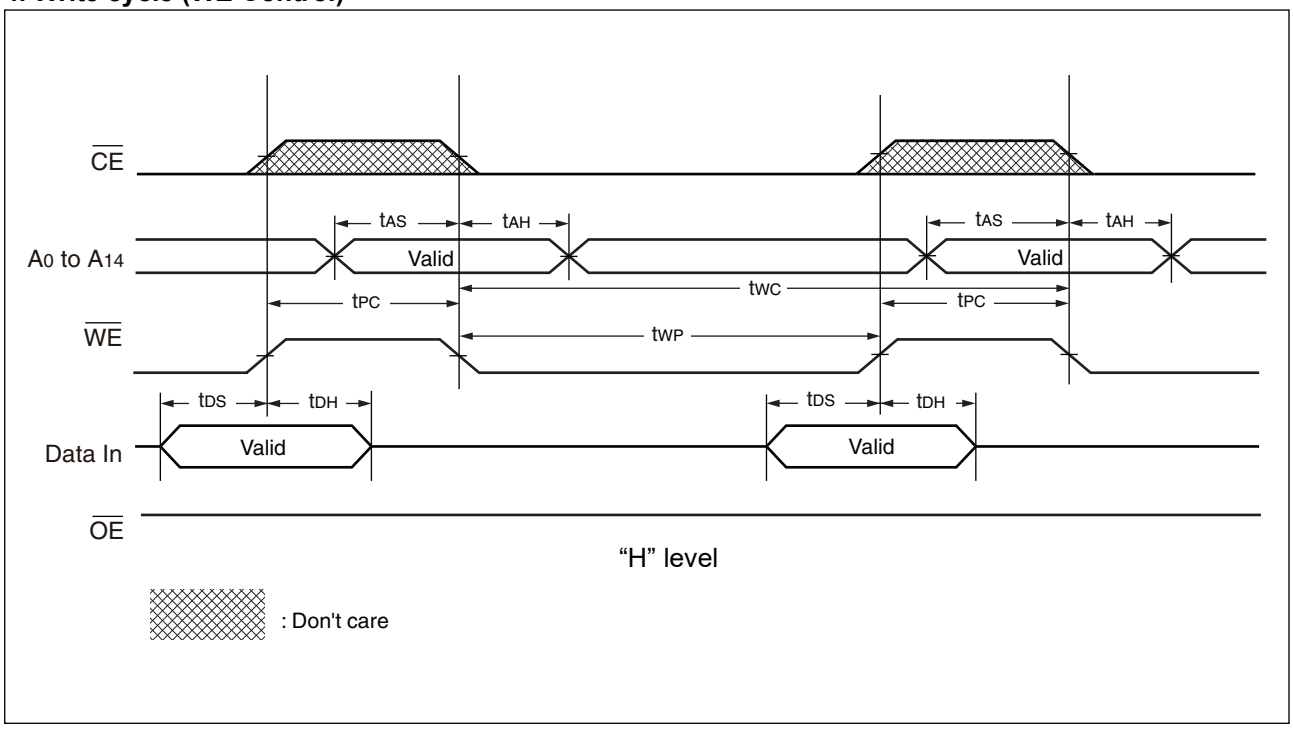
2. Read cycle ($\overline{OE}$ Control)



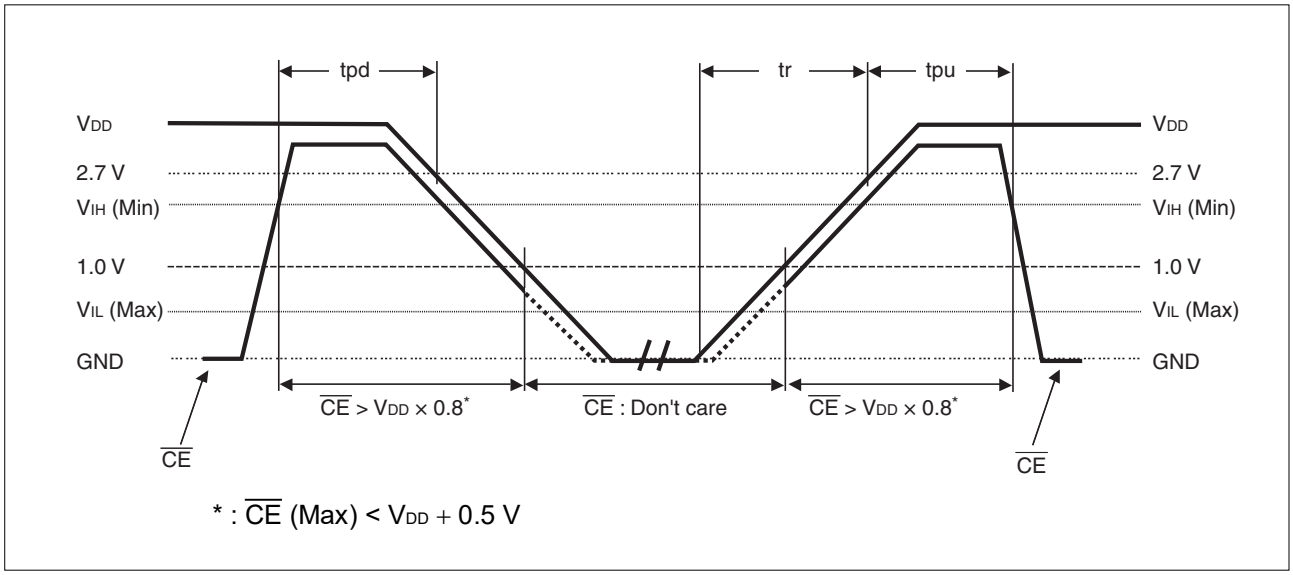
3. Write cycle ($\overline{CE}$ Control)



4. Write cycle ($\overline{WE}$ Control)



■ POWER ON/OFF SEQUENCE



Parameter	Symbol	Value			Unit
		Min	Typ	Max	
$\overline{CE}$ level hold time at power OFF	tpd	80	—	—	ns
$\overline{CE}$ level hold time at power ON	tpu	80	—	—	ns
Power supply rising time	tr	0.05	—	200	ms

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

■ FeRAM CHARACTERISTICS

Item	Min	Max	Unit	Parameter
Read/Write Endurance*1	10^{12}	—	Times/byte	Operation Ambient Temperature T_A = + 85 °C
Data Retention*2	10	—	Years	Operation Ambient Temperature T_A = + 85 °C
	95	—		Operation Ambient Temperature T_A = + 55 °C
	≥ 200	—		Operation Ambient Temperature T_A = + 35 °C

*1 : Total number of reading and writing defines the minimum value of endurance, as an FeRAM memory operates with destructive readout mechanism.

*2 : Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

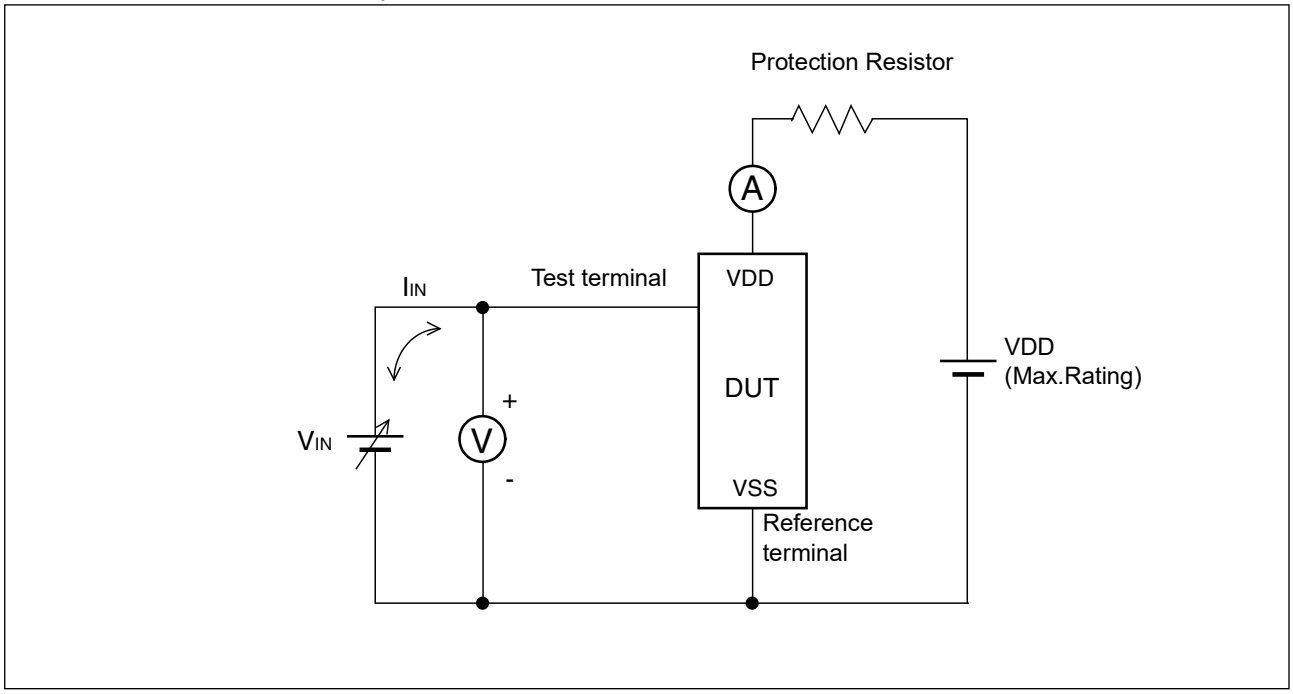
■ NOTES ON USE

We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.

■ ESD AND LATCH-UP

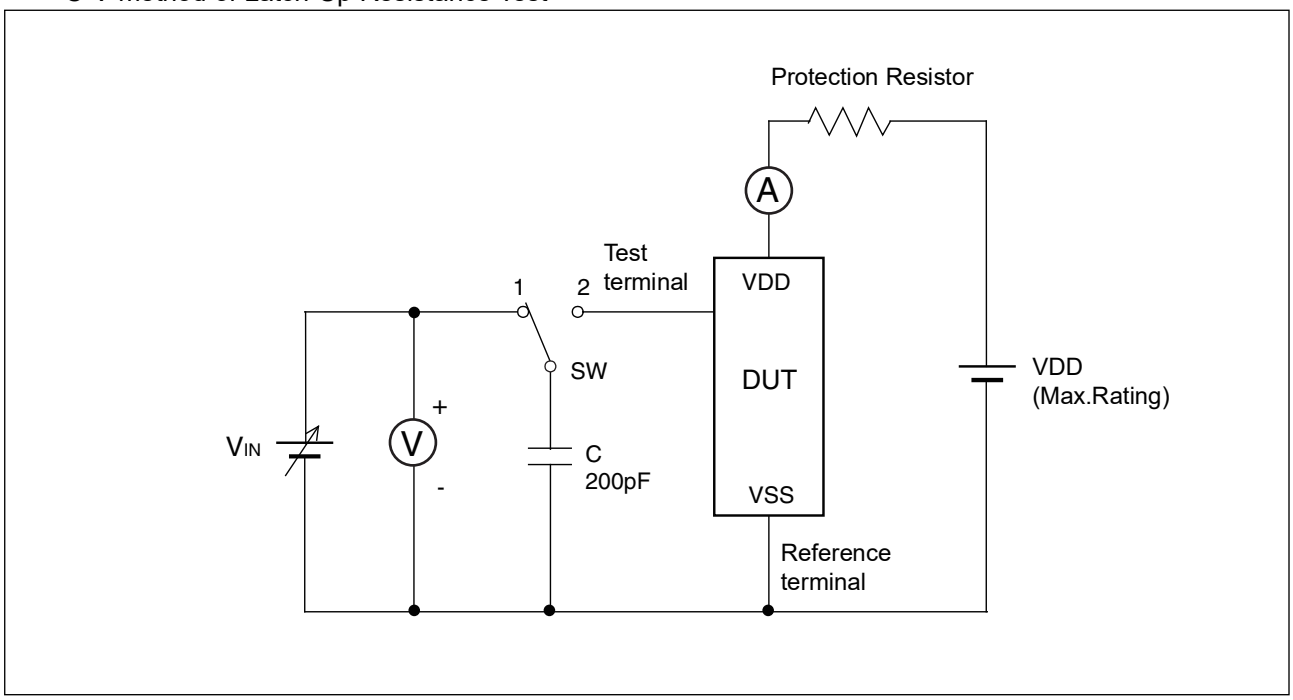
Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant	MB85R256FPFCN-G-BNDE1	≥ |2000 V|
ESD MM (Machine Model) JESD22-A115 compliant		≥ |200 V|
ESD CDM (Charged Device Model) JESD22-C101 compliant		≥ |1000 V|
Latch-Up (I-test) JESD78 compliant		—
Latch-Up (V_{supply} overvoltage test) JESD78 compliant		—
Latch-Up (Current Method) Proprietary method		≥ |300 mA|
Latch-Up (C-V Method) Proprietary method		—

- Current method of Latch-Up Resistance Test



Note : The voltage V_{IN} is increased gradually and the current I_{IN} of 300 mA at maximum shall flow.
Confirm the latch up does not occur under I_{IN} = ± 300 mA.
In case the specific requirement is specified for I/O and I_{IN} cannot be 300 mA, the voltage shall be increased to the level that meets the specific requirement.

• C-V method of Latch-Up Resistance Test



Note : Charge voltage alternately switching 1 and 2 approximately 2 sec interval. This switching process is considered as one cycle.
Repeat this process 5 times. However, if the latch-up condition occurs before completing 5 times, this test must be stopped immediately.

■ REFLOW CONDITIONS AND FLOOR LIFE

[JEDEC MSL] : Moisture Sensitivity Level 3 (IPC/JEDEC J-STD-020E)

■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

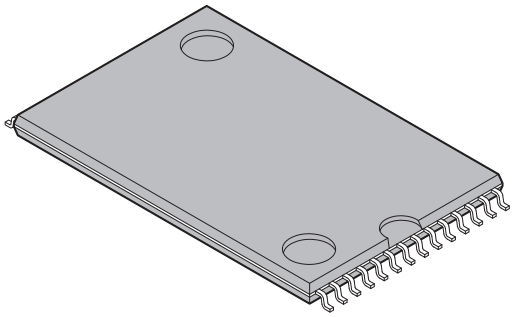
This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

■ ORDERING INFORMATION

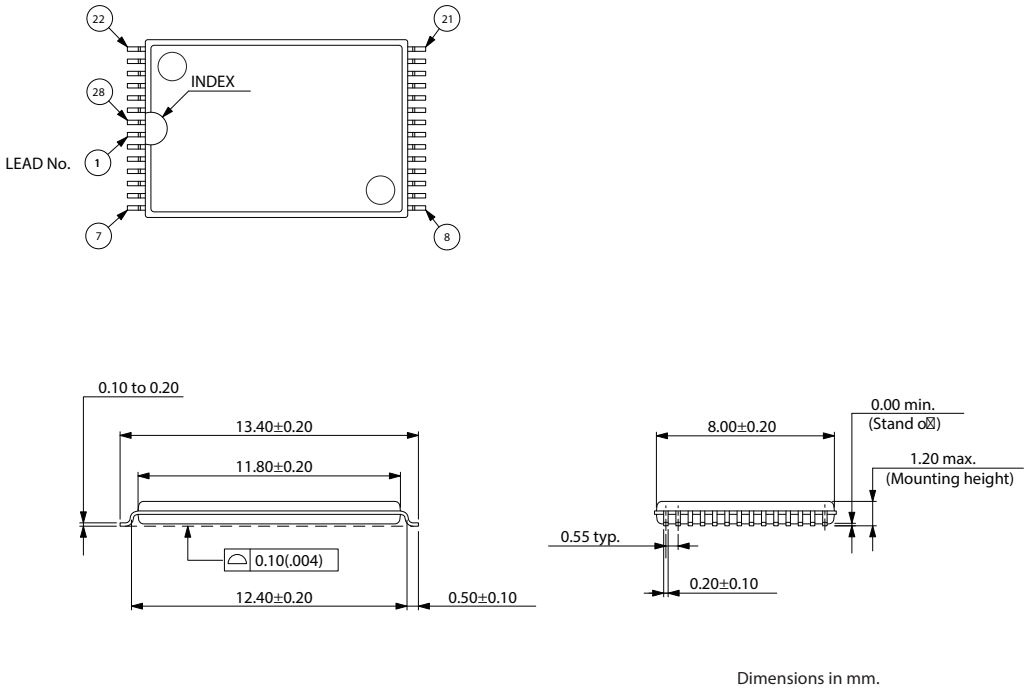
Part number	Package	Shipping form	Minimum shipping quantity
MB85R256FPFCN-G-BNDE1	28-pin plastic TSOP	Tray	—*

*: Please contact our sales office about minimum shipping quantity.

■ PACKAGE DIMENSION

28-pin plastic TSOP		
	Lead pitch	0.55 mm
	Package width × package length	11.80 × 8.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.20 mm Max

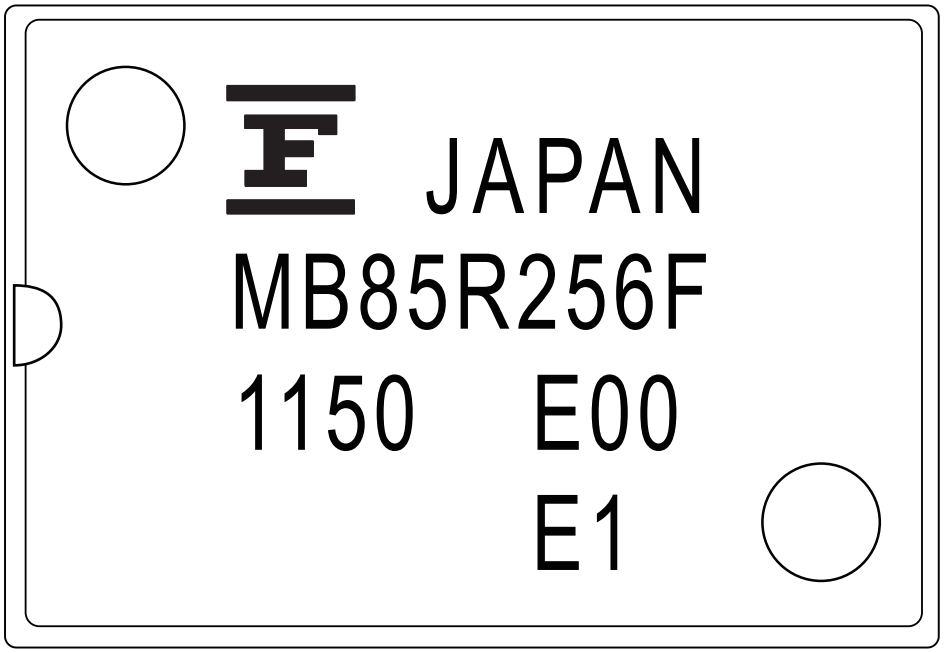
28-pin plastic TSOP

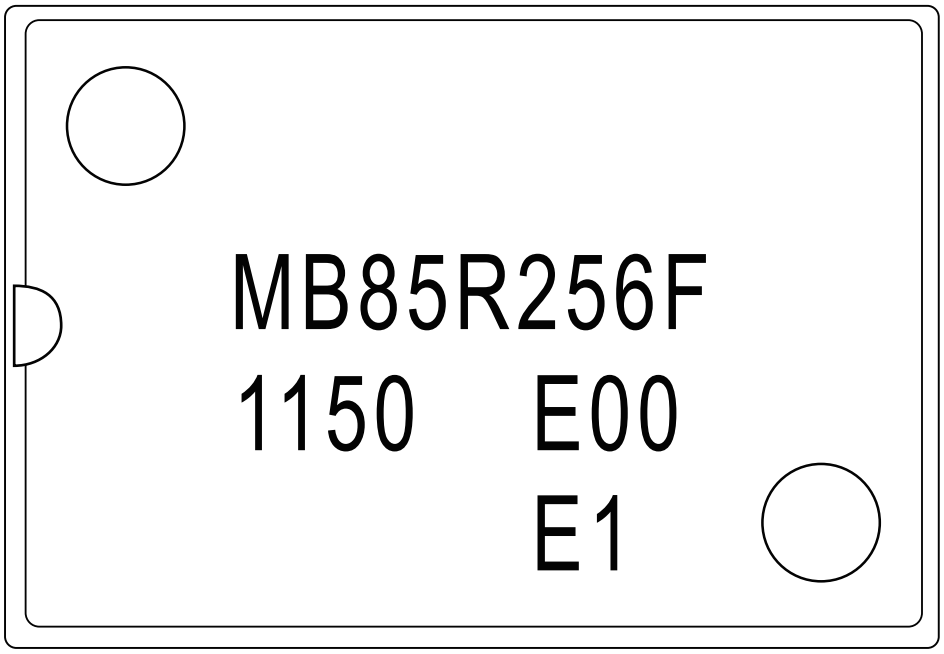


Dimensions in mm.

■ MARKING(Example)

[MB85R256FPFCN-G-BNDE1]





[TSOP 28]

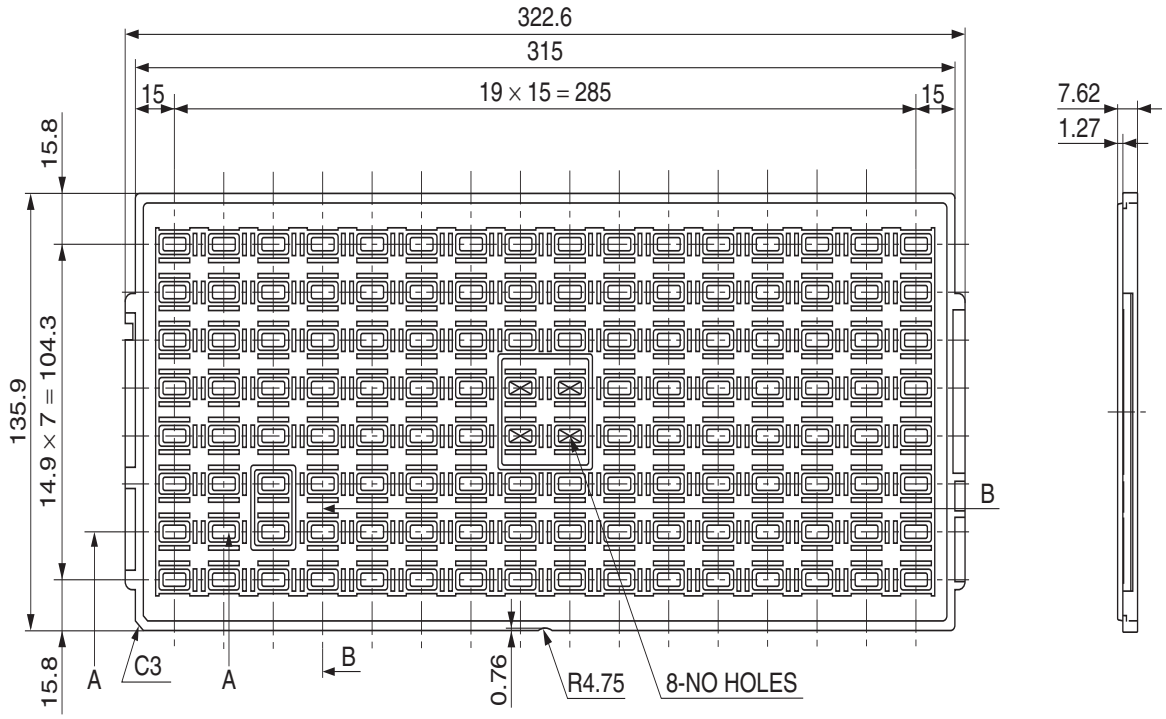
■ PACKING INFORMATION

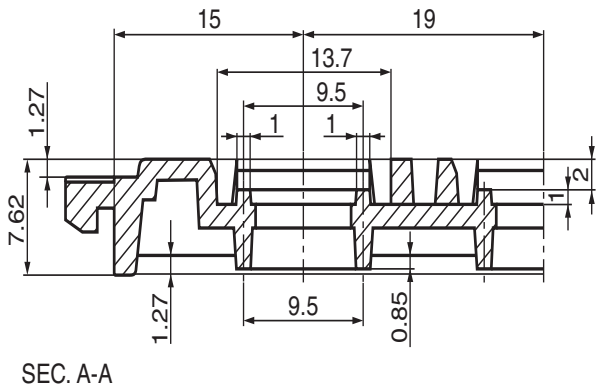
1. Tray

1.1 Tray Dimensions

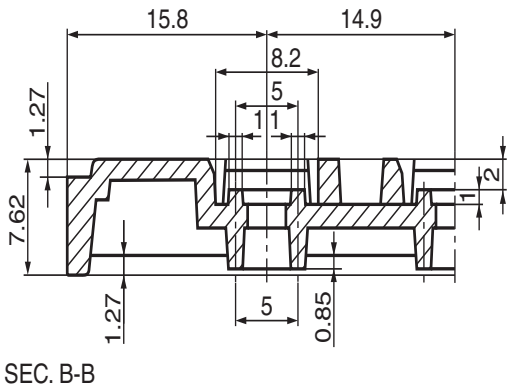
TSOP28

Maximum storage capacity		
pcs/tray	pcs/inner box	pcs/outer box
128	1280	5120





SEC. A-A

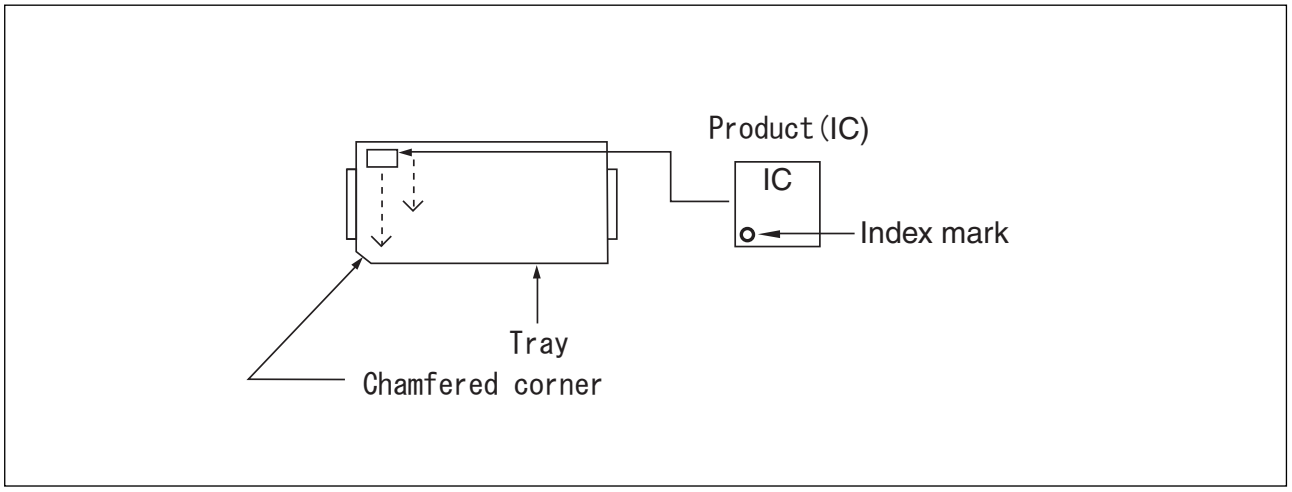


SEC. B-B

(Dimensions in mm)

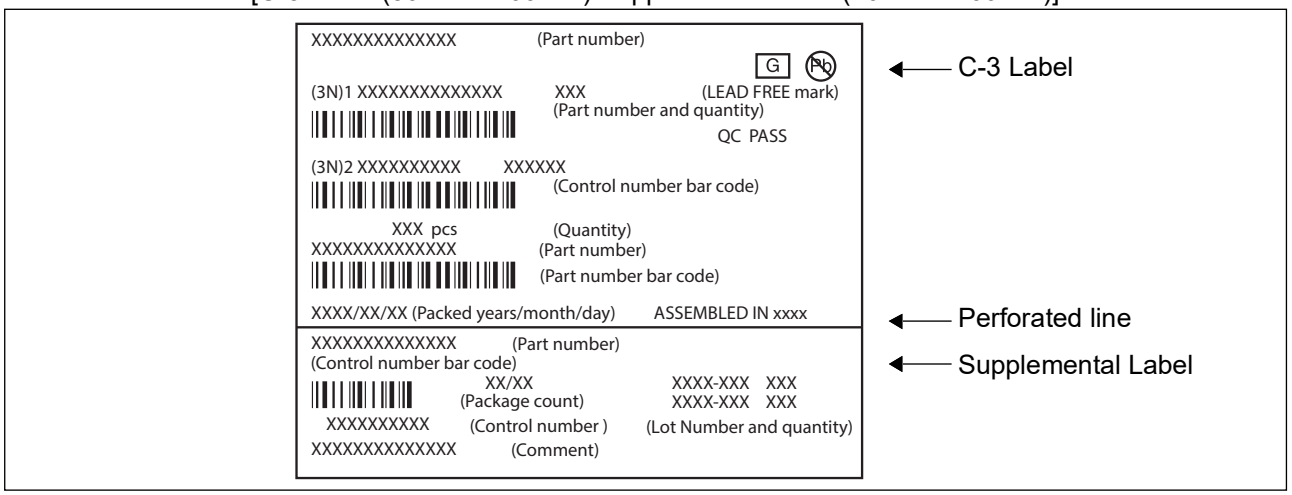
Heat proof temperature : 150 °C Max

1.2 IC orientation



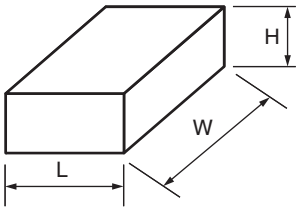
1.3 Product label indicators(example)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]



1.4 Dimensions for Containers

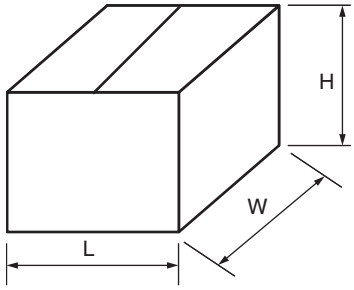
(1) Dimensions for inner box



L	W	H
165	360	75

(Dimensions in mm)

(2) Dimensions for outer box



L	W	H
355	385	195

(Dimensions in mm)

■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

Page	Section	Change Results
15	MARKING	New making format is added.

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