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TFT | OLED | CHARACTER | GRAPHIC | UWVD | SEGMENT | CUSTOM

Graphic Display Module

Part Number:
G240160A-FTW-DW63

Overview:

- 240x160 Graphic LCD
- FSTN Gray Positive
- 71x52 mm Module
- 8-bit 8080 parallel input from MPU Interface(s)
- White LED Backlight
- Transflective
- Wide Temp Range
- 3.3 V
- LCD IC: ST7586S
- RoHS Compliant.

Graphic LCD Features

Resolution: 240x160 Dots
Interface(s): 8-bit 8080 parallel input from MPU
RoHS Compliant.

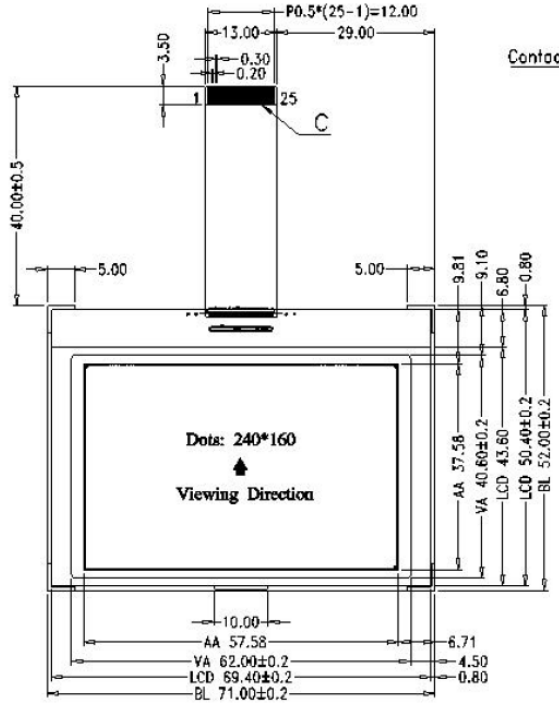
General Information Items	Specification	Unit	Note
	Main Panel		
Viewing Area (VA)	62.0 (H) x 40.6 (V)	mm	--
LCD Type	FSTN Positive	--	--
Viewing Angle	6:00	O'Clock	--
Polarizer	Transflective	--	--
Backlight Type	LED	--	--
Backlight Color	White	mm	--
LCD IC	ST7586S	--	--
Drive Mode	1/160 Duty, 1/12 Bias	--	--
Operating Temperature	-20 to +70	°C	--
Storage Temperature	-30 to +80	°C	--

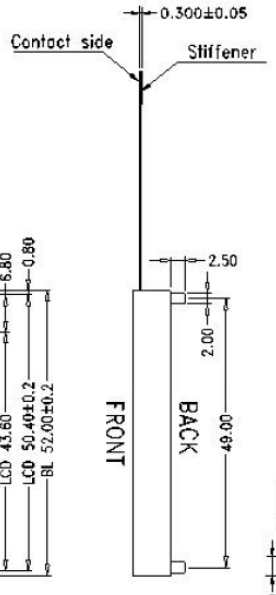
Mechanical Information

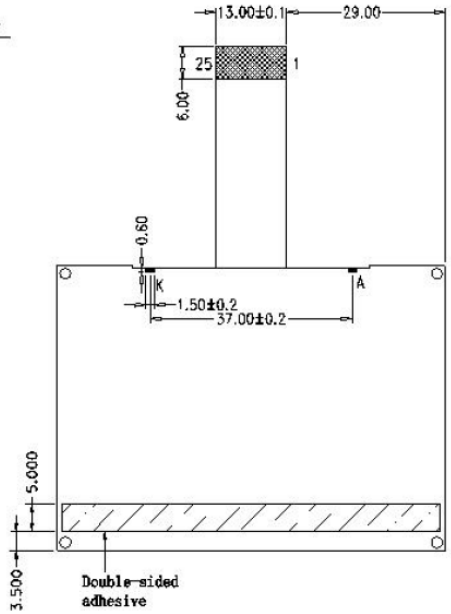
Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	--	71.0	--	mm	--
	Vertical (V)	--	52.0	--	mm	--
	Depth (D)	--	9.8	--	mm	--
Weight		--	35	--	g	Approximate

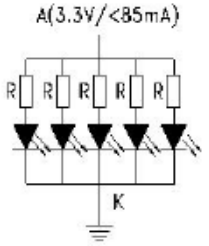
1. Outline Dimensions

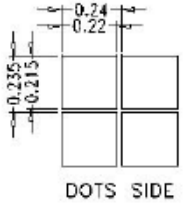
Rev.	Description	Date
1.0	First	04/03/2023

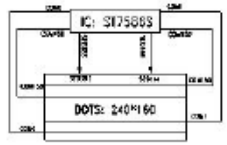




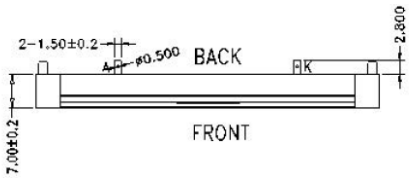








NO	PIN
1	ESD
2	A0
3	RWR
4	D0
5	D1
6	D2
7	D3
8	D4
9	D5
10	D6
11	D7
12	ERD
13	RSTB
14	IF1
15	IF2
16	IF3
17	CSB
18	VDD1
19	VD1
20	VSS
21	VDD
22	VM
23	V0
24	XVO
25	VG



NOTES:

1. DISPLAY DRIVE: DUTY 1/160, BIAS 1/12, VLCD 16V, VDD 3.3V
2. DISPLAY MODE: FSTN GRAY, TRANSFLECTIVE, POSITIVE
3. LCM DRIVER IC: ST7586S OR EQUIVALENTS
4. OPERATING TEMPERATURE: -20°C TO +70°C
5. STORAGE TEMPERATURE: -30°C TO +80°C
6. VIEWING DIRECTION: 6:00
7. BACKLIGHT: WHITE 3.3V, 85mA
8. ROHS COMPLIANT

Model Name: G240160A-FTW-DW63			
General Tol: ±0.2			
Approvals	Date	Drawing No.:	Scale:
DWN:			
CHK:		Size:	Unit: mm / Page: 1/1
APP:			

2. Input Terminal Pin Assignment

NO.	Symbol	Description
1	ESD	Ground
2	A0	The function of this pin is different in parallel and serial interface. In parallel interface: A0 is register selection input. A0 = "H": inputs on data bus are display data; A0 = "L": inputs on data bus are command. In serial interface: this pad will be used as SCL (serial-clock) input.
3	RWR	Read / Write execution control pin. (This pin is only used in parallel interface) MPU Type RWR Description 6800-series R/W Read / Write control input pin R/W = "H" : read R/W = "L" : write 8080-series /WR Write enable clock input pin. The data are latched at the rising edge of the /WR signal. This pin is not used in serial interfaces and should be connected to VDD1.
4-11	D0-D7	Data bus
12	ERD	Read / Write execution control pin. (This pin is only used in parallel interface) MPU Type ERD Description 6800-series E Read / Write control input pin. R/W = "H": When E is "H", data bus is in output status. R/W = "L": The data are latched at the falling edge of the E signal. 8080-series /RD Read enable input pin. When /RD is "L", data bus is in output status. This pin is not used in serial interfaces and should be connected to VDD1.
13	RSTB	These pins select interface operation mode. IF3 IF2 IF1 MPU interface type H H L 80 series 8-bit parallel H L L 68 series 8-bit parallel L H H 8-bit serial (4-Line) L H L 9-bit serial (3-Line) Note: Refer to "Interface Selection" for detailed information.
14	IF1	
15	IF2	
16	IF3	
17	CSB	Chip select input pin.
18	VDD1	VDD1 is the power of interface I/O circuit.
19	VD1	VD1 is the power source of digital circuits.
20	VSS	Ground.
21	VDD	Power of interface I/O circuit.
22	VM	The non-select voltage level of COM-drivers.
23	V0	Positive operating voltage of COM-drivers.
24	XV0	Negative operating voltage of COM-drivers.
25	VG	VG is the power of SEG-drivers.

3. Electrical Characteristics

3.1 Absolute Maximum Rating

Characteristics	Symbol	Min	Max	Unit
Supply Voltage	VDD	-0.3	4.0	V
	Vout	-0.3	18.0	V
Operating Temperature	TOP	-20	+70	°C
Storage Temperature	TST	-30	+80	°C

NOTE: If the absolute maximum rating of the above parameters is exceeded, even momentarily, the quality of the product may be degraded. Absolute maximum ratings specify the values which the product may be physically damaged if exceeded. Be sure to use the product within the range of the absolute maximum ratings.

3.2 DC Electrical Characteristics

Characteristics		Symbol	Condition	Min	Typ.	Max	Unit
LCD Driving Voltage		VLCD		--	16.0	--	V
Supply Voltage		Logic	VDD-GND	--	3.3	--	V
Input Voltage	H Level	VDD		0.8VDD	--	VDD	V
	L Level	VIH		VSS	--	0.2VDD	V

Condition:

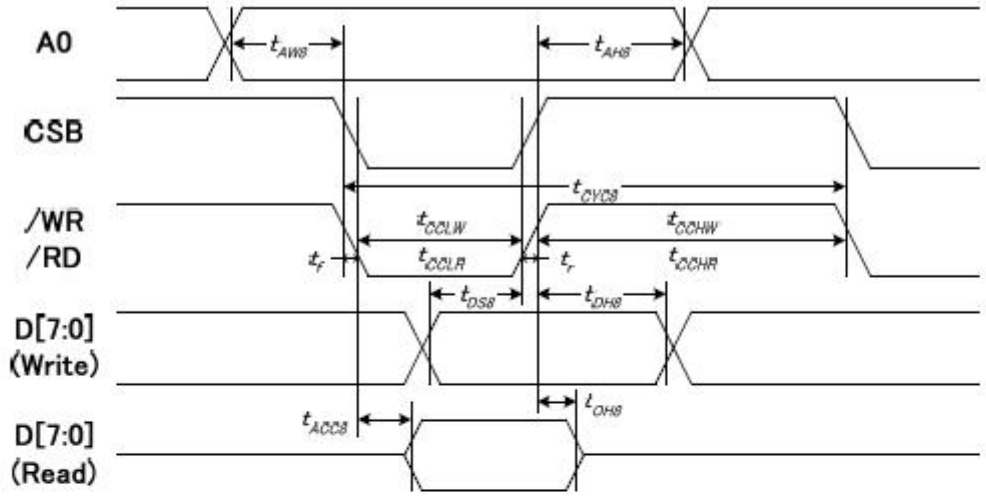
1. VDD = 3.3V
2. 1/160 Duty, 1/12 Bias

4. Module Function Description

4.1 Timing Characteristics

TIMING CHARATERISTIC

System Bus Timing for 8080 MCU Interface



VDD1 = 1.8V, Ta = 25°C

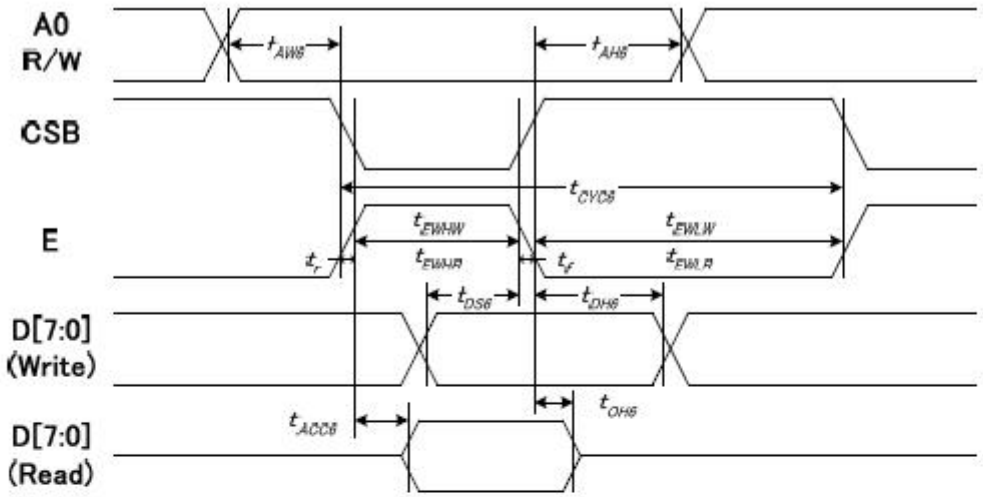
Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		0	—	ns
Address hold time		tAH8		0	—	
System cycle time (WRITE)	/WR	tCYC8		240	—	
/WR L pulse width (WRITE)		tCCLW		100	—	
/WR H pulse width (WRITE)		tCCHW		100	—	
System cycle time (READ)	RD	tCYC8		500	—	
/RD L pulse width (READ)		tCCLR		220		
/RD H pulse width (READ)		tCCHR		220		
WRITE Data setup time	D[7:0]	tDS8		20	—	
WRITE Data hold time		tDH8		20	—	
READ access time		tACC8	CL = 30 pF	—	100	
READ Output disable time		tOH8	CL = 30 pF	10	110	

Note:

1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≦ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≦ (tCYC8 – tCCLR – tCCHR) are specified.
2. All timing is specified using 20% and 80% of VDD1 as the reference.
3. tCCLW and tCCLR are specified as the overlap between CSB being "L" and WR and RD being at the "L" level.

4.2 System bus timing for 6800

System Bus Timing for 6800 MCU Interface



VDD1 = 1.8V, Ta = 25°C

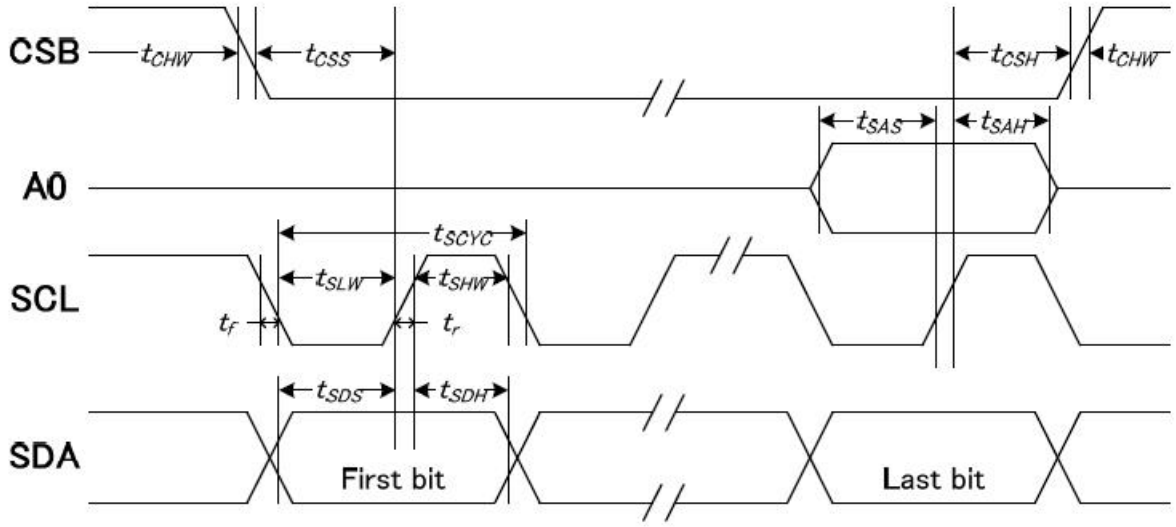
Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		0	—	ns
Address hold time		tAH6		0	—	
System cycle time (WRITE)	E	tCYC6		240	—	
Enable L pulse width (WRITE)		tEWLW		100	—	
Enable H pulse width (WRITE)		tEWHW		100	—	
System cycle time (READ)		tCYC6		500		
Enable L pulse width (READ)		tEWLR		220	—	
Enable H pulse width (READ)		tEWHR		220		
Write data setup time	D[7:0]	tDS6		20	—	
Write data hold time		tDH6		20	—	
Read data access time		tACC6	CL = 16 pF	—	100	
Read data output disable time		tOH6	CL = 16 pF	10	110	

Note:

1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≤ (tCYC6 – tEWLR – tEWHR) are specified.
2. All timing is specified using 20% and 80% of VDD1 as the reference.
3. tEWLW and tEWLR are specified as the overlap between CSB being "L" and E.

4.3 System bus timing for 4-Line

System Bus Timing for 4-Line SPI MCU Interface



VDD1 = 1.8V, Ta = 25°C

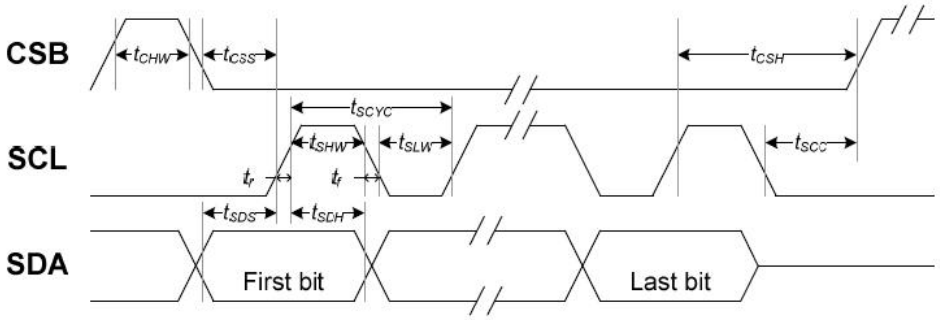
Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	tSCYC		100	—	ns
SCLK "H" pulse width		tSHW		45	—	
SCLK "L" pulse width		tSLW		45	—	
Address setup time	A0	tSAS		20	—	
Address hold time		tSAH		20	—	
Data setup time	SDA	tSDS		20	—	
Data hold time		tSDH		20	—	
CSB-SCLK time	CSB	tCSS		20	—	
CSB-SCLK time		tCSH		20	—	
CS "H" pulse width		tCHW		0	—	

Note:

1. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of VDD1 as the standard.

4.4 System bus timing for 3-Line

System Bus Timing for 3-Line SPI MCU Interface



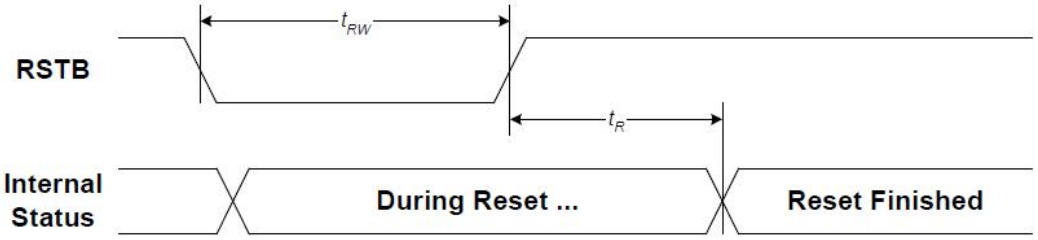
VDD1 = 1.8V, Ta = 25℃

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Serial Clock Period	SCLK	tSCYC		100	—	ns
SCL "H" pulse width		tSHW		45	—	
SCL "L" pulse width		tSLW		45	—	
Data setup time	SDA	tSDS		20	—	
Data hold time		tSDH		20	—	
CS-SCL time	CSB	tCSS		30	—	
		tCSH		30	—	
CS "H" pulse width		tCHW		0	—	

Note:

1. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
2. All timing is specified using 30% and 70% of VDD1 as the standard.

Reset Timing



VDD1 = 1.8V, Ta = 25°C

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		120	—	ms
Reset "L" pulse width	tRW		10	—	us

4.5 Command Table

INSTRUCTION	A0	R/W	COMMAND BYTE D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
NOP	0	0	0	0	0	0	0	0	0	0	No operation
RESET	0	0	0	0	0	0	0	0	0	1	Software reset
Power Save	0	0	0	0	0	1	0	0	0	SLP	Set power save mode SLP=0: Sleep in mode SLP=1: Sleep out mode
Partial Mode	0	0	0	0	0	1	0	0	1	PTL	Set partial mode PTL=0: Partial mode on PTL=1: Partial mode off
Inverse Display	0	0	0	0	1	0	0	0	0	INV	Set inverse display mode INV=0: Normal display INV=1: Inverse display
All Pixel ON/OFF	0	0	0	0	1	0	0	0	1	AP	Set all pixel on mode AP=0: All pixel off mode AP=1: All pixel on mode
Display ON/OFF	0	0	0	0	1	0	1	0	0	DSP	Set LCD display DSP=0: Display off DSP=1: Display on
Set Column Address	0	0	0	0	1	0	1	0	1	0	Set column address Starting column address: 00h≦XS≦7Fh Ending column address: XS≦XE≦7Fh
	1	0	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	
	1	0	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
	1	0	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	
	1	0	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	
Set Row Address	0	0	0	0	1	0	1	0	1	1	Set row address Starting row address: 00h≦YS≦9Fh Ending row address: YS≦YE≦9FH
	1	0	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	
	1	0	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
	1	0	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	
	1	0	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	
Write Display Data	0	0	0	0	1	0	1	1	0	0	Write display data to DDRAM
	1	0	D7	D6	D5	D4	D3	D2	D1	D0	
Read Display Data	0	0	0	0	1	0	1	1	1	0	Read display data from DDRAM
	1	1	D7	D6	D5	D4	D3	D2	D1	D0	
Partial Display Area	0	0	0	0	1	1	0	0	0	0	Set partial area Partial display address start: 00h≦PTS≦9Fh Partial display address end: 00h≦PTE≦9Fh Display Area: 64≦Duty≦160
	1	0	PTS15	PTS14	PTS13	PTS12	PTS11	PTS10	PTS9	PTS8	
	1	0	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0	
	1	0	PTE15	PTE14	PTE13	PTE12	PTE11	PTE10	PTE9	PTE8	
	1	0	PTE7	PTE6	PTE5	PTE4	PTE3	PTE2	PTE1	PTE0	
Scroll Area	0	0	0	0	1	1	0	0	1	1	Set scroll area Top Area: TA=00h~A0h Scrolling Area: SA=00h~A0h Bottom Area: BA=00h~A0h TA+SA+BA=160
	1	0	TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0	
	1	0	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0	
	1	0	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0	
Display Control	0	0	0	0	1	1	0	1	1	0	Set scan direction of COM and SEG MY=0: COM0→COM159 MY=1: COM159→COOM0 MX=0: SEG0→SEG383 MX=1: SEG383→SEG0
	1	0	MY	MX	0	0	0	0	0	0	
Start Line	0	0	0	0	1	1	0	1	1	1	Set display start line S=00h~9Fh
	1	0	S7	S6	S5	S4	S3	S2	S1	S0	

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Display Mode	0	0	0	0	1	1	1	0	0	M	Set display mode M=0: Gray mode M=1: Monochrome mode
Enable DDRAM Interface	0	0	0	0	1	1	1	0	1	0	Enable DDRAM interface
	1	0	0	0	0	0	0	0	1	0	
Display Duty	0	0	1	0	1	1	0	0	0	0	Set display duty DT=03h~9Fh
	1	0	DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0	
First Output COM	0	0	1	0	1	1	0	0	0	1	Set first output COM FC=00h~9Fh
	1	0	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	
FOSC Divider	0	0	1	0	1	1	0	0	1	1	Set FOSC dividing ratio
	1	0	0	0	0	0	0	0	FOD1	FOD0	
Partial Display	0	0	1	0	1	1	0	1	0	0	Set partial display mode
	1	0	1	0	1	0	0	0	0	0	
N-Line Inversion	0	0	1	0	1	1	0	1	0	1	Set N-Line inversion
	1	0	M	0	0	NL4	NL3	NL2	NL1	NL0	
Read Modify Write	0	0	1	0	1	1	1	0	0	RMW	Read modify write control RMW=0: Enable read modify write RMW=1: Disable read modify write
Set Vop	0	0	1	1	0	0	0	0	0	0	Set Vop
	1	0	Vop7	Vop6	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0	
	1	0	-	-	-	-	-	-	-	Vop8	
Vop Increase	0	0	1	1	0	0	0	0	0	1	Vop increase one step
Vop Decrease	0	0	1	1	0	0	0	0	1	0	Vop decrease one step
BIAS System	0	0	1	1	0	0	0	0	1	1	Set BIAS system
	1	0	-	-	-	-	-	BS2	BS1	BS0	
Booster Level	0	0	1	1	0	0	0	1	0	0	Set booster level
	1	0	-	-	-	-	-	BST2	BST1	BST0	
Vop Offset	0	0	1	1	0	0	0	1	1	1	Set Vop offset
	1	0	0	VOF6	VOF5	VOF4	VOF3	VOF2	VOF1	VOF0	
Analog Control	0	0	1	1	0	1	0	0	0	0	Enable analog circuit
	1	0	0	0	0	1	1	1	0	1	
Auto Read Control	0	0	1	1	0	1	0	1	1	1	Auto read control XARD=0: Enable auto read XARD=1: Disable auto read
	1	0	1	0	0	XARD	1	1	1	1	
OTP WR/RD Control	0	0	1	1	1	0	0	0	0	0	OTP WR/RD control WR/RD=0: Enable OTP read WR/RD=1: Enable OTP write
	1	0	0	0	WR /RD	0	0	0	0	0	
OTP Control Out	0	0	1	1	1	0	0	0	0	1	OTP control out
OTP Write	0	0	1	1	1	0	0	0	1	0	OTP programming procedure
OTP Read	0	0	1	1	1	0	0	0	1	1	OTP up-load procedure
OTP Selection Control	0	0	1	1	1	0	0	1	0	0	OTP selection control Ctrl=0: Disable OTP Ctrl=1: Enable OTP
	1	0	0	Ctrl	0	1	1	0	0	1	
OTP Programming Setting	0	0	1	1	1	0	0	1	0	1	OTP programming setting
	1	0	0	0	0	0	1	1	1	1	

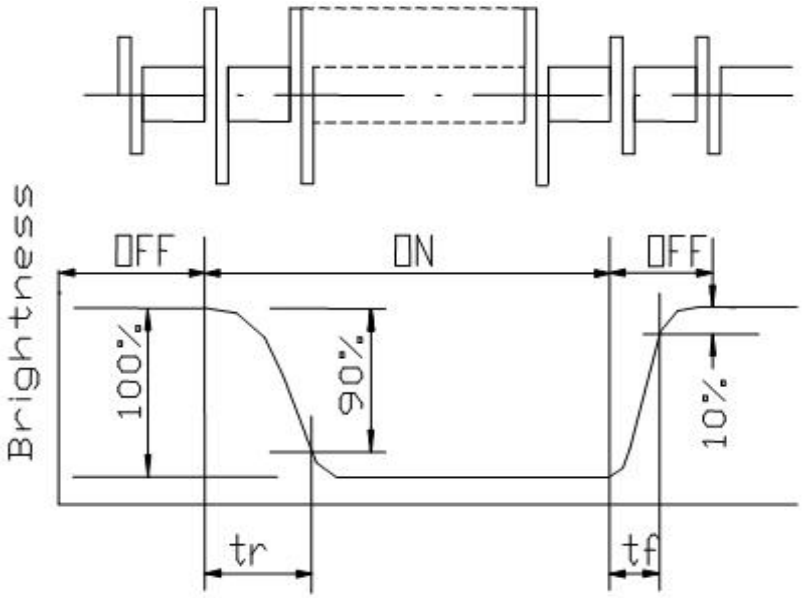
INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Frame Rate (Gray Scale Mode)	0	0	1	1	1	1	0	0	0	0	Frame rate setting in different temperature range (Gray scale mode)
	1	0	-	-	-	FRA4	FRA3	FRA2	FRA1	FRA0	
	1	0	-	-	-	FRB4	FRB3	FRB2	FRB1	FRB0	
	1	0	-	-	-	FRC4	FRC3	FRC2	FRC1	FRC0	
	1	0	-	-	-	FRD4	FRD3	FRD2	FRD1	FRD0	
Frame Rate (Monochrome Mode)	0	0	1	1	1	1	0	0	0	1	Frame rate setting in different temperature range (Monochrome mode)
	1	0	-	-	-	FRA4	FRA3	FRA2	FRA1	FRA0	
	1	0	-	-	-	FRB4	FRB3	FRB2	FRB1	FRB0	
	1	0	-	-	-	FRC4	FRC3	FRC2	FRC1	FRC0	
	1	0	-	-	-	FRD4	FRD3	FRD2	FRD1	FRD0	
Temperature Range	0	0	1	1	1	1	0	0	1	0	Temperature range setting
	1	0	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0	
	1	0	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0	
	1	0	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0	
Temperature Gradient Compensation	0	0	1	1	1	1	0	1	0	0	Set temperature gradient compensation coefficient
	1	0	MT13	MT12	MT11	MT10	MT03	MT02	MT01	MT00	
	1	0	MT33	MT32	MT31	MT30	MT23	MT22	MT21	MT20	
	1	0	MT53	MT52	MT51	MT50	MT43	MT42	MT41	MT40	
	1	0	MT73	MT72	MT71	MT70	MT63	MT62	MT61	MT60	
	1	0	MT93	MT92	MT91	MT90	MT83	MT82	MT81	MT80	
	1	0	MTB3	MTB2	MTB1	MTB0	MTA3	MTA2	MTA1	MTA0	
	1	0	MTD3	MTD2	MTD1	MTD0	MTC3	MTC2	MTC1	MTC0	
	1	0	MTF3	MTF2	MTF1	MTF0	MTE3	MTE2	MTE1	MTE0	

5. LCD Optical Characteristics

5.1 FSTN Type

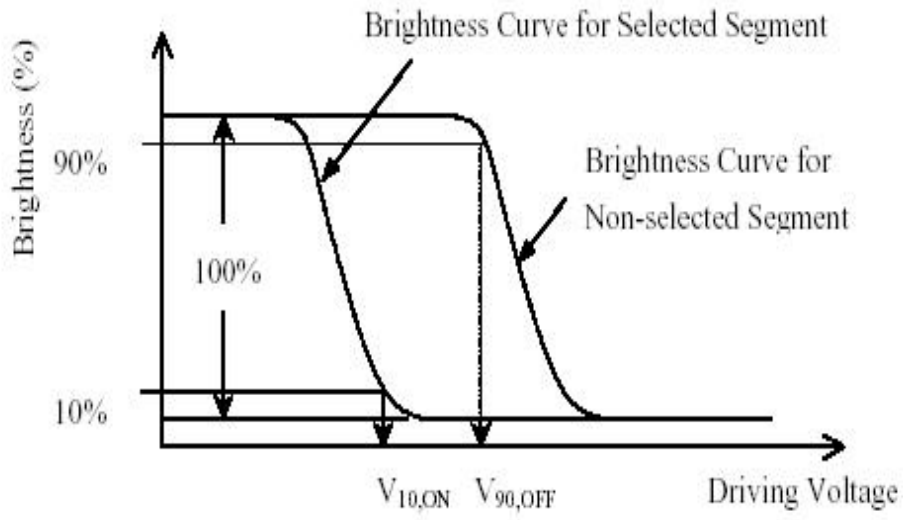
Item	Symbol	Condition	Min	Typ	Max	Units
Contrast	K	θ=0° Φ=0°	5 : 1	—	—	deg.
Viewing Angle	θ	K=5 Φ=0°	$\theta_2 - \theta_1$=30	—	—	deg.
		K=5 θ=10°	Φ= ± 30	—	—	deg.
Response time	T_{on}	25°C	—	—	250	ms
	T_{off}	25°C	—	—	250	ms

5.2 Definition of Optical Response Time

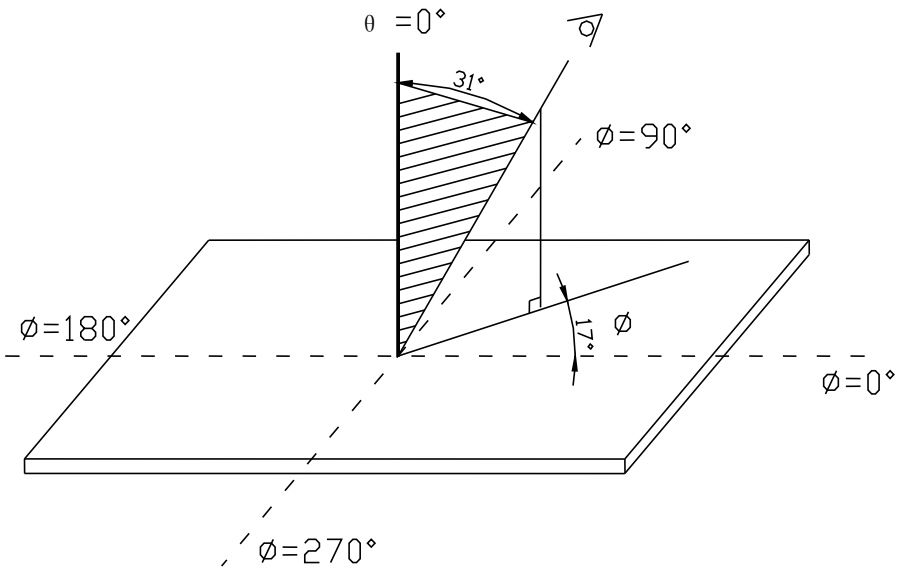


5.3 Definition of Driving Voltage (Vlcd)

Vlcd=(V10,ON +V90,OFF)/2



5.4 Definition of Viewing Angle θ and Φ



5.5 Life Time

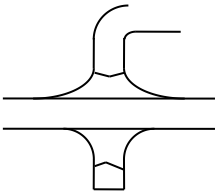
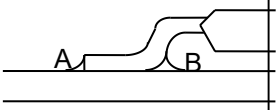
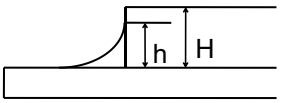
Item	Description
LCD	Function, performance, appearance, etc. shall be free from remarkable deterioration within 50,000 hours under ordinary operating and storage conditions of room temperature (25±10°C), normal humidity (45±20% RH), and in area not exposed to direct sunlight.
LED BL	L70. The brightness of the backlight LEDs should not fall below 70% of its original brightness within 24 months under ordinary operating and storage conditions of room temperature (25±10°C), normal humidity (45±20% RH), and in area not exposed to direct sunlight.

6. Reliability

No.	Test Item	Content of Test	Test Condition
1	High Temperature Storage	Endurance test applying the high storage temperature for a long time	+80 C 96H
2	Low Temperature Storage	Endurance test applying the low storage temperature for a long time	-30 C 96H
3	High Temperature Operation	Endurance test applying the electric stress (voltage & current) and the thermal stress to the element for a long time	+70 C 96H
4	Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time	-20 C 96H
5	High Temperature/ Humidity Storage	Endurance test applying the high temperature and humidity storage for a long time	40 C 90%RH 96H
6	Temperature Cycle	Endurance test applying the low and high temperature cycle -20°C ⟷ 25°C ⟷ 70°C ⟷ 25°C 30min 5min 30min 5min ⟷ 1 cycle	-20 C/70 C 10 cycles
7	Vibration Test (Package State)	Endurance test applying the vibration during transportation	10Hz －55Hz , 50m/s,15min
8	Shock Test (Package State)	Endurance test applying the shock during transportation	Half-sinewave, 100m/s,11ms
9	Atmospheric Pressure Test	Endurance test applying the atmospheric pressure during transportation by air	40 kPa 16 H

7. Inspection Criteria

Module Cosmetic Criteria

No.	Item	Judgment Criterion	Partition
1	Pattern peeling	No substrate pattern peeling and floating	Major
2	Soldering defects	No soldering missing No soldering bridge No cold soldering	Major Major Minor
3	Resist flaw on substrate	Invisible copper foil (∅0.5mm or more) on substrate pattern	Minor
4	Accretion of metallic Foreign matter	No soldering dust No accretion of metallic foreign matters (Not exceed ∅0.2mm)	Minor Minor
5	Stain	No stain to spoil cosmetic badly	Minor
6	Plate discoloring	No plate fading, rusting and discoloring	Minor
7	Solder amount 1. Lead parts	a. Soldering side of PCB Solder to form a 'Filet' all around the lead. Solder should not hide the lead form perfectly. (too much)  b. Components side (In case of 'Through Hole PCB') Solder to reach the Components side of PCB.	Minor
	2. Flat packages	Either 'Toe' (A) or 'Seal' (B) of the lead to be covered by 'Filet'.  Lead form to be assume over solder.	Minor
	3. Chips	$(3/2)\,H \geq h \geq (1/2)\,H$  	Minor

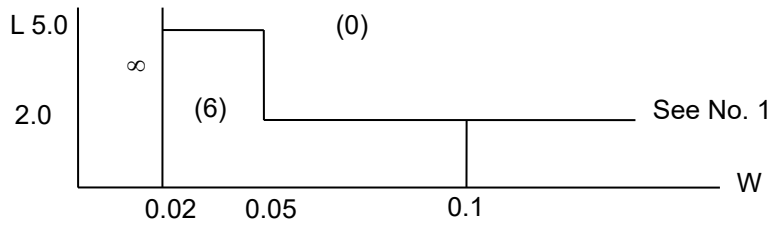
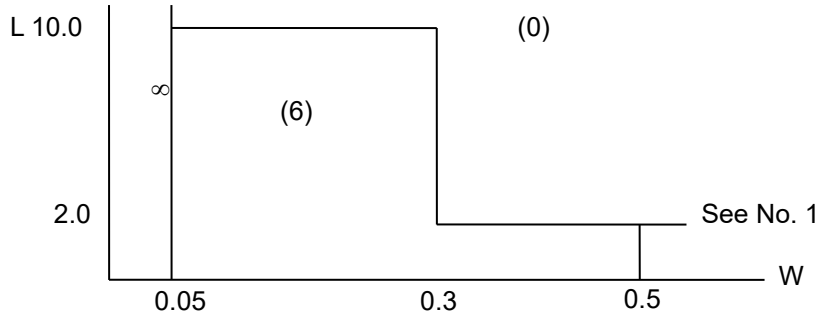
Screen Cosmetic Criteria (Non-Operating)

No.	Defect	Judgment Criterion	Partition
1	Spots	In accordance with Screen Cosmetic Criteria (Operating) No.1.	Minor
2	Lines	In accordance with Screen Cosmetic Criteria (Operating) No.2.	Minor
3	Bubbles In polarizer	Size : d mm / Acceptable ty in active area $d \leq 0.3$ — Disregard $0.3 < d \leq 1.0$ — 3 $1.0 < d \leq 1.5$ — 1 $1.5 < d$ — 0	Minor
4	Scratch	In accordance with spots and lines operating cosmetic	Minor

		criteria. When the light reflects on the panel surface, the scratches are not to be remarkable.	
5	Allowable density	Above defects should be separated more than 30mm each other.	Minor
6	Coloration	Not to be noticeable coloration in the viewing area of the LCD panels. Back-lit type should be judged with back-lit on state only.	Minor
7	Contamination	Not to be noticeable.	Minor

Screen Cosmetic Criteria (Operating)

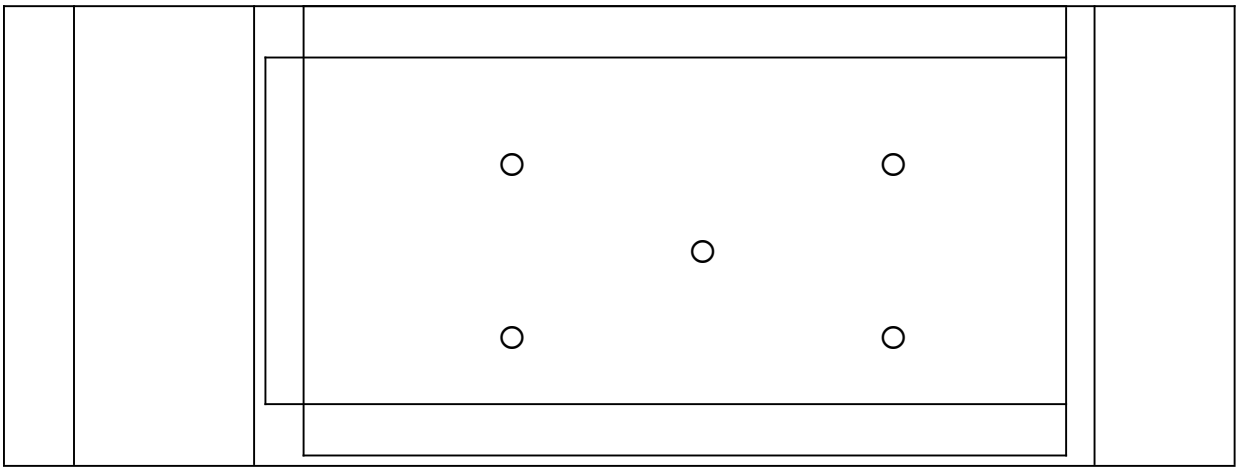
<table>
<tr><th>No.</th><th>Defect</th><th>Judgment Criterion</th><th>Partition</th></tr>
<tr><td>1</td><td>Spots</td><td>A) Clear
<table>
<tr><th>Size : d mm</th><th>Acceptable Qty in active area</th></tr>
<tr><td>$d \leq 0.1$</td><td>Disregard</td></tr>
<tr><td>$0.1 < d \leq 0.$</td><td>4</td></tr>
<tr><td>$0. < d \leq 0.3$</td><td>2</td></tr>
<tr><td>$0.3 < d$</td><td>0</td></tr>
</table>
Note : Including pin holes and defective dots which must be within one pixel size.
B) Unclear
<table>
<tr><th>Size : d mm</th><th>Acceptable Qty in active area</th></tr>
<tr><td>$d \leq 0.$</td><td>Disregard</td></tr>
<tr><td>$0. < d \leq 0.$</td><td>4</td></tr>
<tr><td>$0. < d \leq 0.$</td><td>2</td></tr>
<tr><td>$0. < d$</td><td>0</td></tr>
</table></td><td>Minor</td></tr>
</table>

2	Lines	A) Clear  Note : ( ) - Acceptable Qty in active area L - Length (mm) W- Width (mm) ∞-Disregard B) Unclear  	Minor

'Clear' = The shade and size are not changed by VO.

'Unclear' = The shade and size are changed by VO.

No.	Defect	Judgment Criterion	Partition
3	Rubbing line	Not to be noticeable.	Minor
4	Allowable density	Above defects should be separated more than 10mm each other.	Minor
5	Rainbow	Not to be noticeable.	Minor
6	Dot si e	To be 95% ~ 105% of the dot size (Typ.) in drawing. Partial defects of each dot (ex. pin-hole) should be treated as 'spot'. (see *Screen Cosmetic Criteria (Operating) No.1*)	Minor
7	Uneven brightness (only back-lit type module)	Uneven brightness must be BMAX / BMIN ≤2 - BMAX : Max. value by measure in 5 points - BMIN : Min. value by measure in 5 points Divide active area into 4 vertically and hori ontally. O: Measure 5 points shown in the following figure.	Minor



Note :

(1) Size : d = (long length + short length) / 2

(2) The limit samples for each item have priority.

(3) Complexed defects are defined item by item, but if the number of defects are defined above table, the total number should not exceed 10.

(4) In case of ‘concentration’, even the spots or the lines of ‘disregarded’ size should not allowed. Following three situations should be treated as ‘concentration’.

- 7 or over defects in circle of ∅5mm.
- 10 or over defects in circle of ∅10mm.
- 20 or over defects in circle of ∅20mm.

8.0 Cautions and Handling Precautions

8.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the “Power ON” condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence.

8.2 Storage and Transportation

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.