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Ph. 480-503-4295 | NOPP@FocusLCD.com

TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

Graphic Display Module

Part Number

G160100B-FTW-LW63

Overview

160x100(49.2x47.6), FSTN, Gray background, White Edge lit, Bottom view, Wide temp, Transflective (positive), 3.0V LCD, 3.3V LED, Controller=ST7528i, RoHS Compliant

1.Features

1. 160X100 dots
2. Built-in controller (ST7528I)
3. +3.3V power supply
4. 1/100 duty cycle;1/11bias
5. BKL to be driven by A, K.

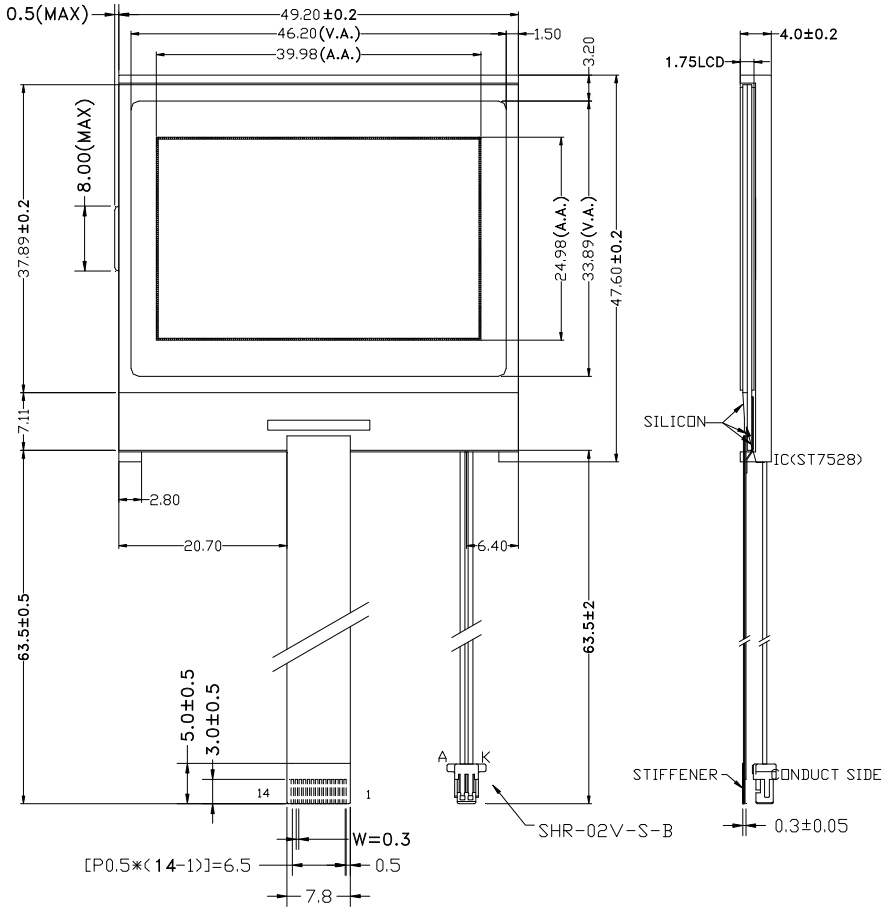
LCD type	☑FSTN positive		☐FSTN Negative	
	☐STN Yellow Green	☐STN Gray		☐STN-Blue
View direction	☑6 O'clock	☐12 O'clock		
Rear Polarizer	☐Reflective	☑Transflective		☐Transmissive
Backlight Type	☑LED Edge	☐EL	☐Internal Power	☐4.2V input
	☐LED Array	☐CCFL	☑External Power	☑3.0 input
Backlight Color	☑White	☐Amber	☐Blue-Green	☐Yellow-Green
Temperature Range	☐Normal	☐Wide		☑Super Wide
DC to DC circuit	☑Build-in		☐Not Build-in	
El Driver IC	☐Build-in		☑Not Build-in	
Touch screen	☐With		☐Without	
Font type	☐English-Japanese	☐English-European	☐English-Russian	☑other
	☑ ROHS			

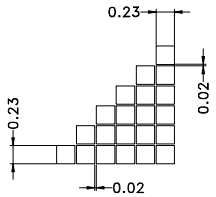
2. MECHANICAL SPECIFICATIONS

Module size	49.2 mm(L) * 47.6 mm(W) * 4.0(H)mm Max
Viewing area	46.2 mm(L) * 33.9 mm(W)
Dots size	0.23 mm(L) * 0.23 mm(W)
Dots pitch	0.25 mm(L) * 0.25 mm(W)
Weight	Approx.

3.**Outline dimension**

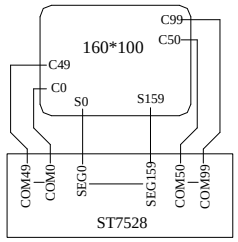
REV	DESCRIPTION:	DATE
1.0	First	





Scale:5/1

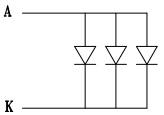
Detail:DOTS



PIN ASSIGNMENT

1	CSB
2	RST
3	NC
4	SCL
5	SDA
6	VDD
7	VSS
8	VOUT
9	V4
10	V3
11	V2
12	V1
13	NC
14	NC

WHITE LED BACKLIGHT



SM02B-SRSS-TB

Specification:

1). Driving: Duty:1/100, 1/11 Bais, Vlcd: 11.5V
2). Viewing Direction: 6 O'clock
3). Display mode: FSTN/Positive/Transflective
4). Operating temp.: -20°c~+70°C
Storage temp.: -30°c~+80°C
5). Driver : ST7528i Vdd:3.0V I2C Interface
6). Ledbacklight: White Color, 3~3.3V, Curent: 45~60mA
7). RoHS Compliant

Model Name:		FocusLCDs.com LCDs MADE SIMPLE®	
GENERAL TOL: ± 0.2			
APPROVALS	DATE	DRAWN NO. G160BLGFGSW6WTC3XAM	SCALE:
DWN:		SIZE: A4	UNIT: mm / Page:
CHK:			
APP:			

4.Absolute maximum ratings

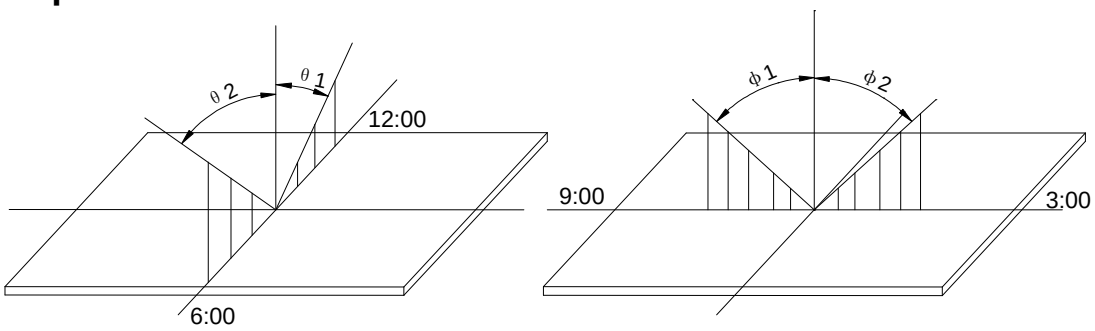
Item	Symbol	Standard			Unit
Power voltage	V_{DD}-V_{SS}	0.3	-	3.6	V
Input voltage	V_{IN}	VSS	-	VDD	
Operating temperature range	T_{OP}	-20	-	+70	℃
Storage temperature range	T_{ST}	-30	-	+80	

5.Interface pin description

Recommended Connector: FH12-14S-0.5SH(55)

Pin no.	Symbol	External connection	Function
1	CSB	MPU	Chip select input pins, Chip is enabled only when CSB is "L".
2	RST	MPU	Reset input pin ,When RESETB is “L”, initialization is executed.
3	NC		
4	SCL	MPU	Serial clock input
5	SDA	MPU	Serial data input
6	V_{DD}	Power supply	Power supply for LCM (+3.3V)
7	V_{SS}	Power supply	
8	VOUT	supply	Internal Vout voltage
9~12	V4~V1	supply	LCD driver supply voltages
13	NC		
14	NC		

6.Optical characteristics



STN type display module (Ta=25℃, VDD=3.3V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing angle	θ 1	$C_r \geqslant 3$		20		deg
	θ 2			40		
	Φ 1			35		
	Φ 2			35		
Contrast ratio	C_r		-	10	-	-
Response time (rise)	T_r	-	-	200	250	ms
Response time (fall)	T_r	-	-	300	350	

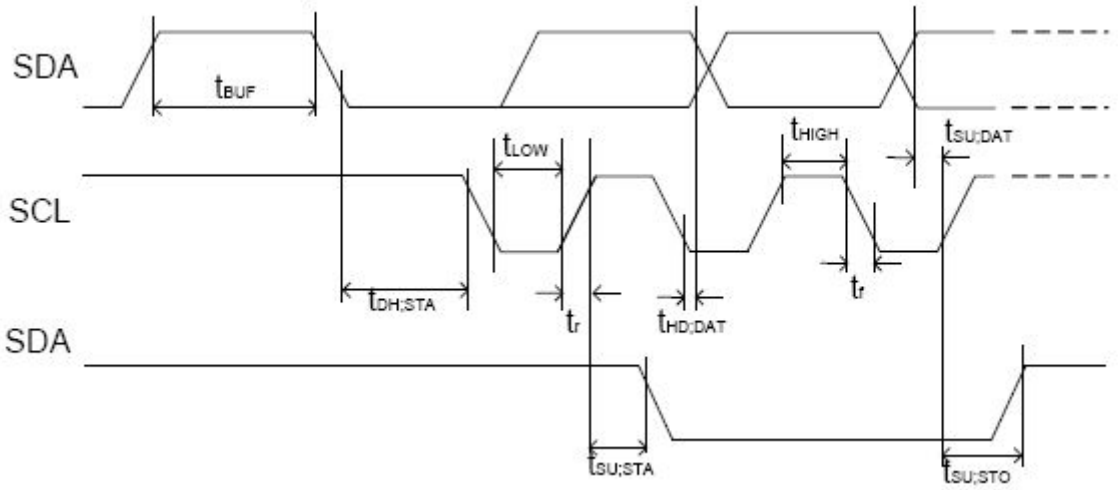
7.Electrical characteristics

DC characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage for LCD	V_{DD}-V_0	Ta =25℃		11.5		V
Input voltage	V_{DD}		2.4	3.3	3.3	
Supply current	I_{DD}	Ta=25℃, V_{DD}=5.0V	-	500	-	uA
Input leakage current	I_{LKG}		-	-		uA
“H” level input voltage	V_{IH}		2.2	-	V_{DD}	V
“L” level input voltage	V_{IL}	Twice initial value or less	0	-	0.6	
“H” level output voltage	V_{OH}	LOH=-0.25mA	2.4	-	-	
“L” level output voltage	V_{OL}	LOH=1.6mA	-	-	0.4	
Backlight supply voltage	V_F		-	3.0	-	
Backlight supply current	I_{LED}	V_F=3.0V	-	45	-	mA

8. TIMING CHARACTERISTICS

SERIAL INTERFACE(IIC Interface)



(VDD=3.3V,Ta=-30~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
SCL clock frequency	SCL	FSCLK		-	400	kHZ
SCL clock low period	SCL	TLOW		1.3	-	us
SCL clock high period	SCL	THIGH		0.6	-	us
Data set-up time	SI	TSU;Data		100	-	ns
Data hold time	SI	THD;Data		0	0.9	us
SCL,SDA rise time	SCL	TR		20+0.1Cb	300	ns
SCL,SDA fall time	SCL	TF		20+0.1Cb	300	ns
Capacitive load represented by each bus line		Cb		-	400	pF
Setup time for a repeated START condition	SI	TSU;SUA		0.6	-	us
Start condition hold time	SI	THD;STA		0.6	-	us
Setup time for STOP ondition		TSU;STO		0.6	-	us
Tolerable spike width on bus		TSW		-	50	ns
BUS free time between a STOP and StART condition	SCL	TBUF		1.3		us

9. DESCRIPTION OF FUNCTIONS

➢ **IIC Interface**

The IIC interface receives and executes the commands sent via the IIC Interface. It also receives RAM data and sends it to the RAM.

The IIC Interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Figure 3.

START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Figure 4.

SYSTEM CONFIGURATION

The system configuration is illustrated in Figure 5.

· Transmitter: the device, which sends the data to the bus.

· Receiver: the device, which receives the data from the bus.

· Master: the device, which initiates a transfer, generates clock signals and terminates a transfer.

· Slave: the device addressed by a master.

· Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.

· Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.

· Synchronization: procedure to synchronize the clock signals of two or more devices.

ACKNOWLEDGE

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. A master receiver must also generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the IIC Interface is illustrated in Figure 5.

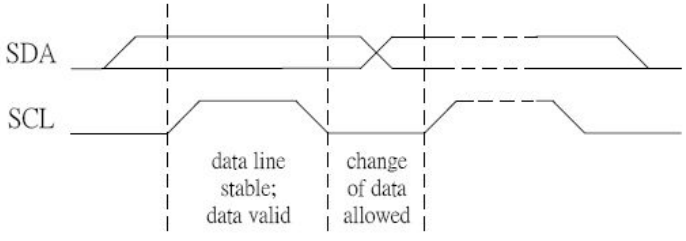


Figure 3 Bit transfer

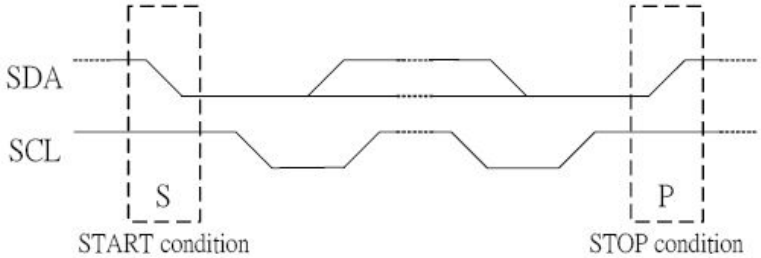


Figure 4 Definition of START and STOP conditions

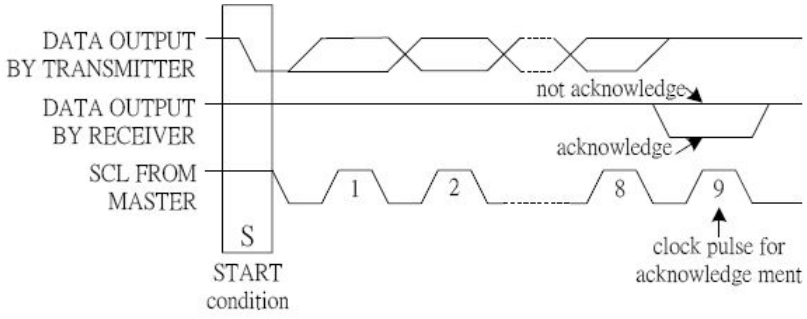


Figure 5 Acknowledgement on the 2-line Interface

IIC Interface protocol

The ST7528 supports command, data write addressed slaves on the bus. Before any data is transmitted on the IIC Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (0111100, 0111101, 0111110 and 0111111) are reserved for the ST7528. The least significant bit of the slave address is set by connecting the input SA0 and SA1 to either logic 0 (VSS) or logic 1 (VDD). The IIC Interface protocol is illustrated in Figure 6.

Note: ST7528 IIC interface can not use with other slaver IIC device

The sequence is initiated with a START condition (S) from the IIC Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the IIC Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines Co and A0, plus a data byte. The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the A0 bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the A0 bit setting; either a series of display data bytes or command data bytes may follow. If the A0 bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended ST7528 device. If the A0 bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the IIC INTERFACE-bus master issues a STOP condition (P).If the R/W bit is set to logic 1 the chip will output data immediately after the slave address if the A0 bit, which was sent during the last write access, is set to logic 0. If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

Write mode:

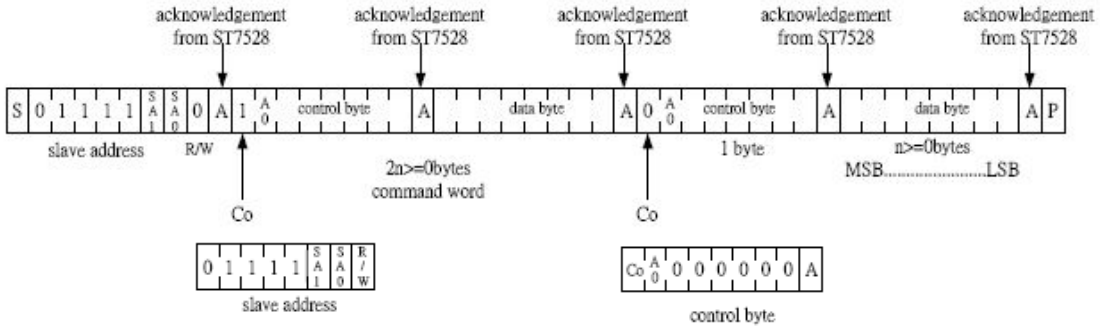


Figure 6 2-line Interface protocol

Co	0	Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by s STOP or RE-START condition.
	1	Another control byte will follow the data byte unless a STOP or RE-START condition is received.

DISPLAY DATA RAM (DDRAM)

When Mode 0 is selected

The Display Data RAM stores pixel data for the LCD. It is 129-row (17 pages by 8 bits) by 132-column addressable array.

Each pixel can be selected when the page and column addresses are specified. The 129 rows are divided into 16 pages of 8 lines and the 17th page with a single line (DB0 only). Data is read from or written to the 8 lines of

each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

When Mode 1 is selected

The Display Data RAM stores pixel data for the LCD. It is 101-row (13 pages by 8 bits) by 160-column addressable array.

Each pixel can be selected when the page and column addresses are specified. The 101 rows are divided into 12 pages of 8 lines and the 13th page with 4 lines; the Page Address 16 (17th page) is for Icon page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

Page Address Circuit

In mode 0

It incorporates 4-bit Page Address register changed by only the “Set Page” instruction. Page Address 16 is a special RAM area for the icons and display data DB0 is only valid. The page address is set from 0 to 15, and Page 16 is for Icon page.

In mode 1

It incorporates 4-bit Page Address register changed by only the “Set Page” instruction. Page Address 16 is a special RAM area for the icons and display data DB0 is only valid. The page address is set from 0 to 12, and Page 16 is for Icon page.

Line Address Circuit

In mode 0

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting Line Address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM. It incorporates 7-bit Line Address register changed by only the initial display line instruction and 7-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the line address for transferring the 128-bit RAM data to the display data latch circuit. When icon is enabled by setting icon control register, display data of icons are not scrolled because the MPU can not access Line Address of icons.

In mode 1

The 7-bit Line Address register is set from 0 ~ 99, If the register is set from 100 ~ 127, It will be no operation. The register value will be kept in last value.

Column Address Circuit

In Mode 0, 1

Column Address Circuit has a 10-bit preset counter that provides Column Address to the Display Data RAM. When set Column Address MSB / LSB instruction is issued, 8-bit [Y9:Y2] are set and lowest 2 bit, Y[1:0] is set to “00”. Since this address is increased by 1 each a read or write data instruction, microprocessor can access the display data continuously. However, the counter is not increased and locked if a non-existing address above 9FH. It is unlocked if a column address is set again by set Column Address MSB / LSB instruction. And the column address counter is independent of page address register.

ADC select instruction makes it possible to invert the relationship between the Column Address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing ADC select instruction. Refer to the following Figure 9 and Figure 10.

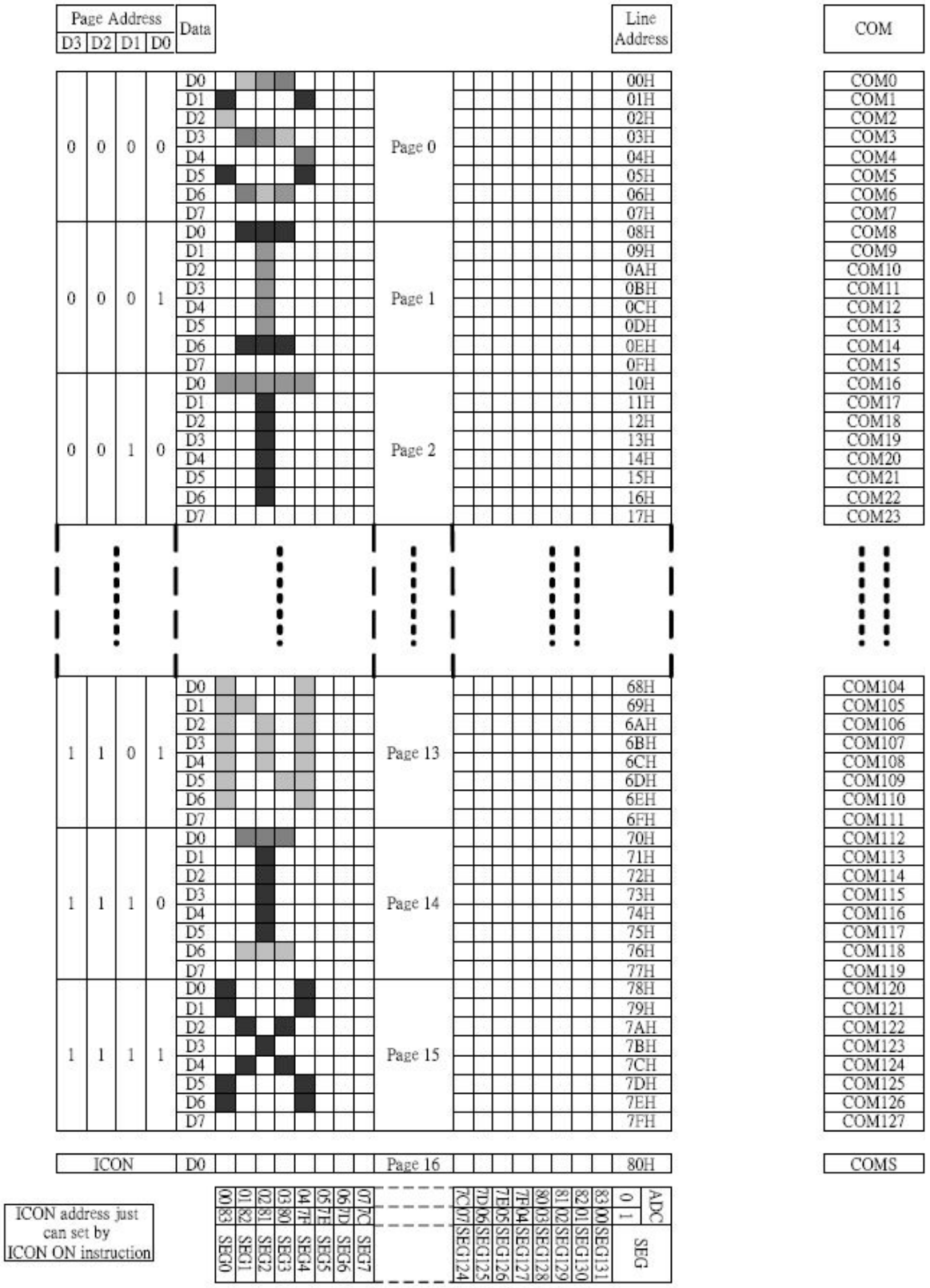
(Note: in mode read or write in fourth, the column address will turn to next column address)

MODE 0

SEG output	SEG 0	SEG 1	SEG 2	SEG 3	…	SEG 128	SEG 129	SEG 130	SEG 131
Column address [Y9:Y2]	00H	01H	02H	03H	…	80H	81H	82H	83H
Internal column address [Y9:Y0]	00 01 02 03	04 05 06 07	08 09 0A 0B	0C 0D 0E 0F	…	200 201 202 203	204 205 206 207	208 209 20A 20B	20C 20D 20E 20F
Display data (ADC=0)	1 1 1 1	1 1 1 0	1 1 0 1	1 1 0 0	…	0 0 1 1	0 0 1 0	0 0 0 1	0 0 0 0
LCD panel display					…				
Display data (ADC=1)	0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	…	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1
LCD panel display					…				

Figure 9. The Relationship between the Column Address and the Segment Outputs

Mode-0 Display RAM Mapping diagram

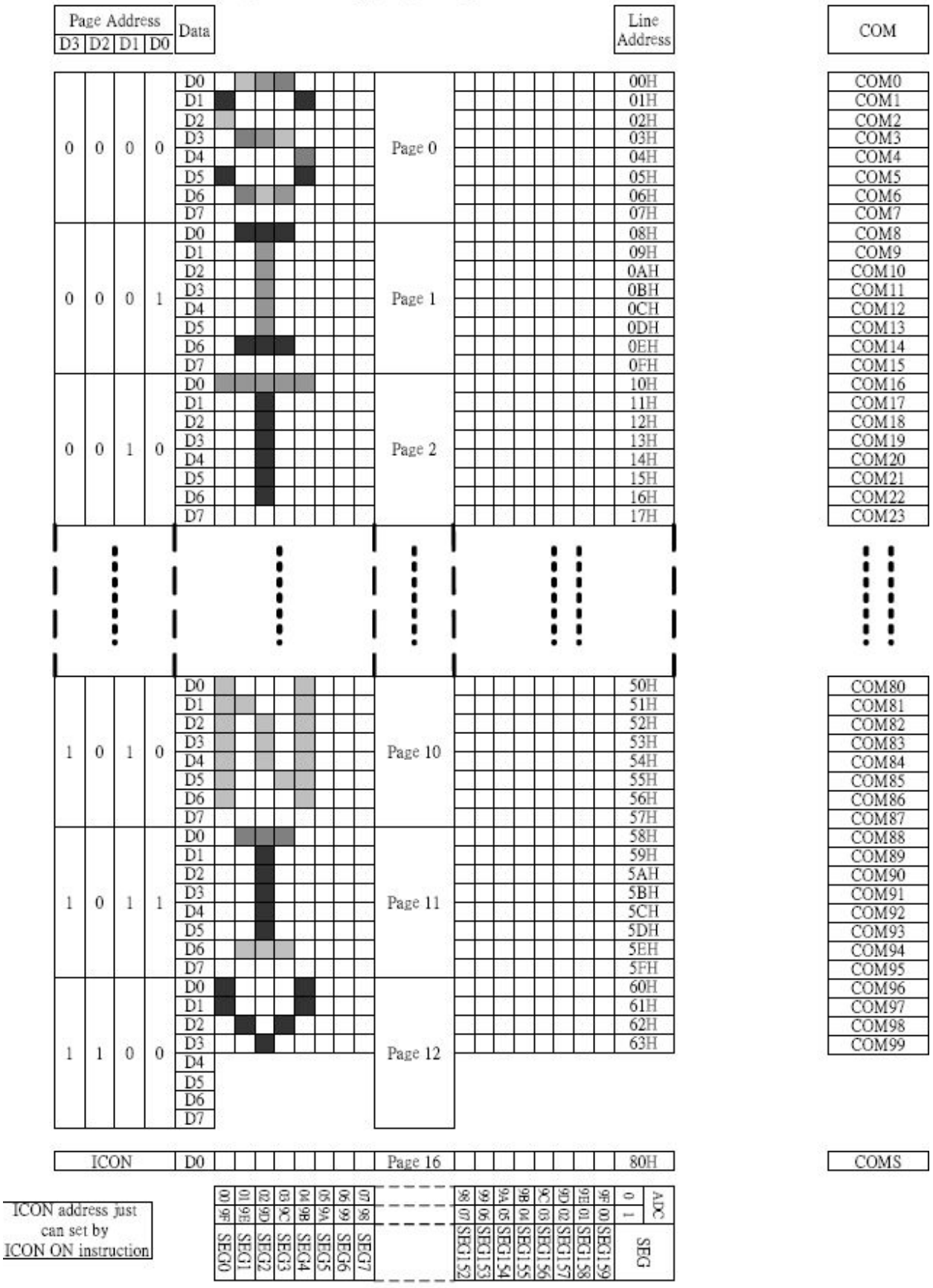

Page Address
D3 D2 D1 D0
Data
Line Address
COM
0 0 0 0 D0 Page 0 00H COM0
D1 01H COM1
D2 02H COM2
D3 03H COM3
D4 04H COM4
D5 05H COM5
D6 06H COM6
D7 07H COM7
0 0 0 1 D0 Page 1 08H COM8
D1 09H COM9
D2 0AH COM10
D3 0BH COM11
D4 0CH COM12
D5 0DH COM13
D6 0EH COM14
D7 0FH COM15
0 0 1 0 D0 Page 2 10H COM16
D1 11H COM17
D2 12H COM18
D3 13H COM19
D4 14H COM20
D5 15H COM21
D6 16H COM22
D7 17H COM23
1 1 0 1 D0 Page 13 68H COM104
D1 69H COM105
D2 6AH COM106
D3 6BH COM107
D4 6CH COM108
D5 6DH COM109
D6 6EH COM110
D7 6FH COM111
1 1 1 0 D0 Page 14 70H COM112
D1 71H COM113
D2 72H COM114
D3 73H COM115
D4 74H COM116
D5 75H COM117
D6 76H COM118
D7 77H COM119
1 1 1 1 D0 Page 15 78H COM120
D1 79H COM121
D2 7AH COM122
D3 7BH COM123
D4 7CH COM124
D5 7DH COM125
D6 7EH COM126
D7 7FH COM127
ICON D0 Page 16 80H COMS
ICON address just can set by ICON ON instruction
ADC 0 1
00 83 SEG0
01 82 SEG1
02 81 SEG2
03 80 SEG3
04 7F SEG4
05 7E SEG5
06 7D SEG6
07 7C SEG7
7C 07 SEG124
7D 06 SEG125
7E 05 SEG126
7F 04 SEG127
80 03 SEG128
81 02 SEG129
82 01 SEG130
83 00 SEG131
SEG

MODE 1

SEG output	SEG 0	SEG 1	SEG 2	SEG 3	…	SEG 156	SEG 157	SEG 158	SEG 159
Column address [Y9:Y2]	00H	01H	02H	03H	…	9CH	9DH	9EH	9FH
Internal column address [Y9:Y0]	00 01 02 03	04 05 06 07	08 09 0A 0B	0C 0D 0E 0F	…	270 271 272 273	274 275 276 277	278 279 27A 27B	27C 27D 27E 27F
Display data (ADC=0)	1 1 1 1	1 1 1 0	1 1 0 1	1 1 0 0	…	0 0 1 1	0 0 1 0	0 0 0 1	0 0 0 0
LCD panel display					…				
Display data (ADC=1)	0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	…	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1
LCD panel display					…				

Figure 10. The Relationship between the Column Address and the Segment Outputs

Mode-1 Display RAM Mapping diagram



LCD DISPLAY CIRCUITS

FRC (Frame Rate Control) and PWM (Pulse Width Modulation) Function Circuit

The ST7528 incorporates an FRC function and a PWM function circuit to display a 16-level gray scale. The FRC function and PWM utilize liquid crystal characteristics whose transmittance is changed by an effective

value of applied voltage. The ST7528 provides palette-registers to assign the desired gray level. These registers are set by the instructions and the RESETB.

– **Gray Scale Table of 4 FRC (Frame Rate Control)**

4 FRC setting	(DB7 to DB0)
1st FR (FR1)	Set 1st Frame Pulse Width Modulation Instruction
1st FR (FR1)	Set 1st Frame Pulse Width Modulation Data
2nd FR (FR2)	Set 2nd Frame Pulse Width Modulation Instruction
2nd FR (FR2)	Set 2nd Frame Pulse Width Modulation Data
3rd FR (FR3)	Set 3rd Frame Pulse Width Modulation Instruction
3rd FR (FR3)	Set 3rd Frame Pulse Width Modulation Data
4th FR (FR4)	Set 4th Frame Pulse Width Modulation Instruction
4th FR (FR4)	Set 4th Frame Pulse Width Modulation Data

Gray Scale Table of 3 FRC (Frame Rate Control)

3 FRC setting	(DB7 to DB0)
1st FR (FR1)	Set 1st Frame Pulse Width Modulation Instruction
1st FR (FR1)	Set 1st Frame Pulse Width Modulation Data
2nd FR (FR2)	Set 2nd Frame Pulse Width Modulation Instruction
2nd FR (FR2)	Set 2nd Frame Pulse Width Modulation Data
3rd FR (FR3)	Set 3rd Frame Pulse Width Modulation Instruction
3rd FR (FR3)	Set 3rd Frame Pulse Width Modulation Data
4th FR (FR4)	No used
4th FR (FR4)	No used

Gray Scale Table of 45 PWM (Pulse Width Modulation)

Dec	Hex	6-bits	PWM (on width)	Note
0	00	000000	0(0/45)	Brighter
1	01	000001	1/45	
2	02	000010	2/45	
3	03	000011	3/45	
4	04	000100	4/45	
...	...	...	...	
...	...	...	...	
...	...	...	...	
...	...	...	...	
42	2A	101010	42/45	
43	2B	101011	43/45	
44	2C	101100	44/45	
45	2D	101101	1(45/45)	Darker
...	...	...	...	This area is selected to OFF level (0/45 level)
...	...	...	...	
61	3D	111101	0/45	
62	3E	111110	0/45	
63	3F	111111	0/45	

-Gray Scale Table of 60 PWM (Pulse Width Modulation)

Dec	Hex	6-bits	PWM (on width)	Note
0	00	000000	0(0/60)	Brighter
1	01	000001	1/60	
2	02	000010	2/60	
3	03	000011	3/60	
4	04	000100	4/60	
...	...	...	...	
...	...	...	...	
...	...	...	...	
...	...	...	...	
...	...	...	...	
...	...	...	...	
56	39	111001	56/60	
57	3A	111010	57/60	
58	3B	111011	58/60	
59	3C	111100	59/60	
60	39	111001	1 (60/60)	Darker
61	3D	111101	0/60	This area is selected to OFF level (0/60 level)
62	3E	111110	0/60	
63	3F	111111	0/60	

Partial Display on LCD

The ST7528 realizes the Partial Display function on LCD with low-ratio driving for saving power consumption and showing the various display ratio. To show the various display ratio on LCD, LCD driving ratio and bias are programmable via the instruction. And, built-in power supply circuits are controlled by the instruction for adjusting the LCD driving voltages.

In mode 0 the partial display ratio could be set from 16 ~ 128.

In mode 1 could be set from 16 ~ 100.

If the partial display region is out of the Max. Display range, it would be no operation.

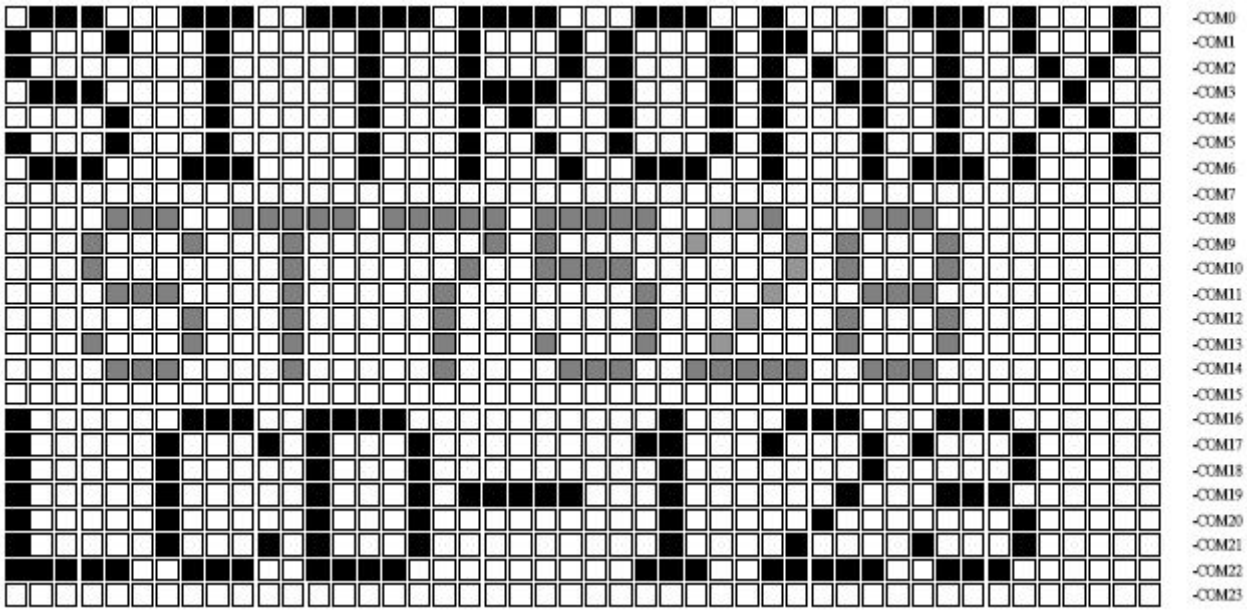


Figure 13 Reference Example for Partial Display

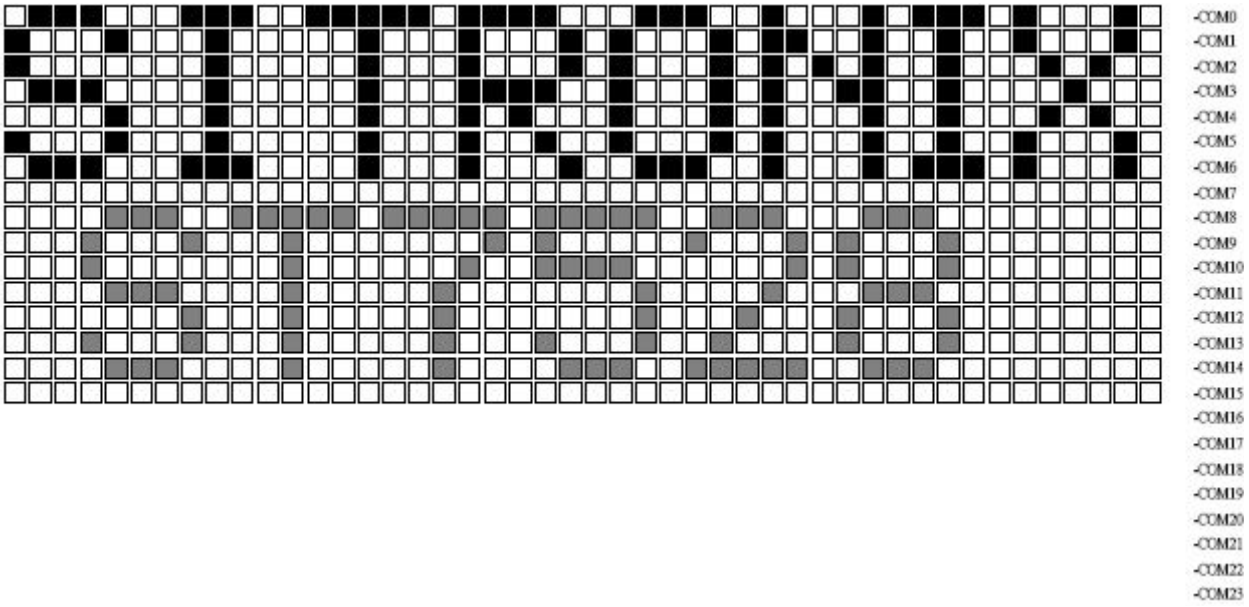


Figure 14 Partial Display (Partial Display ratio=16,initial COM0=0)

POWER SUPPLY CIRCUITS

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction. For details, refers to "Instruction Description". Table 4 shows the referenced combinations in using Power Supply circuits.

Table 4 Recommended Power Supply Combinations

User setup	Power control (VC VR VF)	V/C circuits	V/R circuits	V/F circuits	VOUT_IN	V0	V1 to V4
Only the internal power supply circuits are used	1 1 1	ON	ON	ON	Internal	Without capacitor	With capacitor
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	OFF	ON	ON	External input	Without capacitor	With capacitor
Only the voltage follower circuits are used	0 0 1	OFF	OFF	ON	OPEN	External input	With capacitor
Only the external power supply circuits are used	0 0 0	OFF	OFF	OFF	OPEN	External input	External input

Voltage Converter Circuits

These circuits boost up the electric potential between VDD2 and Vss to 3, 4, 5 or 6 times toward positive side and boosted voltage is outputted from VOUT pin. It is possible to select the lower boosting level in any boosting circuit by “Set DC-DC Step-up” instruction. When the higher level is selected by instruction, VOUT voltage is not valid.

Note: we would like to recommend to use the external VOUT when the panel is large than 1.8 inch

Voltage Regulator Circuits

The function of the internal Voltage Regulator circuits is to determine liquid crystal operating voltage, V0, by adjusting resistors, Ra and Rb, within the range of |V0| < |VOUT|. Because VOUT is the operating voltage of operational-amplifier circuits shown in Figure 16, it is necessary to be applied internally or externally.

For the Eq. 1, we determine V0 by Ra, Rb and VEV. The Ra and Rb are connected internally or externally by INTRS pin. And VEV called the voltage of electronic volume is determined by Eq. 2, where the parameter a is the value selected by instruction, "Set Reference Voltage Register", within the range 0 to 63. VREF voltage at Ta= 25°C is shown in Table 5.

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times VEV\ [V] \text{ ------ (Eq. 1)}$$

$$VEV = \left(1 - \frac{(63 - \alpha)}{210}\right) \times VREF\ [V] \text{ ------ (Eq. 2)}$$

Table 5 VREF Voltage at Ta = 25° C

REF	Temp. coefficient	VREF [V]
1	-0.125% / °C	2.1
0	External input	VEXT

In Case of Using Internal Resistors, Ra and Rb (INTRS = "H")
When INTRS pin is **"H"**, resistor Ra is connected internally between VR pin and VSS, and Rb is connected between V0 and VR. We determine V0 by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".
Table 6 Internal Rb / Ra Ratio depending on 3-bit Data (R2 R1 R0)

	3-bit data settings (R2 R1 R0)							
	0 0 0	**0 0 1**	**0 1 0**	**0 1 1**	**1 0 0**	**1 0 1**	**1 1 0**	**1 1 1**
1 + (Rb / Ra)	2.3	3.0	3.7	4.4	5.1	5.8	6.5	7.2

RESET CIRCUIT
Setting RESETB to “L” or Reset instruction can initialize internal function.
When RESETB becomes “L”, following procedure is occurred.
Page address: 0
Column address: 0
Read-modify-write: OFF
Display ON / OFF: OFF
Initial display line: 0 (first)
Initial COM0 register: 0 (COM0)
Partial display ratio: 1/128
Reverse display ON / OFF: OFF (normal)
N-line inversion register: 0 (disable)
Entire Display ON/OFF: OFF
ICON Control register ON/OFF: OFF (ICON disable)
Power control register (VC, VR, VF) = (0, 0, 0)
DC-DC converter circuit = (0, 0)
Booster Efficiency BE = (1)
Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)
Contrast Level: 32
LCD bias ratio: 1/12
COM Scan Direction: 0
ADC Select: 0
Oscillator: OFF
Power Save Mode: Release
Display Data Length register: 0 (for SPI mode)
All Gray Level Set : OFF
In Level0, 2, 4, 6, 8, 10, 12, 14 , the Gray Level palette register (GA5, GA4, GA3, GA2, GA1, GA0) = (0,0,0,0,0)
All Gray Level Set : OFF
In Level1, 3, 5, 7, 9, 11, 13, 15, the Gray Level palette register (GA5, GA4, GA3, GA2, GA1, GA0) = (1,1,1,1,1)
FRC, PWM mode: 4FRC, 45PWM
When RESET instruction is issued, following procedure is occurred.
Page address: 0

Column address: 0
Read-modify-write: OFF
Initial display line: 0 (First)
Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)
Contrast Level: 32
Display Data Length register: 0 (for SPI mode)
All Gray Level Set : OFF
In Level0, 2, 4, 6, 8, 10, 12, 14 , the Gray Level palette register (GA5, GA4, GA3, GA2, GA1, GA0) = (0,0,0,0,0)
All Gray Level Set : OFF
In Level1, 3, 5, 7, 9, 11, 13, 15, the Gray Level palette register (GA5, GA4, GA3, GA2, GA1, GA0) = (1,1,1,1,1)
FRC, PWM mode: 4FRC, 45PWM
While RESETB is “L” or reset instruction is executed, no instruction except read status can be accepted. Reset status appears at DB4. After DB4 becomes ”L”, any instruction can be accepted. RESETB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESETB is essential before used.

10. Table of LCM commands

Instruction	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
EXT=0 or 1											
Mode Set	0	0	0	0	1	1	1	0	0	0	2-byte instruction to set Mode and FR(Frame frequency control) BE(Booster efficiency control)
	0	0	FR3	FR2	FR1	FR0	0	BE	x'	EXT	
EXT=0											
Read display data	1	1	Read data								Read data into DDRAM
Write display data	1	0	Write data								Write data into DDRAM
Read status	0	1	BUSY	ON	RES	MF2	MF1	MF0	DS1	DS0	Read the internal status
ICON control register ON/OFF	0	0	1	0	1	0	0	0	1	ICON	ICON=0: ICON disable(default) ICON=1: ICON enable & set the page address to 16
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	Y9	Y8	Y7	Y6	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y5	Y4	Y3	Y2	Set column address LSB
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	release modify-read mode
Display ON/OFF	0	0	1	0	1	0	1	1	1	D	D=0: Display OFF D=1: Display ON
Set initial display line register	0	0	0	1	0	0	0	0	x'	x'	2-byte instruction to specify the initial display line to realize vertical scrolling
	0	0	x'	S6	S5	S4	S3	S2	S1	S0	
Set initial COM0 register	0	0	0	1	0	0	0	1	x'	x'	2-byte instruction to specify the initial COM0 to realize window scrolling
	0	0	x'	C6	C5	C4	C3	C2	C1	C0	
Select partial display line	0	0	0	1	0	0	1	0	x'	x'	2-byte instruction to set partial display ratio
	0	0	D7	D6	D5	D4	D3	D2	D1	D0	
Set N-line inversion	0	0	0	1	0	0	1	1	x'	x'	2-byte instruction to set N-line inversion register
	0	0	x'	x'	x'	N4	N3	N2	N1	N0	
Release N-line inversion	0	0	1	1	1	0	0	1	0	0	Release N-line inversion mode
Reverse display ON/OFF	0	0	1	0	1	0	0	1	1	REV	REV=0: normal display REV=1: reverse display
Entire display ON/OFF	0	0	1	0	1	0	0	1	0	EON	EON=0: normal display EON=1: entire display ON

Instruction	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Ext=0											
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Select DC-DC step-up	0	0	0	1	1	0	0	1	DC1	DC0	Select the step-up of internal voltage converter
Select regulator register	0	0	0	0	1	0	0	R2	R1	R0	Select the internal resistance ratio of the regulator resistor
Select electronic volumn register	0	0	1	0	0	0	0	0	0	1	2-byte instruction to specify the reference voltage
	0	0	x'	x'	EV5	EV4	EV3	EV2	EV1	EV0	
Select LCD bias	0	0	0	1	0	1	0	B2	B1	B0	Select LCD bias
Set Bias Power Save Mode	0	0	1	1	1	1	0	0	1	1	Bias Power save Save the Bias current consumption
	0	0	0	0	0	0	0	0	0	0	
Release Bias Power Save Mode	0	0	1	1	1	1	0	0	1	1	Bias Power save release set the Bias power to normal
	0	0	0	0	0	0	0	1	0	0	
SHL select	0	0	1	1	0	0	SHL	x'	x'	x'	COM bi-directional selection SHL=0: normal direction SHL=1: reverse direction
ADC select	0	0	1	0	1	0	0	0	0	ADC	SEG bi-direction selection ADC=0: normal direction ADC=1: reverse direction
Oscillator on start	0	0	1	0	1	0	1	0	1	1	Start the built-in oscillator
Set power save mode	0	0	1	0	1	0	1	0	0	P	P=0: normal mode P=1: sleep mode
Release power save mode	0	0	1	1	1	0	0	0	0	1	release power save mode
Reset	0	0	1	1	1	0	0	0	1	0	initial the internal function
Set data direction & display data length(DDL)	x'	x'	1	1	1	0	1	0	0	0	2-byte instruction to specify the number of data bytes. (SPI mode)
	x'	x'	D7	D6	D5	D4	D3	D2	D1	D0	
Select FRC and PWM mode	0	0	1	0	0	1	0	FRC	PWM1	PWM0	FRC(1:3FRC, 0:4FRC) PWM1 PWM0 0 0 45PWM 0 1 45 PWM 1 0 60PWM 1 1 ---
NOP	0	0	1	1	1	0	0	0	1	1	*No operation*
Test Instruction	0	0	1	1	1	1	x'	x'	x'	x'	*Don't use this instruction*

Instruction	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
EXT=1											
Set white mode and 1st frame,	0	0	1	0	0	0	0	0	0	0	Set white mode and 1st frame
set pulse width	0	0	X'	X'	GA05	GA04	GA03	GA02	GA01	GA00	
Set white mode and 2nd frame,	0	0	1	0	0	0	0	0	0	1	Set white mode and 2nd frame
set pulse width	0	0	X'	X'	GA05	GA04	GA03	GA02	GA01	GA00	
Set white mode and 3rd frame,	0	0	1	0	0	0	0	0	1	0	Set white mode and 3rd frame
set pulse width	0	0	X'	X'	GA05	GA04	GA03	GA02	GA01	GA00	
Set white mode and 4th frame,	0	0	1	0	0	0	0	0	1	1	Set white mode and 4th frame
set pulse width	0	0	X'	X'	GA05	GA04	GA03	GA02	GA01	GA00	
Set gray level 1 mode	0	0	84H~87H (4 bytes)								Set gray level1
Set gray level 2 mode	0	0	88H~8BH (4 bytes)								Set gray level2
Set gray level 3 mode	0	0	8CH~8FH (4bytes)								Set gray level3
Set gray level 4 mode	0	0	90H~93H (4bytes)								Set gray level4
Set gray level 5 mode	0	0	94H~97H (4bytes)								Set gray level5
Set gray level 6 mode	0	0	98H~9BH (4 bytes)								Set gray level6
Set gray level 7 mode	0	0	9CH~9FH (4 bytes)								Set gray level7
Set gray level 8 mode	0	0	A0H~A3H (4 bytes)								Set gray level8
Set gray level 9 mode	0	0	A4H~A7H (4 bytes)								Set gray level9
Set gray level 10 mode	0	0	A8H~ABH (4 bytes)								Set gray level10
Set gray level 11mode	0	0	ACH~AFH (4 bytes)								Set gray level11
Set gray level 12 mode	0	0	B0H~B3H (4 bytes)								Set gray level12
Set gray level 13 mode	0	0	B4H~B7H (4 bytes)								Set gray level13
Set gray level 14 mode	0	0	B8H~BBH (4 bytes)								Set gray level14
Set Dark mode and 1st frame,	0	0	1	0	1	1	1	1	0	0	Set Dark mode and 1st frame, set pulse width
set pulse width	0	0	X'	X'	GAF5	GAF4	GAF3	GAF2	GAF1	GAF0	
Set Dark mode and 2nd frame,	0	0	1	0	1	1	1	1	0	1	Set Dark mode and 2nd frame, set pulse width
set pulse width	0	0	X'	X'	GAF5	GAF4	GAF3	GAF2	GAF1	GAF0	
Set Dark mode and 3rd frame,	0	0	1	0	1	1	1	1	1	0	Set Dark mode and 3rd frame, set pulse width
set pulse width	0	0	X'	X'	GAF5	GAF4	GAF3	GAF2	GAF1	GAF0	
Set Dark mode and 4th frame,	0	0	1	0	1	1	1	1	1	1	Set Dark mode and 4th frame, set pulse width
set pulse width	0	0	X'	X'	GAF5	GAF4	GAF3	GAF2	GAF1	GAF0	

Set Mode Register

2-byte instruction to set Mode (EXT) and FR (Frame frequency control), BE (Booster efficiency control).

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	0	0

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	FR3	FR2	FR1	FR0	0	BE	x'	EXT

Frame frequency

This command is used to set the frame frequency. This table is suitable for no partial display

FR3	FR2	FR1	FR0	FR frequency
0	0	0	0	77 Hz ±5%
0	0	0	1	51 Hz ±20%
0	0	1	0	55 Hz ±20%
0	0	1	1	58 Hz ±20%
0	1	0	0	63 Hz ±20%
0	1	0	1	67 Hz ±20%
0	1	1	0	68 Hz ±20%
0	1	1	1	70 Hz ±20%
1	0	0	0	73 Hz ±20%
1	0	0	1	75 Hz ±20%
1	0	1	0	80 Hz ±20%
1	0	1	1	85 Hz ±20%
1	1	0	0	91 Hz ±20%
1	1	0	1	102 Hz ±20%
1	1	1	0	113 Hz ±20%
1	1	1	1	123 Hz ±20%

Booster Efficiency

The ST7528 incorporates software configurable Booster Efficiency Command. It could be used with Voltage multiplier to get the suitable Vout and Power consumption. Default setting is Level 2

Flag	Description	
BE	0	Booster Efficiency Level 1
	1	Booster Efficiency Level 2

Mode Set

Flag	Description	
EXT	Default	EXT=0
	EXT=0	The Instruction of EXT=0 Mode is available
	EXT=1	The Instruction of EXT=1 Mode is available

Read Display Data

8-bit data from Display Data RAM specified by the column address and page address can be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display Data cannot be read through the serial interface.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read data							

Write Display Data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor

can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Write data							

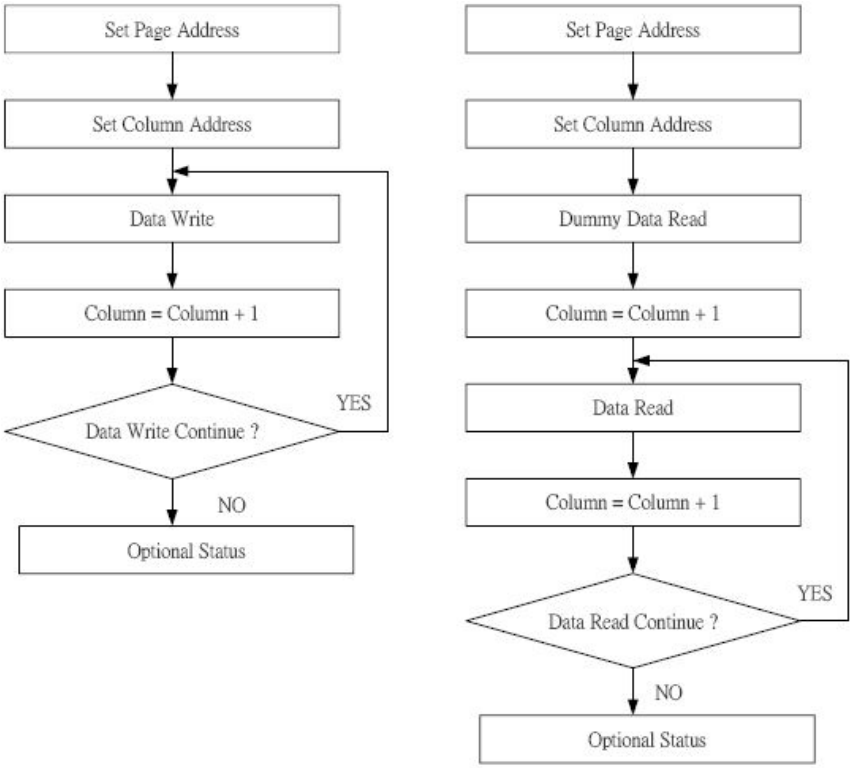


Figure 18 Sequence for Writing Display Data (Left) and Sequence for Reading Display Data (Right)

Read Status

Indicates the internal status of the ST7528

A0	**RW**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
0	1	BUSY	ON	RES	MF2	MF1	MF0	DS1	DS0

Flag	**Description**
BUSY	The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes Low. 0: chip is active, 1: chip is being busy
ON	Indicates display ON / OFF status 0: display OFF, 1: display ON
RESET	Indicates the initialization is in progress by RESET signal. 0: chip is active, 1: chip is being reset
MF	Manufacturer ID; suggest value: MF2 MF1 MF0 = [0 0 0] The value of MF2, MF1 and MF0 will follow the hardware selection.
DS	Display size ID; suggest value: DS1 DS0 = [1 0] The value of DS1 and DS2 will follow the hardware selection.

Set Page Address

Sets the Page Address of display data RAM from the microprocessor into the page address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write or read display data. Changing the Page Address doesn't affect the display status. Set Page Address instruction can not be used to set the page address to “16”. Use ICON control register ON/OFF instruction to set the page address to “16”.

A0	**RW**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
0	0	1	0	1	1	P3	P2	P1	P0

P3	P2	P1	P0	**Page**
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
1	1	1	0	14
1	1	1	1	15

Set Column Address
Sets the Column Address of display RAM from the microprocessor into the column address register. Along with the Column Address, the Column Address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display data to or from display RAM, Column Addresses are automatically increased.

Set Column Address MSB

A0	**RW**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
0	0	0	0	0	1	Y9	Y8	Y7	Y6

Set Column Address LSB

A0	**RW**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
0	0	0	0	0	0	Y5	Y4	Y3	Y2

Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	**Column address[Y9:Y2]**
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	0	126
0	1	1	1	1	1	1	1	127
:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	1	0	158
1	0	0	1	1	1	1	1	159

Set Modify-Read
This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset Modify-Read instruction.

A0	**RW**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
0	0	1	1	1	0	0	0	0	0

Reset Modify-Read
This instruction cancels the Modify-Read mode, and makes the column address return to its initial value just before the set Modify-Read instruction is started.

A0	**RW**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
0	0	1	1	1	0	1	1	1	0

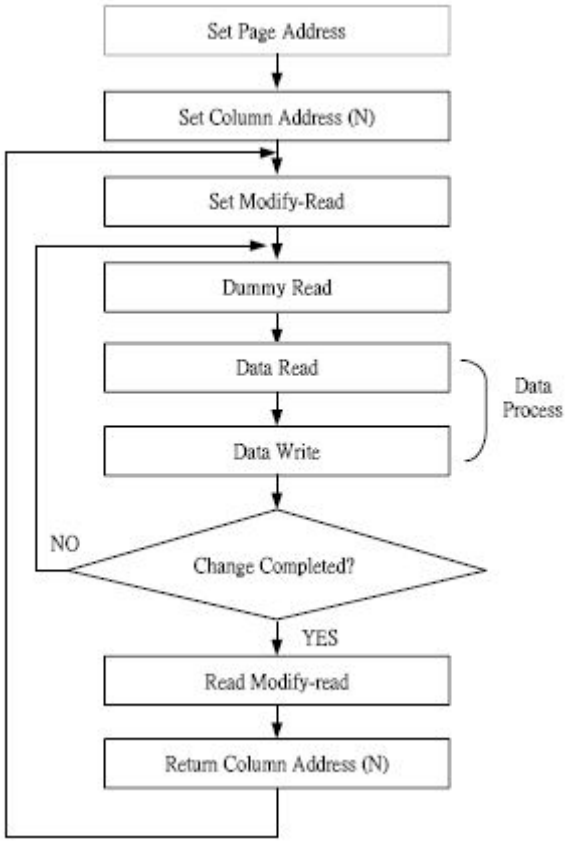


Figure 19 Sequence for Cursor Display

Display ON / OFF

Turns the display ON or OFF.

This command has priority over Entire Display On/Off and Reverse Display On/Off. Commands are accepted while the display is off, but the visual state of the display does not change.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	DON

DON = 1: display ON
DON = 0: display OFF

Set Initial Display Line Register

Sets the line address of display RAM to determine the initial display line using 2-byte instruction. The RAM display data is displayed at the top of row (COM0) of LCD panel.

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	0	x	x

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	S6	S5	S4	S3	S2	S1	S0

S6	S5	S4	S3	S2	S1	S0	Line address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:
1	1	0	0	1	0	0	125
							126
1	1	1	1	1	1	1	127

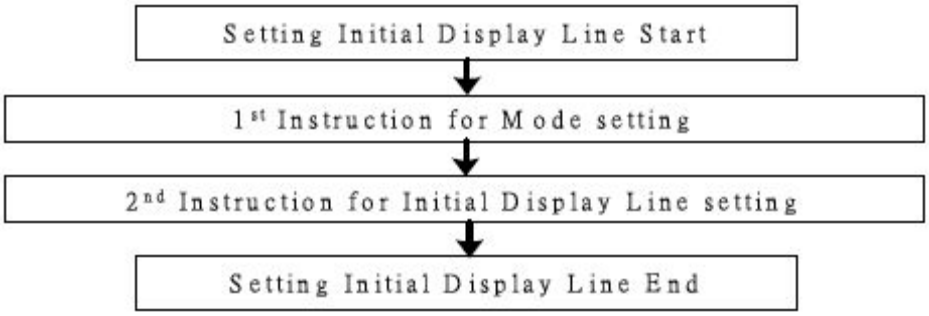


Figure 20 Sequence For Setting Initial Display Line

Set Initial COM0 Register

Sets the initial row (COM) of the LCD panel using the 2-byte instruction. By using this instruction, it is possible to realize the window moving without the change of display data.

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	1	x	x

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	C6	C5	C4	C3	C2	C1	C0

C6	C5	C4	C3	C2	C1	C0	**Initial COM0**
0	0	0	0	0	0	0	COM0
0	0	0	0	0	0	1	COM1
0	0	0	0	0	1	0	COM2
0	0	0	0	0	1	1	COM3
:	:	:	:	:	:	:	:
1	1	1	1	1	0	0	COM124
1	1	1	1	1	0	1	COM125
1	1	1	1	1	1	0	COM126
1	1	1	1	1	1	1	COM127

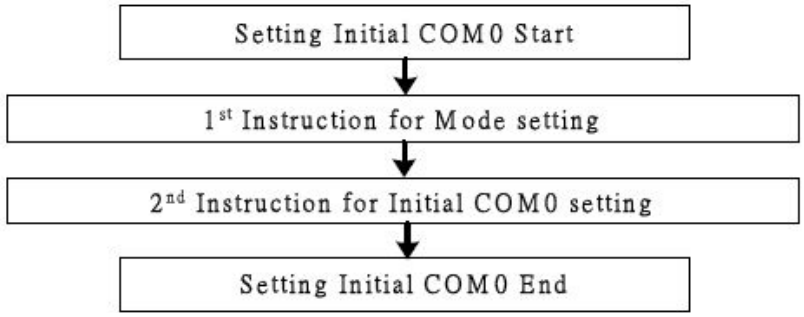


Figure 21 Sequence For Setting Initial COM

Select partial display line

Sets the ratio within range of 16 to 128 (ICON disabled) or 17 to 129 (ICON enabled) to realize partial display by using the 2-byte instruction.

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	0	x	x

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	D7	D6	D5	D4	D3	D2	D1	D0

D7	D6	D5	D4	D3	D2	D1	D0	Selected partial Display line mode 0	Selected partial Display line mode 1
0	0	0	0	0	0	0	0	No operation	No operation
:	:	:	:	:	:	:	:		
0	0	0	0	1	1	1	1		
0	0	0	1	0	0	0	0	1/16	1/16
0	0	0	1	0	0	0	1	1/17	1/17
:	:	:	:	:	:	:	:	:	:
0	1	1	0	0	1	0	0	1/100	1/100
:	:	:	:	:	:	:	:	:	1/100
0	1	1	1	1	1	1	1	1/127	1/100
1	0	0	0	0	0	0	0	1/128	1/100
1	0	0	0	0	0	0	1	No Operation	No Operation
:	:	:	:	:	:	:	:		
1	1	1	1	1	1	1	1		

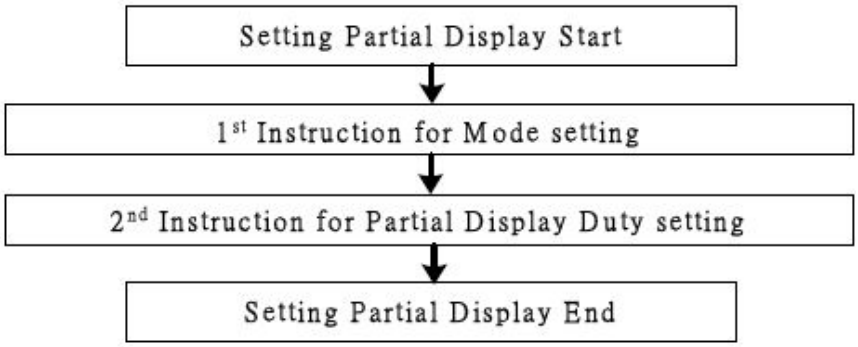


Figure 22 Sequence For Setting Partial Display

Set N-line Inversion Register

Sets the inverted line number within range of 3 to 33 to improve the display quality by controlling the phase of the internal LCD AC signal (M) by using the 2-byte instruction. The DC-bias problem could be occurred if K is even number. So, we recommend customers to set K to be odd number. K :
D/N
D : The number of display ratio (D is selectable by customers)
N : N for N-line inversion (N is selectable by customers).

The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	1	x	x

The 2st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	x	x	N4	N3	N2	N1	N0

N4	N3	N2	N1	N0	Selected n-line inversion
0	0	0	0	0	0-line inversion (frame inversion)
0	0	0	0	1	3-line inversion
0	0	0	1	0	4-line inversion
0	0	0	1	1	5-line inversion
:	:	:	:	:	:
1	1	1	0	1	31-line inversion
1	1	1	1	0	32-line inversion
1	1	1	1	1	33-line inversion

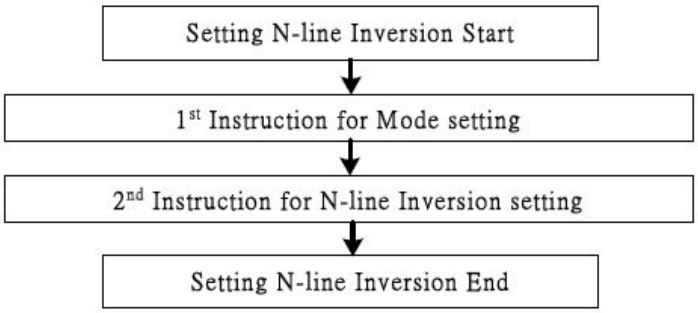


Figure 23 Sequence For N-line Inversion

Release N-line Inversion

Returns to the frame inversion condition from the n-line inversion condition.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	1	0	0

Reverse Display ON / OFF

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	White	Gray level 1	…..	Gray level 14	– Dark
0 (normal)	White (“0000”)	Gray 1 (“0001”)	…..	Gray 14 (“1110”)	Dark (“1111”)
1 (reverse)	Dark (“1111”)	Gray 14 (“1110”)	…..	Gray 1 (“0001”)	White (“0000”)

Entire Display ON / OFF

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priority over the Reverse Display ON / OFF instruction.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

Entire	White	Gray level 1	…..	Gray level 14	– Dark
0 (normal)	White (“0000”)	Gray 1 (“0001”)	…..	Gray 14 (“1110”)	Dark (“1111”)
1 (Entire)	Dark (“1111”)	Dark (“1111”)	Dark (“1111”)	Dark (“1111”)	Dark (“1111”)

Power Control

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

VC	VR	VF	Status of internal power supply circuits
0			Internal voltage converter circuit is OFF
1			Internal voltage converter circuit is ON
	0		Internal voltage regulator circuit is OFF
	1		Internal voltage regulator circuit is ON
		0	Internal voltage follower circuit is OFF
		1	Internal voltage follower circuit is ON

Set Bias Power Save Mode
Consist of 2-byte Instructions
The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	0	1	1

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0

This command is for saving the IC current consumption by Bias Power Saving
After this Instruction is set, Bias function is also working

Release Bias Power Save Mode
Consist of 2-byte Instructions
The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	0	1	1

The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	0	0

This command is for release Bias Power Save

Select DC-DC Step-up
Selects one of 4 DC-DC step-up to reduce the power consumption by this instruction. It is very useful to realize the partial display function.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	0	1	DC1	DC0

DC1	DC0	Selected DC-DC converter circuit
0	0	3 times boosting circuit
0	1	4 times boosting circuit
1	0	5 times boosting circuit
1	1	6 times boosting circuit

Select Regulator Resistor
Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit. Refer to the Table 6.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	1+ (Rb / Ra)
0	0	0	2.3
0	0	1	3.0
0	1	0	3.7
0	1	1	4.4
1	0	0	5.1
1	0	1	5.8
1	1	0	6.5
1	1	1	7.2

Set Electronic Volume Register
Consist of 2-byte Instructions
The 1st instruction set Reference Voltage mode, the 2nd one updates the contents of reference voltage register. After second instruction, Reference Voltage mode is released.

The 1st Instruction: Set Reference Voltage Select Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

The 2nd Instruction: Set Reference Voltage Register

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	x	EV5	EV4	EV3	EV2	EV1	EV0

EV5	EV4	EV3	EV2	EV1	EV0	Reference voltage parameter (a)
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

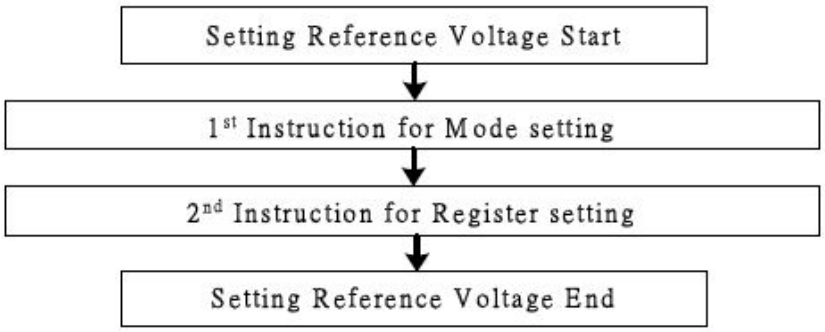


Figure 24 Sequence For Setting the Electronic Volume

Select LCD Bias

Selects LCD bias ratio of the voltage required for driving the LCD.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	0	B2	B1	B0

B2	B1	B0	LCD bias
0	0	0	1/5
0	0	1	1/6
0	1	0	1/7
0	1	1	1/8
1	0	0	1/9
1	0	1	1/10
1	1	0	1/11
1	1	1	1/12

SHL Select

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	x	x	x

In Mode 0
SHL = 0: normal direction (COM0 -> COM127) SHL = 1: reverse direction (COM127-> COM0)

In Mode 1
SHL = 0: normal direction (COM0 -> COM99) SHL = 1: reverse direction (COM99 -> COM0)

ADC Select
Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins could be reversed by software. This makes IC layout flexible in LCD module assembly.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

In Mode 0
ADC = 0: normal direction (SEG0 -> SEG127) ADC = 1: reverse direction (SEG127 -> SEG0)
In Mode 1
ADC = 0: normal direction (SEG0-> SEG159) ADC = 1: reverse direction (SEG159 -> SEG)

Oscillator ON Start
This instruction enables the built-in oscillator circuit.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1

Power Save
The ST7528 enters the Power Save status to reduce the power consumption to the static power consumption value and returns to the normal operation status by the following instructions.

Set Power Save Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	P

P = 0: normal mode
P = 1: sleep mode

Release Power Save Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	1

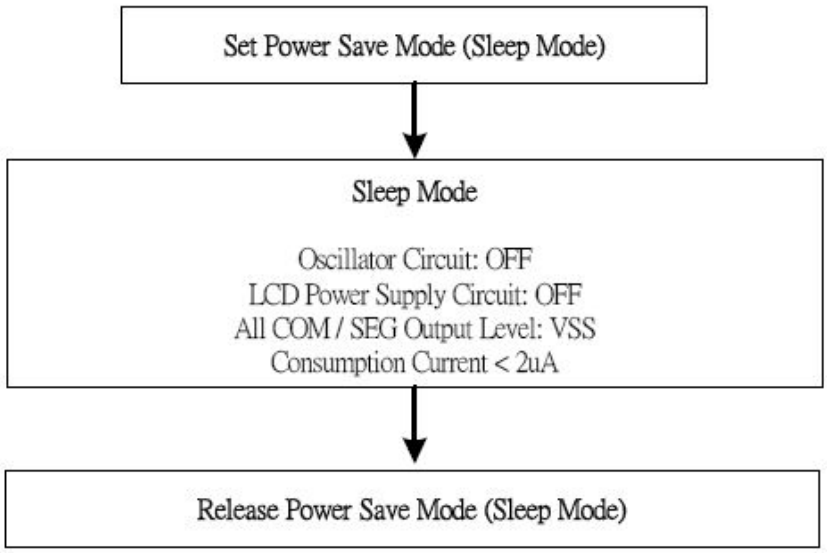


Figure 25 Power Save Routine

Reset
This instruction Resets initial display line, column address, page address, and common output status select to their initial status, but dose not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the RESETB pin.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

Set Data Direction & Display Data Length (3-Line SPI Mode)
Consists of 2 bytes instruction.
This command is used in 3-Line SPI mode only (PS0 = ”L” and PS1 = ”L”). It will be two continuous commands, the first byte control the data direction(write mode only) and inform the LCD driver the second byte will be number of data bytes will be write. When A0 is not used, the Display Data Length instruction is used to indicate that a specified number of display data bytes are to be transmitted. The next byte after the display data string is handled as command data.
The 1st Instruction: Set Data Direction (Only Write Mode)

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
x	x	1	1	1	0	1	0	0	0

The 2nd Instruction: Set Display Data Length (DDL) Register

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
x	x	D7	D6	D5	D4	D3	D2	D1	D0

D7	D6	D5	D4	D3	D2	D1	D0	Display Data Length
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	1	254
1	1	1	1	1	1	1	0	255
1	1	1	1	1	1	1	1	256

NOP
No operation

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

Test Instruction
This instruction is for testing IC. Please do not use it.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	x	x	x	x

Set FRC & PWM mode
Selects 3/4 FRC and 45 / 60 PWM

FRC	PWM1	PWM0	Status of PWM & FRC
0			4FRC
1			3FRC
	0	0	45PWM
	0	1	45PWM
	1	0	60PWM
	1	1	---

NOTE: the value of register could not set [PWM1:PWM0]=[1:1]
Set Gray Scale Mode & Register
Consists of 2 bytes instruction. The first byte sets grayscale mode and the second byte updates the contents of gray scale register without issuing any other instruction.

- **Set Gray Scale Mode**

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	GRAY3	GRAY2	GRAY1	GRAY0	FRAMX1	FRAMX0

GRAY3	GRAY2	GRAY1	GRAY0	FRAMX1	FRAMX0	Description
0	0	0	0	0	0	In case of setting whit mode and 1st frame
0	0	0	0	0	1	In case of setting whit mode and 2nd frame
0	0	0	0	1	0	In case of setting whit mode and 3rd frame
0	0	0	0	1	1	In case of setting whit mode and 4th frame
0	0	0	1	0	0	In case of setting GRAY LEVEL 1 mode and 1st frame
0	0	0	1	0	1	In case of setting GRAY LEVEL 1 mode and 2 rd frame
0	0	0	1	1	0	In case of setting GRAY LEVEL 1 mode and 3rd frame
:	:	:	:	:	:	:
1	1	1	0	0	1	In case of setting GRAY LEVEL 14 mode and 2nd frame
1	1	1	0	1	0	In case of setting GRAY LEVEL 14 mode and 3rd frame
1	1	1	0	1	1	In case of setting GRAY LEVEL 14 mode and 4th frame
1	1	1	1	0	0	In case of setting dark mode and 1st frame
1	1	1	1	0	1	In case of setting dark mode and 2nd frame
1	1	1	1	1	0	In case of setting dark mode and 3rd frame
1	1	1	1	1	1	In case of setting dark mode and 4th frame

Set Gray Scale Register

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	X	X	GAX5	GAX4	GAX3	GAX2	GAX1	GAX0

GAX5	GAX4	GAX3	GAX2	GAX1	GAX0	Pulse width (45 PWM)	Pulse width (60 PWM)
0	0	0	0	0	0	0/45	0/60
0	0	0	0	0	1	1/45	1/60
0	0	0	0	1	0	2/45	2/60
0	0	0	0	1	1	3/45	3/60
0	0	0	1	0	0	4/45	4/60
:	:	:	:	:	:	:	:
1	0	1	0	1	1	43/45	43/60
1	0	1	1	0	0	44/45	44/60
1	0	1	1	0	1	45/45	45/60
1	0	1	1	1	0	0/45	46/60
1	0	1	1	1	1	0/45	47/60
:	:	:	:	:	:	:	:
1	1	1	0	1	1	0/45	59/60
1	1	1	1	0	0	0/45	60/60
1	1	1	1	0	1	0/45	0/60
:	:	:	:	:	:	:	:
1	1	1	1	1	1	0/45	0/60

COMMAND DESCRIPTION

Referential Instruction Setup Flow: Initializing with the built-in Power Supply Circuits

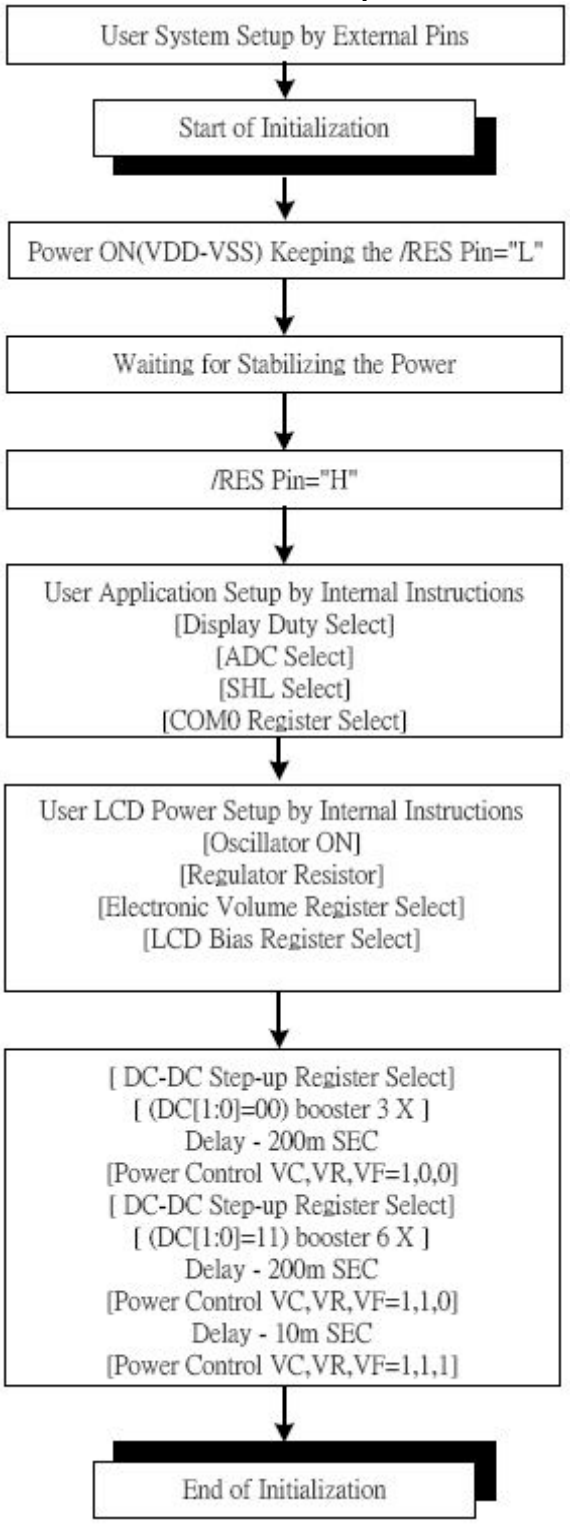


Figure 26 Initializing with the Built-in Power Supply Circuits

Referential Instruction Setup Flow: Initializing without the built-in Power Supply Circuits

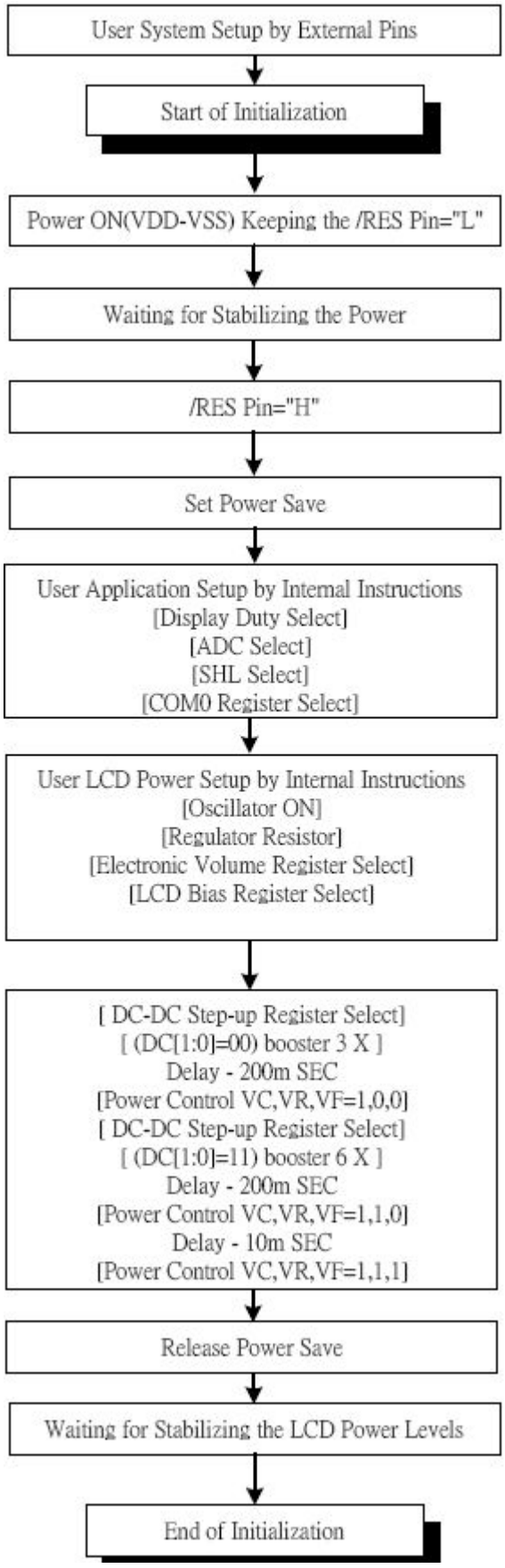


Figure 27 Initializing without Built-in Power Supply Circuits

Referential Instruction Setup Flow: Data Displaying

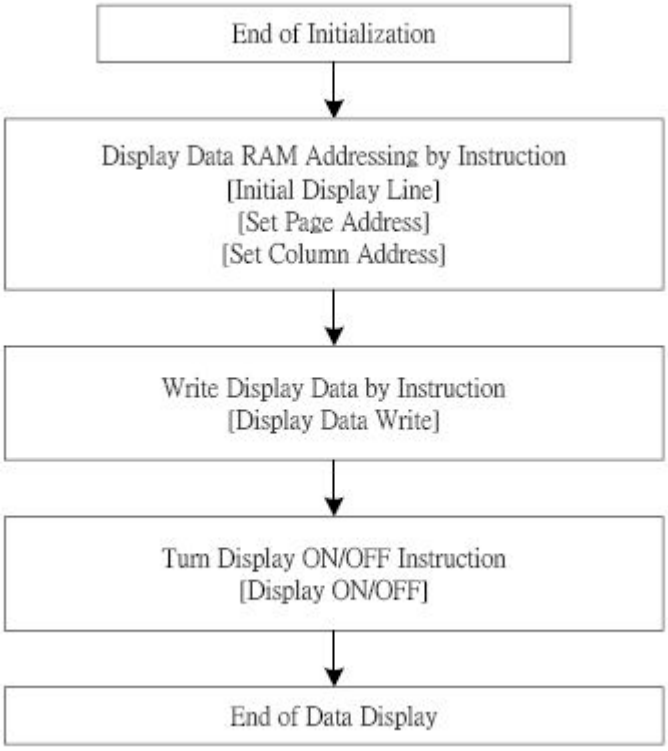


Figure 28 Data Displaying

Referential Instruction Setup Flow: Power OFF

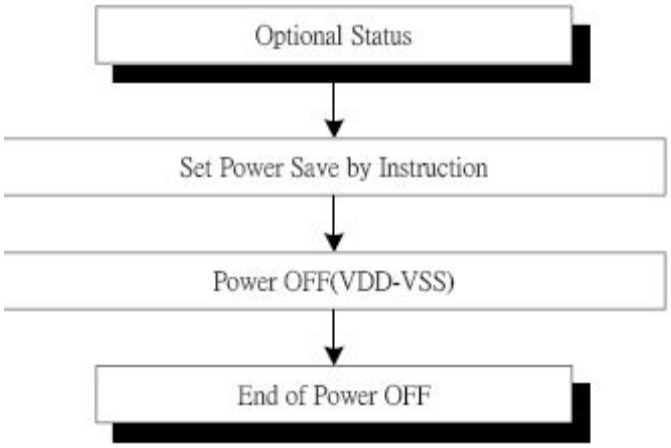


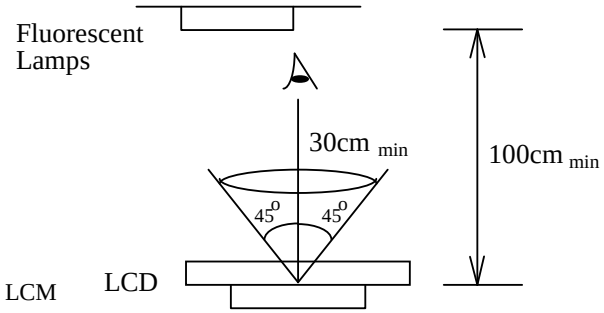
Figure 29 Power OFF

11.QUALITY SPECIFICATIONS

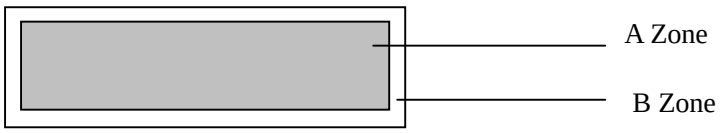
11.1 Standard of the product appearance test

Manner of appearance test: The inspection should be performed in using 20W x 2 fluorescent lamps. Distance between LCM and fluorescent lamps should be 100 cm or more. Distance between LCM and inspector eyes should be 30 cm or more.

Viewing direction for inspection is 45° from vertical against LCM.



Definition of zone:



A Zone: Active display area (minimum viewing area).
B Zone: Non-active display area (outside viewing area).

11.2 Specification of quality assurance

AQL inspection standard

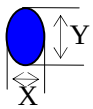
Sampling method: MIL-STD-105E, Level II, single sampling

Defect classification **(Note: * is not including)**

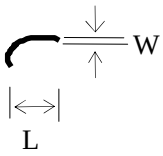
Classify	Item		Note	AQL
Major	Display state	Short or open circuit	1	0.65
		LC leakage		
		Flickering		
		No display		
		Wrong viewing direction		
		Contrast defect (dim, ghost)	2	
		Back-light	1,8	
	Non-display	Flat cable or pin reverse	10	
		Wrong or missing component	11	
Minor	Display state	Background color deviation	2	1.0
		Black spot and dust	3	
		Line defect, Scratch	4	
		Rainbow	5	
		Chip	6	
		Pin hole	7	
	Polarizer	Protruded	12	
		Bubble and foreign material	3	
	Soldering	Poor connection	9	
	Wire	Poor connection	10	
	TAB	Position, Bonding strength	13	

Note on defect classification

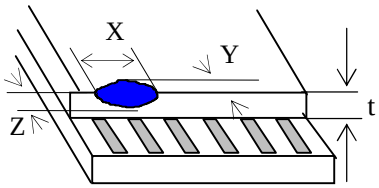
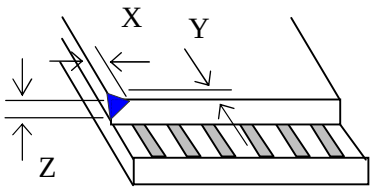
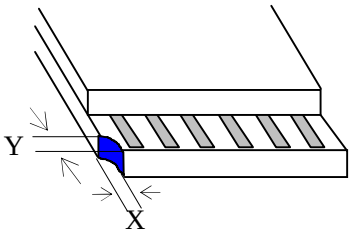
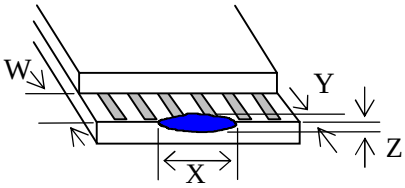
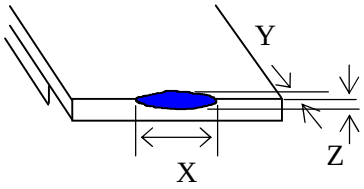
<table>
<tr><th>No.</th><th>Item</th><th>Criterion</th></tr>
<tr><td rowspan="6">1</td><td>Short or open circuit</td><td rowspan="6">Not allow</td></tr>
<tr><td>LC leakage</td></tr>
<tr><td>Flickering</td></tr>
<tr><td>No display</td></tr>
<tr><td>Wrong viewing direction</td></tr>
<tr><td>Wrong Back-light</td></tr>
<tr><td rowspan="2">2</td><td>Contrast defect</td><td rowspan="2">Refer to approval sample</td></tr>
<tr><td>Background color deviation</td></tr>
<tr><td>3</td><td>Point defect,
Black spot, dust
(including Polarizer)

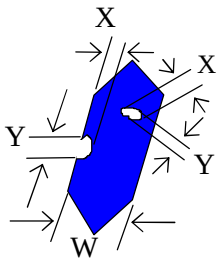
ϕ = (X+Y)/2</td><td> 

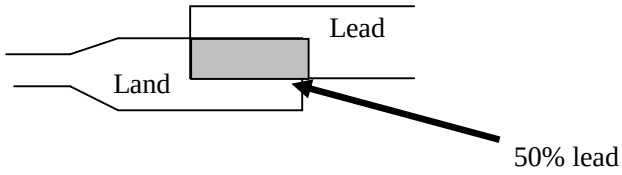
<table>
<tr><th>Point Size</th><th>Acceptable Qty.</th></tr>
<tr><td>ϕ≤0.10</td><td>Disregard</td></tr>
<tr><td>0.10<ϕ≤0.20</td><td>3</td></tr>
<tr><td>0.20<ϕ≤0.25</td><td>2</td></tr>
<tr><td>0.25<ϕ≤0.30</td><td>1</td></tr>
<tr><td>ϕ>0.30</td><td>0</td></tr>
</table>
Unit: mm</td></tr>
<tr><td>4</td><td>Line defect,

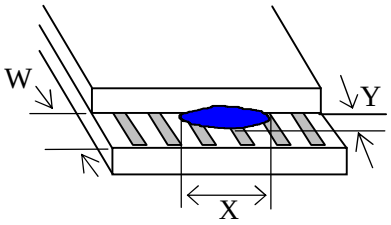
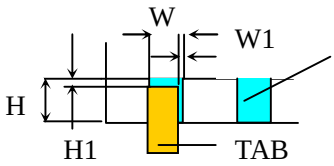
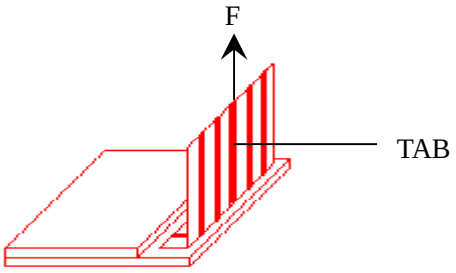
Scratch</td><td> 

<table>
<tr><th colspan="2">Line</th><th>Acceptable Qty.</th></tr>
<tr><td>L</td><td>W</td><td></td></tr>
<tr><td>---</td><td>0.015≥W</td><td>Disregard</td></tr>
<tr><td>3.0≥L</td><td>0.03≥W</td><td rowspan="2">2</td></tr>
<tr><td>2.0≥L</td><td>0.05≥W</td></tr>
<tr><td>1.0≥L</td><td>0.1>W</td><td>1</td></tr>
<tr><td>---</td><td>0.05<W</td><td>Applied as point defect</td></tr>
</table>
Unit: mm</td></tr>
<tr><td>5</td><td>Rainbow</td><td>Not more than two color changes across the viewing area.</td></tr>
</table>

No	Item	Criterion
6	Chip Remark: X: Length direction Y: Short direction Z: Thickness direction t: Glass thickness W: Terminal Width	 Acceptable criterion X: ≤2; Y: 0.5mm; Z: ≤t/2  Acceptable criterion X: ≤2; Y: 0.5mm; Z: ≤t  Acceptable criterion X: ≤3; Y: ≤2; Z: ≤t shall not reach to ITO  Acceptable criterion X: Disregard; Y: ≤0.2; Z: ≤t  Acceptable criterion X: ≤5; Y: ≤2; Z: ≤t/3

<table>
<tr><th>No.</th><th>Item</th><th>Criterion</th></tr>
<tr><td>7</td><td>Segment
pattern
W = Segment width
ϕ = (X+Y)/2</td><td>(1) Pin hole
ϕ < 0.10mm is acceptable.
 

<table>
<tr><th>Point Size</th><th>Acceptable Qty</th></tr>
<tr><td>ϕ≤1/4W</td><td>Disregard</td></tr>
<tr><td>1/4W< ϕ≤1/2W</td><td>1</td></tr>
<tr><td>ϕ>1/2W</td><td>0</td></tr>
</table>
Unit: mm</td></tr>
<tr><td>8</td><td>Back-light</td><td>(1) The color of backlight should correspond its specification.
(2) Not allow flickering</td></tr>
<tr><td>9</td><td>Soldering</td><td>(1) Not allow heavy dirty and solder ball on PCB.
(The size of dirty refer to point and dust defect)
(2) Over 50% of lead should be soldered on Land.
 
</td></tr>
<tr><td>10</td><td>Wire</td><td>(1) Copper wire should not be rusted
(2) Not allow crack on copper wire connection.
(3) Not allow reversing the position of the flat cable.
(4) Not allow exposed copper wire inside the flat cable.</td></tr>
<tr><td>11*</td><td>PCB</td><td>(1) Not allow screw rust or damage.
(2) Not allow missing or wrong putting of component.</td></tr>
</table>

No	Item	Criterion
12	Protruded W: Terminal Width	 Acceptable criteria: Y ≤ 0.4
13	TAB	1. Position  W1≤1/3W H1≤1/3H 2 TAB bonding strength test  P (=F/TAB bonding width) ≥650gf/cm ,(speed rate: 1mm/min) 5pcs per SOA (shipment)
14	Total no. of acceptable Defect	A. Zone Maximum 2 minor non-conformities per one unit. Defect distance: each point to be separated over 10mm B. Zone It is acceptable when it is no trouble for quality and assembly in customer's end product.

11.3 Reliability of LCM

Reliability test condition:

Item	Condition	Time (hrs)	Assessment
High temp. Storage	80°C	48	No abnormalities in functions and appearance
High temp. Operating	70°C	48	
Low temp. Storage	-30°C	48	
Low temp. Operating	-20°C	48	
Humidity	40°C/ 90%RH	48	
Temp. Cycle	0°C ← 25°C →50°C (30 min ← 5 min → 30min)	10cycles	

Recovery time should be 24 hours minimum. Moreover, functions, performance and appearance shall be free from remarkable deterioration within 50,000 hours under ordinary operating and storage conditions room temperature (20±8°C), normal humidity (below 65% RH), and in the area not exposed to direct sun light.

11.4 Precaution for using LCD/LCM

LCD/LCM is assembled and adjusted with a high degree of precision. Do not attempt to make any alteration or modification. The followings should be noted.

General Precautions:

1. LCD panel is made of glass. Avoid excessive mechanical shock or applying strong pressure onto the surface of display area.
2. The polarizer used on the display surface is easily scratched and damaged. Extreme care should be taken when handling. To clean dust or dirt off the display surface, wipe gently with cotton, or other soft material soaked with isoproply alcohol, ethyl alcohol or trichlorotriflorothane, do not use water, ketone or aromatics and never scrub hard.
3. Do not tamper in any way with the tabs on the metal frame.
4. Do not make any modification on the PCB without consulting Focus LCDs
5. When mounting a LCM, make sure that the PCB is not under any stress such as bending or twisting. Elastomer contacts are very delicate and missing pixels could result from slight dislocation of any of the elements.
6. Avoid pressing on the metal bezel, otherwise the elastomer connector could be deformed and lose contact, resulting in missing pixels and also cause rainbow on the display.
7. Be careful not to touch or swallow liquid crystal that might leak from a damaged cell. Any liquid crystal adheres to skin or clothes, wash it off immediately with soap and water.

Static Electricity Precautions:

1. CMOS-LSI is used for the module circuit; therefore operators should be grounded whenever he/she comes into contact with the module.
2. Do not touch any of the conductive parts such as the LSI pads; the copper leads on the PCB and

the interface terminals with any parts of the human body.

3. Do not touch the connection terminals of the display with bare hand; it will cause disconnection or defective insulation of terminals.
4. The modules should be kept in anti-static bags or other containers resistant to static for storage.
5. Only properly grounded soldering irons should be used.
6. If an electric screwdriver is used, it should be grounded and shielded to prevent sparks.
7. The normal static prevention measures should be observed for work clothes and working benches.
8. Since dry air is inductive to static, a relative humidity of 50-60% is recommended.

Soldering Precautions:

1. Soldering should be performed only on the I/O terminals.
2. Use soldering irons with proper grounding and no leakage.
3. Soldering temperature: 280°C±10°C
4. Soldering time: 3 to 4 second.
5. Use eutectic solder with resin flux filling.
6. If flux is used, the LCD surface should be protected to avoid spattering flux.
7. Flux residue should be removed.

Operation Precautions:

1. The viewing angle can be adjusted by varying the LCD driving voltage Vo.
2. Since applied DC voltage causes electro-chemical reactions, which deteriorate the display, the applied pulse waveform should be a symmetric waveform such that no DC component remains. Be sure to use the specified operating voltage.
3. Driving voltage should be kept within specified range; excess voltage will shorten display life.
4. Response time increases with decrease in temperature.
5. Display color may be affected at temperatures above its operational range.
6. Keep the temperature within the specified range usage and storage. Excessive temperature and humidity could cause polarization degradation, polarizer peel-off or generate bubbles.
7. For long-term storage over 40°C is required, the relative humidity should be kept below 60%,and avoid direct sunlight.