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APPLICATION NOTE 3903

Using Internal Calibration and Right Shifting (Scalable Dynamic Ranging) on the DS1863/DS1865 to Enhance ADC Performance

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Abstract: This application note discusses how an application can benefit from using internal calibration and right shifting (Scalable Dynamic Ranging) with the DS1863/DS1865 controller/monitor chip. The article explains how to implement internal calibration and right shifting, and provides an example to illustrate the process.

Introduction

The DS1863 and the DS1865 controller/monitor devices use internal calibration and right shifting (Scalable Dynamic Ranging) to greatly enhance the internal 13-bit ADC, giving it higher precision and accuracy without added cost and size. Furthermore, the DS1863/DS1865's internal calibration features both *programmable scale* and *programmable offset*, which eliminate most, if not all, external signal-conditioning circuitry. With programmable scaling in the analog domain before the ADC, the input signal is scaled to use the entire range of the ADC. Then while in the digital domain, right shifting can be used to divide the digital output back down so that the desired (or mandated by SFF-8472) LSB remains unaffected and even transparent to the user.

Analog Monitor Inputs

The block diagram of the DS1863/DS1865 MON inputs is shown in **Figure 1**. For clarity, only one input is illustrated, although the concepts apply to all four MON inputs (MON1, MON2, MON3, and MON4). The MON inputs are used to monitor signals like Tx Power and Rx Power.
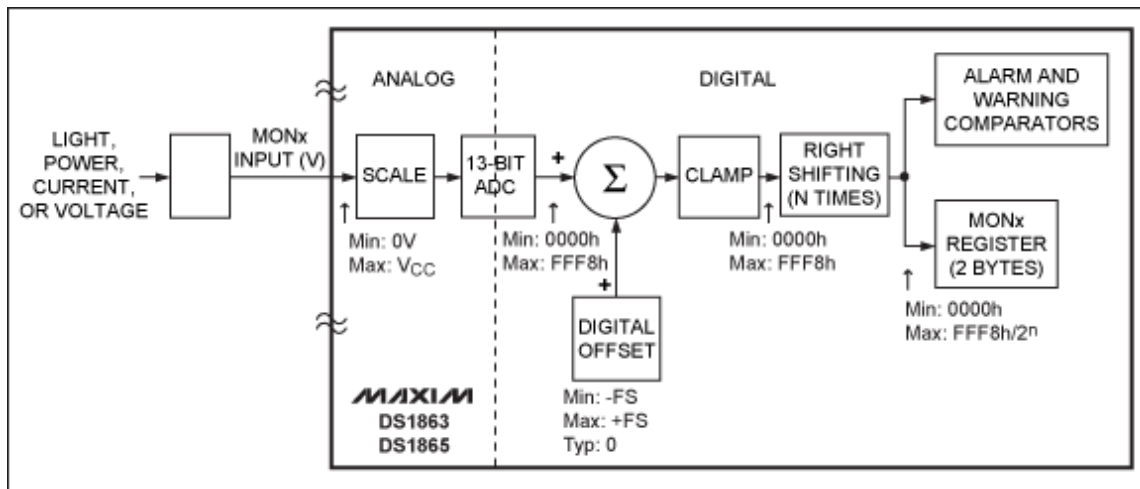
Figure 1. Block diagram of the MON input(s) on the DS1863/DS1865.

As Figure 1 shows, a single-ended voltage is applied to a DS1863/DS1865 MON pin. While in the analog domain, the voltage is fed into a programmable scale block. The scale block makes it possible to calibrate the MON channel to achieve a desired LSB or *full-scale voltage*. The full-scale voltage is the desired LSB × 2^n, where n is the number of bits. Furthermore, the scale block makes it possible to internally gain small input signals to maximize use of the ADC. This procedure will be described in more detail later.

Following the scale block is the 13-bit ADC. The 13-bit conversions are output left-justified in 2-byte (16-bit) values. The ADC can output digital values of 0000h to FFF8h.

Following the ADC, the digitized signal is further adjusted by a user-programmable digital offset. This digital offset can be used to internally add positive or negative offsets by simply performing digital addition. It is important to note that positive offsets will clamp at the digital value of FFF8h; negative offsets will have a full-scale digital value of less than FFF8h (since the negative offset subtracts from the conversions). The minimum digital value in this case will be clamped at 0000h. Detailed information regarding the digital offset is provided later in the **Offset Register** section.

Right shifting is the final operation before the digital values are output. Each MON input has three bits which control the number of desired right shifts. (The benefits of right shifting will be discussed later.) Setting the three bits to zero disables the right-shifting functionality. As with the offset, right shifting also affects the full-scale digital output. If set to two right shifts, for example, the full-scale digital output becomes 3FFEh. After the shifting is performed, the value is then written to the appropriate register where the user reads the conversion (Lower Memory, Registers 64h-6Bh). This is also the value used for alarm and warning comparisons.

A Note about Password Access

The settings for the scale and offset values for the four MON inputs are located in Table 02h of the DS1863/DS1865. To read or write to these values, level 2 password access (PW2) is required. This access is granted if the password for PW2 level entry is entered into the password entry bytes (PWE located in Lower Memory, Registers 7Bh-7Eh).

The Factory-Calibrated MON Inputs

Each of the DS1863/DS1865 MON inputs are factory-trimmed to a full-scale voltage of 2.5V. Also, each of the digital offsets is factory-programmed to zero so that a 0V input will output a digital value of 0000h.

The right shifting factory default is also 0. The transfer function for the factory-calibrated DS1863/DS1865 is illustrated in plot B of **Figure 2**, and will be described later.

A factory-trimmed device will output one of 8192 digital values for input voltages from 0 to 2.5V, yielding a resolution of 305µV (2.5V/8192) for the 13-bit conversion. Ideally, the input signal to be digitized is a 0 to 2.5V signal so that the entire range is utilized. However in a real-world application, this is not always the case. With Receive Power (Rx Power), for example, voltages of 0 to .5V are common, meaning that 80% of the digital output codes will never be used. The 13-bit ADC, capable of generating 8192 codes, will thus only be outputting one of 1638 codes. The remaining 6554 digital codes will never be used. Moreover, of the 1638 codes that are used, the resolution remains at 305µV.

To make better use of the 13-bit ADC, the DS1863/DS1865 MON value will have to be recalibrated to a full-scale voltage of 0.5V. However, recalibrating the MON value alone does not solve the input-signal problem, because the LSB will change and no longer match the desired LSB. Ultimately, to get maximum performance from the ADC, right shifting must be used with adjustments to the scale and offset values.

Internal Calibration and Right Shifting

Internal calibration and right shifting are beneficial when the signal to be monitored is small and, hence, not using the entire ADC range. By amplifying the signal in the analog domain before the analog-to-digital conversion, and then by dividing it back down by the same factor in the digital domain, the desired LSB is preserved. Both precision and accuracy are improved by a factor of two for every right shift (up to three). After three right shifts, precision or accuracy will not improve any further.

The benefit of using internal calibration and right shifting can best be illustrated in the example shown in Figure 2. Plot A is a voltage vs. time plot of an example signal that is to be monitored. The example signal swings between 0 to 0.5V. Plots B and C illustrate MON input voltage vs. digital output. These latter plots show the factory-calibrated transfer function, an example transfer function using two right shifts, and a full-scale voltage of 2.5V/4 = 0.625V, respectively. A full-scale voltage of 0.625V means that fewer codes will be wasted, thus resulting in conversions that are four times larger than the 2.5V full-scale voltage, but which are then divided back down by a factor of four (two right shifts). Determining the number of right shifts and, hence, the full-scale voltage will be discussed below. Two right shifts are used here simply to compare a right-shifting example against no right shifting. The device settings used, as well as calculations pertaining to each of the transfer functions, are shown below each of the corresponding transfer functions.
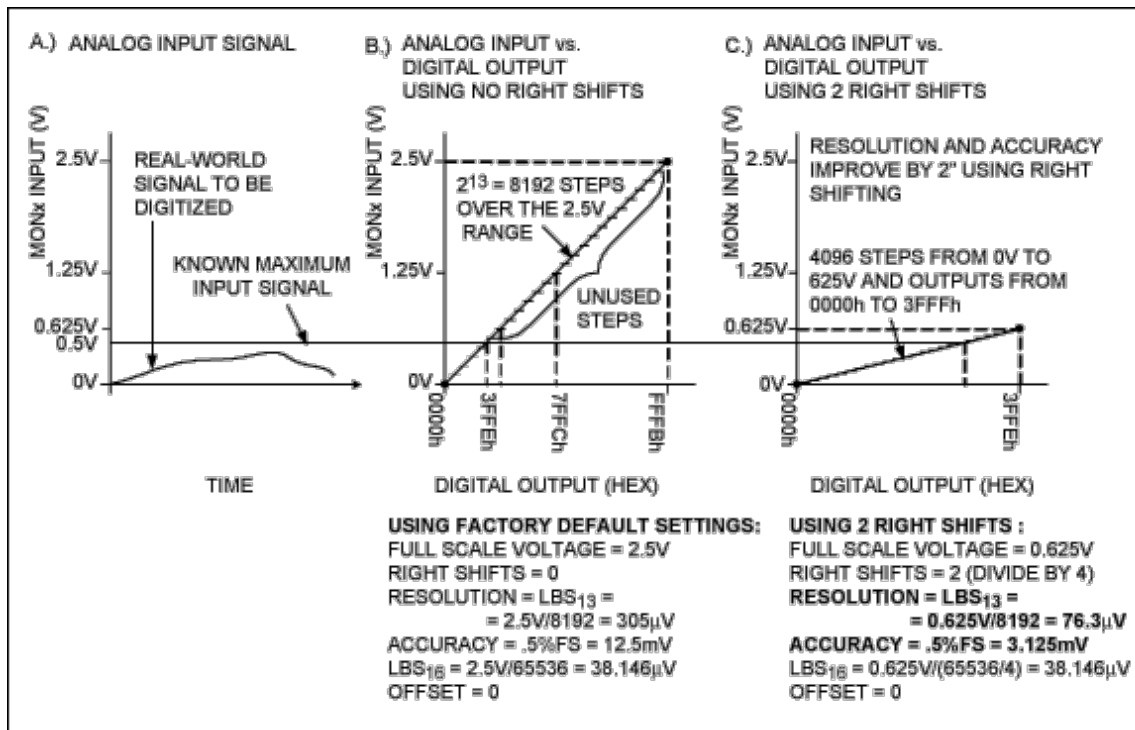
Figure 2. Data illustrate a comparison between no right shifting (B) vs. right shifting (C).

All three plots in Figure 2 are shown side-by-side on the same y-axis and scale. A horizontal line can be drawn through any particular point on the input signal (Plot A) and each of the transfer functions, so that a rough approximation of the digital output can be made. If one returns to the example input signal ranging from 0 to 0.5V, where 0.5V is indicated by the bold horizontal line across all three plots, the benefit of right shifting can be seen by comparing plots B and C. When the ADC's input range spans a voltage range much greater than the range of the input signal, numerous steps will be wasted (see plot B). Only 1638 of the 8192 are used; the remaining 80% in plot B are wasted. In contrast, plot C shows that by internally calibrating to a smaller full-scale voltage and using right shifting, the precision increased. Now 6554 of the 8192 digital codes are used to digitize the signal. Moreover, after right shifting, the desired LSB is maintained. The right shifting is transparent to the user. This can be verified by observing that both plots output approximately the same digital value.

Determining How Many Right Shifts Are Needed

The number of right shifts needed for an application is a function of the full-scale voltage (internal calibration) as well as the percentage of digital codes used for a given input signal. If the maximum voltage of the input signal is known (in addition to the full-scale voltage), then the expected digital outputs can be calculated. Otherwise, a "hands-on" approach will be required during the engineering evaluation to determine the range of digital outputs and, thus, the ideal number of right shifts. The hands-on approach is detailed below.

1. Set the right shift bits to 0.
2. Internally calibrate the part to yield the desired LSB, which will determine the initial full-scale voltage. (This process will be discussed later in this application note.)
3. Apply the maximum input signal and read the corresponding digital outputs to determine the used range.
4. Determine what percentage of the ADC range is used. If the digital readings exceed 7FFFh, then

right shifting should not be used (zero right shifts). However, if the digital readings are less than 7FFFh, then at least one right shift can be used. If the digital readings are less than 3FFFh, then two right shifts can be used, and so forth. **Table 1** summarizes this.

Table 1. Number of Right Shifts to Be Used for Various Output Ranges

Output Range Used with Zero Right-Shifts	Number of Right-Shifts Needed
0h .. FFFFh	0
0h .. 7FFFh	1
0h .. 3FFFh	2
0h .. 1FFFh	3

5. To compensate for the division of the digital values which result from right shifting, gain must be added in the analog domain so that the desired LSB is maintained. Adding this gain is done by calculating a new full-scale voltage using the formula:

New full-scale voltage = Initial full-scale voltage/$2^{\text{\# of right shifts}}$

So, if the internal calibration from step 2 resulted in a full-scale voltage of 2.0V, and if the digital readings were greater than 1FFFh but never exceeded 3FFFh, then two right shifts would be ideal. The new full-scale voltage for this example is therefore $2.0V/2^2 = 0.5V$.

6. Internally calibrate the channel (with the right shift bits still set to 0) to the new full-scale voltage.
7. Set the right shift bits to their new value.

Once the evaluation determines the ideal number of right shifts and the full-scale voltage for a particular application, only steps 1, 6, and 7 are needed for production calibration.

Internal Calibration and Right Shifting Registers

The DS1863/DS1865 device registers responsible for each analog channel's internal calibration and right-shifting settings are summarized in **Table 2**. Register addresses are shown for each of the MON channel settings as well as V_{CC}. V_{CC} has been included in the table for completeness, although it will not be discussed in this application note. The locations of the digital conversions have also been included in the table to show their relative location. Notice that the Scale, Offset, and Right Shifting registers reside in Memory Table 02h (not to be confused with Table 2 of this application note). Memory Table 02h is selected by writing 02h into the Table Select byte in Lower Memory, register 7Fh.

Table 2. DS1863/DS1865 Internal Calibration and Right Shifting Registers

	V_{CC}	MON1	MON2	MON3	MON4
Scale*	92-93h	94-95h	96-97h	98-99h	9A-9Bh
Offset*	A2-A3h	A4-A5h	A6-A7h	A8-A9h	AA-ABh
Right Shifts*	N/A	8Eh (b6-b4)	8Eh (b2-b0)	8Fh (b6-b4)	8Fh (b2-b0)
Readings	62-63h	64-65h	66-67h	68-69h	6A-6Bh
	*Table 02h				

Scale Register

The Scale register is a two-byte value that determines the amount of gain/attenuation of a particular monitored channel by adjusting the input switched-capacitor network. The Scale register thus lets the user

calibrate the full-scale voltage to any desired value between ~250mV and 6.5536V. This register must be calibrated because of process variations and varying requirements for the end application. The procedure for this calibration and for determining the value to be written in the Scale register is provided later in the **How to Internal Calibrate** section.

Note: When calibrating the DS1863/DS1865, it is important to know the value of both the offset and the right-shifting registers. Otherwise, if those values are non-zero and not compensated, the device will not be calibrated as intended.

Offset Register

The Offset register is a two-byte value that determines the amount of digital offset applied to each of the monitored inputs. The DS1863/DS1865's offset is a simple digital addition or subtraction of the converted values. So once the scale is trimmed to the desired value (and before right shifting is enabled), the offset can be programmed to null out any offset or to move the range.

Offset is calculated by first determining how many counts should be added to, or subtracted from the conversions. One way that this is typically done is by applying the null input (such as laser off) and then reading the conversion. This process would produce the value that you would have subtracted from all the conversions.

The value that needs to be written into the Offset register is calculated by inserting the desired count into Equation 1:

$$\text{Offset Register} = -(\text{Count}/4) \qquad \text{Eq. 1}$$

Example 1: If the input voltage is referred to a reference other than ground, then this reference can be subtracted from the measurements. Assume that when we apply the reference to the MON input, a count of 200 (C8h) is read. You can use the Offset register to subtract 200 (C8h) from the analog-to-digital conversions to null it out. Using the equation to determine what to write to the register:

$$\text{Offset Register} = -(-\text{C8h}/4) = 0032\text{h} \qquad \text{Eq. 2}$$

Remember that in this case a subtraction is being performed, so the full-scale count (FFF8h) will also decrease by C8h, giving a new full-scale count of FF30h.

Example 2: Suppose that you wanted to add 200 counts to the readings. This results in the following equation:

$$\text{Offset Register} = -(\text{C8h}/4) = \text{FFCEh} \qquad \text{Eq. 3}$$

To calculate the new full-scale count you would (attempt) to add C8h to FFF8h. However, FFF8h is the maximum possible reading, so the full-scale count would remain FFF8h. The lower count would not be 00h, but would be C8h instead, as this offset is added to all readings.

Example 3: Calculate the offset value for zero offset:

$$\text{Offset Register} = (0/4) = 0000\text{h} \qquad \text{Eq. 4}$$

This is also the factory default for the Offset register.

Right Shifting Registers

The Right Shifting registers are found in Table 02h, registers 8Eh-8Fh. Since MON1 through MON4 can perform up to seven right shifts, three bits are required for each MON input. The settings for MON1 and MON2 reside in Table 02h, register 8Eh, while the settings for MON3 and MON4 reside in Table 02h, register 8Fh. Refer to the memory map in the data sheet (or Table 1 above) for the location of the bits. The factory default of these EEPROM registers are 00h, disabling right shifting.

To illustrate the result of right shifting further, **Figure 3** shows several examples of the resultant MON values.
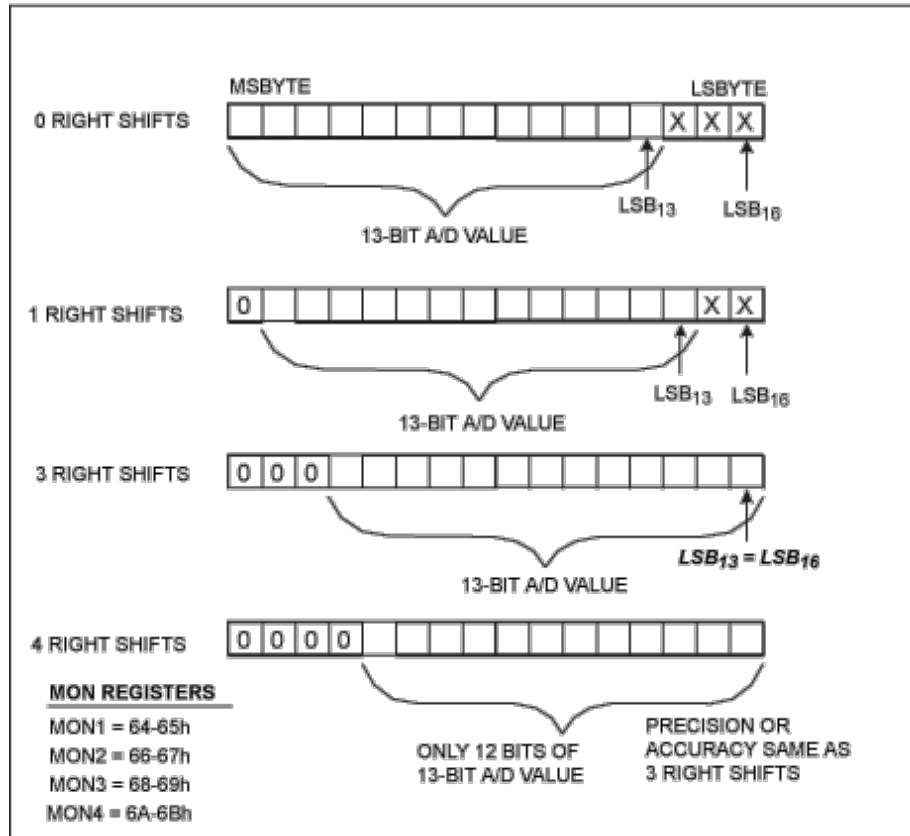

Figure 3. Examples of MON register right shifting.

How to Internal Calibrate

This application note discusses the binary search approach. The outputs of the algorithm are the Scale and Offset register values which yield the desired transfer function, i.e., the desired LSB.

To use the algorithm, one must be able to do two things: set the laser to two different intensities, for example minimum and close to the maximum (around 90%); and be able to go through multiple iterations. For nonoptical applications, two different voltages must be applied on command to the MON inputs. The algorithm provided in this application note uses 90% of maximum, so that a ">" comparison is possible. However, when applying a percentage of the desired full scale, it is important to calculate the corresponding percentage of the digital values as well.

Pseudo Code Example

An explanation of the binary search used to find the scale is best served with the following example of

pseudo code.

```
/* Assume that the null input is 0.5V */
/* Assume that the desired LSB of the lowest weighted bit is 50µV */

        Max Reading = 65535 x 50e-6              /* 3.27675 */
        CNT1 = 0.5 / 50e-6                       /* 10000 */
        CNT2 = 0.90 x FS / 50e-6                 /* 58981.5 */

/* The null input is 0.5V and the 90% of FS input is 0.9*3.27675 = 2.949075V
*/
        Set the trim-offset-register to zero
        Set Right Shift register to zero (typically zero. See Right Shifting
section above..)
        Scale_result = 0h
        Clamp = FFF8h/2^{Right\_Shift\_Register}


        For n = 15 down to 0,
        Begin
                scale_result = scale_result + 2^n
                Force the 90% FS input (2.949075V)

                Meas2 = read the digital result from the part
                If Meas2 >= Clamp then
                        scale_result = scale_result – 2^n
                Else
                        Begin
                                Force the null input (0.5V)
                                Meas1 = read the digital result from the part
                                If (Meas2 – Meas1) > (CNT2 – CNT1) then
                                        scale_result = scale_result – 2^n
                        End
End
Set the Scale register to scale_result
```

The Scale register is now set and the conversion resolution will best match the expected LSB. The next step is to calibrate the offset of the DS1863/DS1865. With the correct scale value written to the Scale register, again force the null input to the pin. Read the digital result from the part (Meas1). The offset can be calculated by using CNT1 as an input in Equation 1.

Explanation of the Pseudo Code

The algorithm begins by setting the Offset and Right Shifting registers to a known state, namely zero offset and zero right shifts. Although this example sets both registers to zero, other values can be used as long as you compensate for them. For example, when starting out with a programmed offset, FFF8h may no longer be the clamped, full-scale digital value. (See the **Offset Register** section.) Besides initializing registers, the algorithm begins by also calculating a few important constants which are a function of the desired LSB.

The binary search for the scale value begins by setting the Scale register to half scale, 8000h. The scale value is then tested by applying the 90% maximum input to the MON channel being calibrated, and then reading the corresponding digital conversion. This conversion value is then called Meas2. Meas2 is checked to see if it is clamped, FFF8h (since offset and right shifts are zero). If the reading is clamped, one cannot conclude whether the conversion is actually FFF8h or much greater (which is also FFF8h). Either way, the scale setting is too high. In binary search fashion, the scale value is cut in half and the process repeats until a nonclamping scale value is found.

As soon as a nonclamping Meas2 is found, the algorithm continues by forcing the null input and reading its digital conversion. This conversion becomes Meas1. Finally, the delta between Meas2 and Meas1 is calculated and compared to the desired delta (CNT2 - CNT1) by using the constants calculated at the

beginning of the algorithm. If Meas2 - Meas1 is greater than CNT2 - CNT1, then the scale is again cut in half. Otherwise, if Meas2 - Meas1 is less than CNT2 - CNT1, then the scale is increased by cutting the scale in half and this time adding it to the current scale. The process repeats until a total of 16 iterations are performed. The resultant is a 16-bit value that yields the desired scale (and desired LSB).

There is an alternate way of visualizing the scale calibration procedure. Beginning with the MSB (b15) of the 16-bit Scale register, set the bit to a 1 (all other bits are initially set to 0). With the MSB = 1, the process of applying the analog input and reading the digital output is performed. If the reading is clamped, then the scale is too high and the MSB is written back to a 0. Otherwise, the MSB remains a 1. The MSB is now known. Now the process moves on to the next bit, b14. Set b14 to 1 (leave b15 set to what was already determined for it). Bits 13 down to b0 are still 0. Now go through the process to determine if the gain is still too high. If so, then b14 becomes a 0. Otherwise, it becomes a 1. The procedure then continues bit by bit until all 16 bits are determined. The result is again a 16-bit value, which yields the desired scale.

Once the desired scale is achieved, a new offset can be calibrated or the scale can be left at 0 (no offset). The calibration method depends on how the offset feature is to be used. The explanation accompanying the algorithm in the product data sheet assumes that the user wants to apply a negative offset to null out the digital readings so that the null analog input will produce all zeros output. This is done simply by applying the null analog input and reading the conversion. If the null input (laser off, for example) produces a digital output, 20h for example, the offset can be programmed so that 20h will be digitally subtracted from every conversion. In this example, 20h is substituted into the offset formula and the result is then programmed into the Offset Cal register for the desired MON channel.

Internal Calibration and Right Shifting Example

The following example is provided to best demonstrate the concepts presented in this application note.

In this example, MON3 is used to monitor Rx Power. When the minimum input of -40dBm is applied, a voltage of 10mV is presented to the MON3 pin. The desired digital output for this input is 0000h. When a 0dBm input is applied, 300mV is presented to MON3. The desired digital output in this case is 2710h, and was chosen to satisfy the LSB dictated by SFF-8472 (the LSB for Rx Power is 0.1µW).

Determining the ideal number of right shifts for this example is relatively simple since the range of the desired digital output has been given (0000h-2710h). Using Table 1 above, the ideal number of right shifts is two. For a 2710h to be the final output *after* two right shifts, we can conclude that an input of 300mV must result in a conversion of 9C40h *before* the right shifts. Therefore, internal calibration will be used to "gain up" the conversion to 9C40h for an input of 300mV. Once the internal calibration and programming of the offset are complete, two right shifts will be enabled. Our example is summarized in **Table 3**.

Table 3. Internal Calibration and Right Shifting Example

Customer Signal Rx Power (dBm)	Voltage Applied to MON3 Pin (mV)	Digital Outputs During Cal. (0 Right Shifts) (hex)	Final Digital Output (2 Right Shifts) (hex)
-40	10	0000	0000
	50		0563
	100		0C1F
	150		12DB
	200		1997
	250		2051

0	300	9C40	2710

Once the relationship between input and output is determined (shown in Table 3), the internal calibration routine provided in the data sheet is used to internally calibrate the device. The routine begins by performing some preliminary calculations which are shown below. Notice that the 90% shown in the data sheet routine is not used here, because the second calibration point (300mV = 9C40h) is already less than 90% of the full-scale value.

Given Table 3, the following calculations are made:

$LSB = (0.300V - 0.010V)/(9C40h - 0000h) = 0.290V/40,000 = 7.25\mu V$

$Max\ Reading = LSB\ x\ 65535 = 7.25\mu V\ x\ 65535 = 0.475128V$

$CNT1 = 0.010/LSB = 1379.3 => 1379\ (dec)$

$CNT2 = 0.300/LSB = 41379.31 => 41379\ (dec)$

CNT1 and CNT2 are the expected (desired) digital outputs when the two calibration points are applied. The internal calibration routine will iterate, searching for a slope as close as possible to the slope determined by these two values.

The iterative portion of the routine goes through 16 cycles of programming a slope in a binary search fashion and then checking if it is equivalent to the desired slope. For the purpose of this example, a DS1863/DS1865 was calibrated using the internal calibration procedure; the inputs and outputs of all 16 iterations are shown in **Table 4**.

The first column of Table 4, Iteration, is equivalent to n in the routine. The column scale_result is the value programmed into the Scale register (device Table 02h, registers 98-99h) for every iteration. Columns Meas2 and Meas1 are the digital values read from the device with 300mV and 10mV applied to the input, respectively. Finally, for iterations in which Meas2 did not clamp, Meas2 - Meas1 is compared to CNT2 - CNT1. If Meas2 - Meas1 is greater than CNT2 - CNT1, then the scale_result is too large. The Scale bit corresponding to that iteration becomes a zero, which in turn determines the scale_result of the successive iteration. Once all 16 iterations are complete, the Scale value is known. The device used in this example resulted in a Scale value of **5038h**.

Table 4. Actual Internal Calibration Values

Iteration	Scale_result	Meas2	Meas1	Meas2	Meas1	Meas2-Meas1	CNT2-CNT1	Bit Result	Scale Register
(dec)	(hex)	(hex)		(dec)		(dec)	(dec)	(bin)	(hex)
15	8000	fd58	870	64856	2160	62696	40000	0	5
14	4000	82a0	450	33440	1104	32336	40000	1	
13	6000	c010	658	49168	1624	47544	40000	0	
12	5000	a138	558	41272	1368	39904	40000	1	
11	5800	b0b8	500	45240	1280	43960	40000	0	0
10	5400	a938	5a0	43320	1440	41880	40000	0	
9	5200	a530	578	42288	1400	40888	40000	0	
8	5100	a328	568	41768	1384	40384	40000	0	
7	5080	a238	568	41528	1384	40144	40000	0	3
6	5040	a1a8	560	41384	1376	40008	40000	0	
5	5020	a170	558	41328	1368	39960	40000	1	
4	5030	a190	558	41360	1368	39992	40000	1	
3	5038	a198	558	41368	1368	40000	40000	1	8
2	503C	a1a0	558	41376	1368	40008	40000	0	
1	503a	a1a0	558	41376	1368	40008	40000	0	
0	5039	a1a0	558	41376	1368	40008	40000	0	

From Table 3, we see that the minimum delta is reached in Iteration 3 (where both Meas2 - Meas1 and CNT2 - CNT1 are at 40000). The user can add a variable in the algorithm that checks at which iteration the minimum delta is reached, and then use the scale_result value at that iteration as the value for the Scale register, instead of the final value.

With the device programmed to its new Scale value, the Offset is determined by forcing 10mV (the voltage which we want to read 0000h) and reading the digital result. The device used in this example output a value of 0558h with 10mV applied. Using the offset formula (equation 1), the Offset is calculated as:

MON3 Offset = -(-0558h/4) = **0156h**

Finally, the new clamp value can be calculated as:

New clamp value (pre-right shift) = FFF8h - 0558h = FAA0h

With the internal calibration complete, the two right shifts are enabled by writing 20h to Table 02h, register 8Fh.

Conclusion

The internal calibration and right shifting features of the DS1863/DS1865 provide the utmost flexibility and make the devices suitable for a wide variety of applications. This application note provides information not found in the DS1863/DS1865 data sheet, specifically why internal calibration and right shifting are beneficial and how to implement them. A hands-on example was also provided to tie the concepts together and to show actual data read from a DS1863/DS1865 during the internal calibration procedure.

Questions/comments/suggestions concerning this application note can be sent to:
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