2N4117/A, 2N4118/A, 2N4119/A N-Channel JFET

Features

- InterFET N0001H Geometry
- Low gate leakage: 120fA typical @20V
- Low C_{ISS}: 1.8pF typical
- Typical BV_{GSS}: -60V
- High radiation tolerance
- RoHS, REACH, CMR compliant
- Custom test and binning options available
- SMT, TH, and bare die package options
- Edge case SPICE modeling: InterFET SPICE

Industry Standard Crosses

- SST4117, SST4118, SST4119, MMBF4117, MMBF4118, MMBF4119, 2N4117, 2N4118, 2N4119, VCR7N

InterFET Similar Parts

- SMP4117-8-9, PN4117-8-9, SMPVCR7N, PNVCR7N

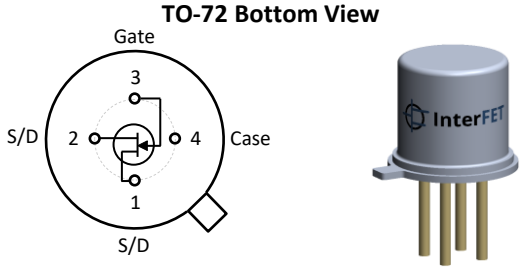
InterFET Dual Parts

- IFNU421-2-3-4-5-6

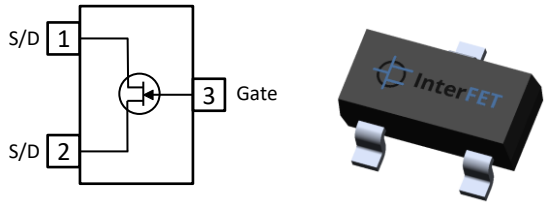
Applications

- General: Buffers; Signal mixers; Femtoampere diodes
- Military/Aero: Radar; Communications; Satellites
- Medical: Imaging systems; Monitors; Ultrasound

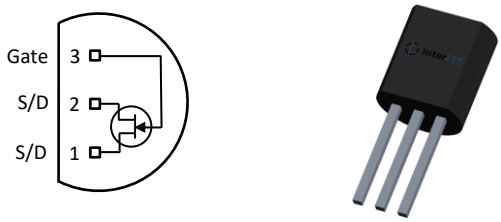
TO-72 Bottom View



SOT23 Top View



TO-92 Bottom View



NOTE: S/D pins are interchangeable Source Drain connections

Description

The -50V InterFET 2N4117/A, 2N4118/A, and 2N4119/A JFET's are targeted for ultra high input impedance applications. Gate leakages are typically 120fA at room temperatures. Proprietary InterFET processes yield exceptionally high radiation tolerance. Parts can be connected for femtoampere diode applications.

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
2N4117; 2N4118; 2N4119 2N4117A; 2N4118A; 2N4119A	Through-Hole	TO-72	Bulk
PN4117; PN4118; PN4119 PN4117A; PN4118A; PN4119A	Through-Hole	TO-92	Bulk
SMP4117; SMP4118; SMP4119 SMP4117A; SMP4118A; SMP4119A	Surface Mount	SOT23	Bulk
SMP4117TR; SMP4118TR; SMP4119TR SMP4117ATR; SMP4118ATR; SMP4119ATR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
2N4117COT; 2N4118COT; 2N4119COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
2N4117CFT; 2N4118CFT; 2N4119CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack

NOTICE: Please refer to the end of this document for information on product materials, compliance, safety, and legal statements.

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		TO-72	SOT-23	TO-92	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-20	-20	-20	V
I_{FG}	Continuous Forward Gate Current	50	50	50	mA
P_D	Continuous Device Power Dissipation[1]	500	350	500	mW
P	Power Derating[1]	3.3	2.8	4	mW/°C
T_J	Operating Junction Temperature	-65 to 175	-55 to 150	-55 to 150	°C
T_{STG}	Storage Temperature	-65 to 175	-55 to 150	-55 to 150	°C

[1] Thermal power dissipation and derating values obtained with gate pin (substrate) thermally connected to pad and/or internal layer.

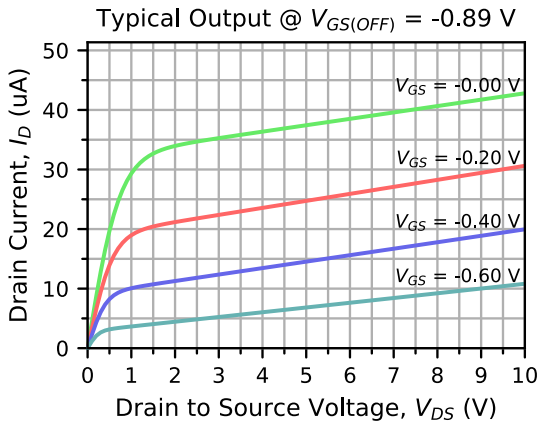
Static Characteristics (@ TA = 25°C, Unless otherwise specified, Highlighted values = A variant)

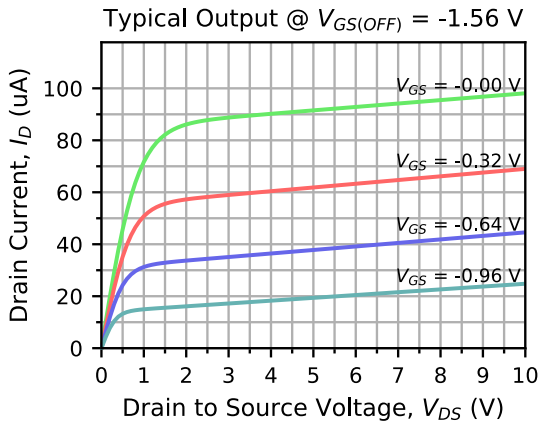
Parameters		Conditions	2N4117/A		2N4118/A		2N4119/A		Unit
			Min	Max	Min	Max	Min	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	I_G = -1µA, V_{DS} = 0V	-40		-40		-40		V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = -20V, V_{DS} = 0V		-10		-10		-10	pA
				-1		-1		-1	pA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = 10V, I_D = 1nA	-0.6	-1.8	-1	-3	-2	-6	V
I_{DSS}	Drain to Source Saturation Current	V_{DS} = 10V, V_{GS} = 0V (Pulsed)	0.03	0.09	0.08	0.24	0.2	0.6	mA
			0.015	0.09	0.08	0.24	0.2	0.6	mA

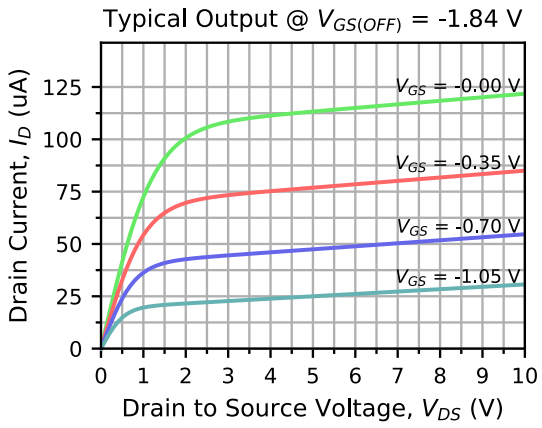
Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

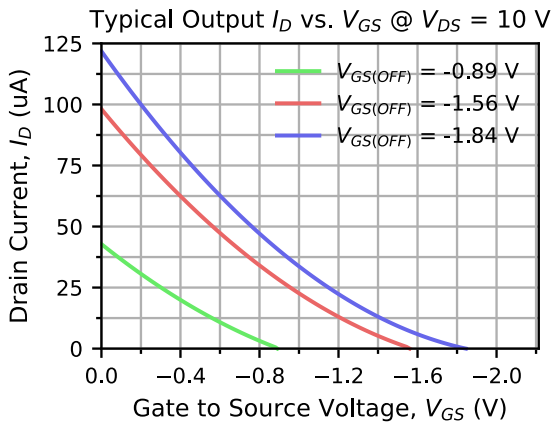
Parameters		Conditions	2N4117/A		2N4118/A		2N4119/A		Unit
			Min	Max	Min	Max	Min	Max	
G_{FS}	Forward Transconductance	V_{DS} = 10V, V_{GS} = 0V, f = 1kHz	70	210	80	250	100	330	µS
G_{OS}	Output Conductance	V_{DS} = 10V, V_{GS} = 0V, f = 1kHz		3		5		10	µS
C_{iss}	Input Capacitance	V_{DS} = 10V, V_{GS} = 0V, f = 1MHz		3		3		3	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 10V, V_{GS} = 0V, f = 1MHz		1.5		1.5		1.5	pF

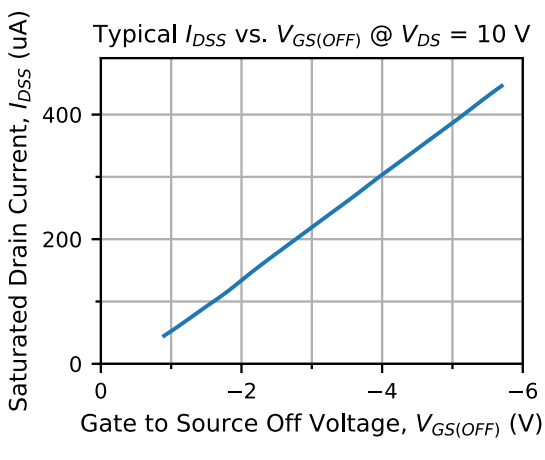
Typical 2N4117, 2N4118, 2N4119 Characteristics

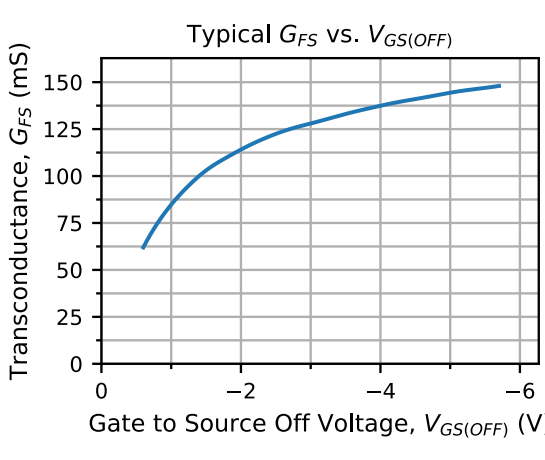




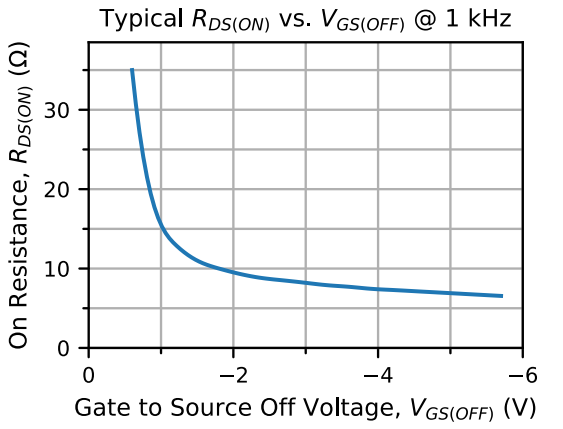


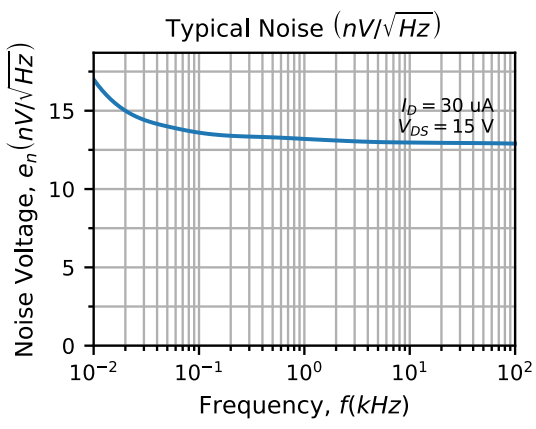


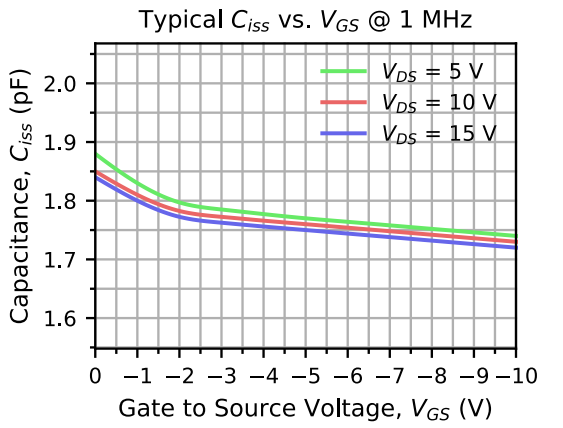


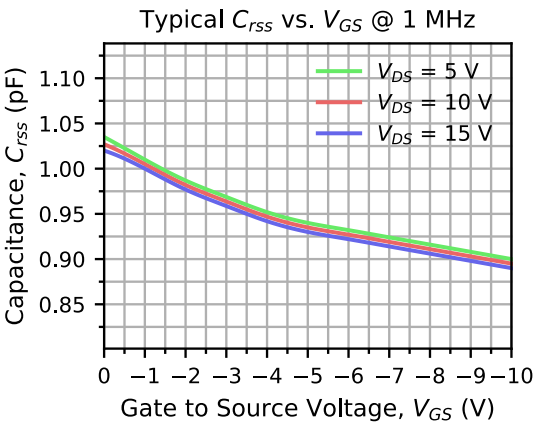


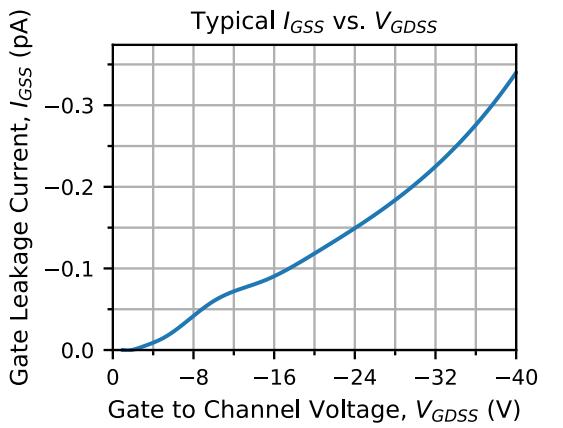
Typical 2N4117, 2N4118, 2N4119 Characteristics (Continued)





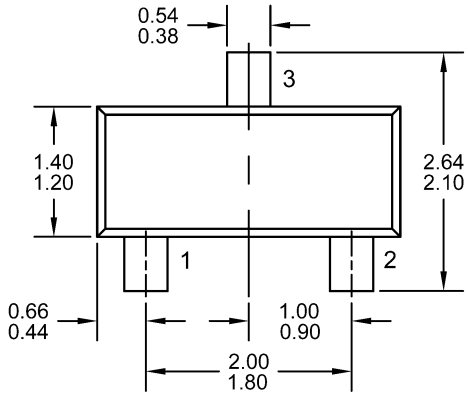


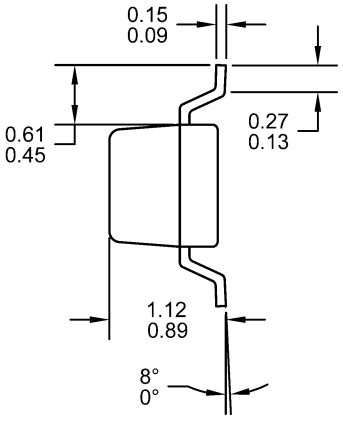


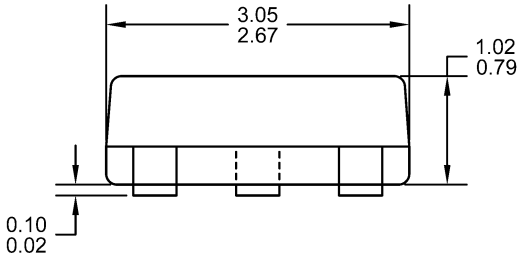


SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data

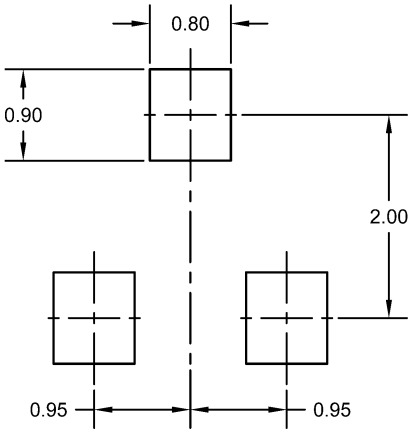






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

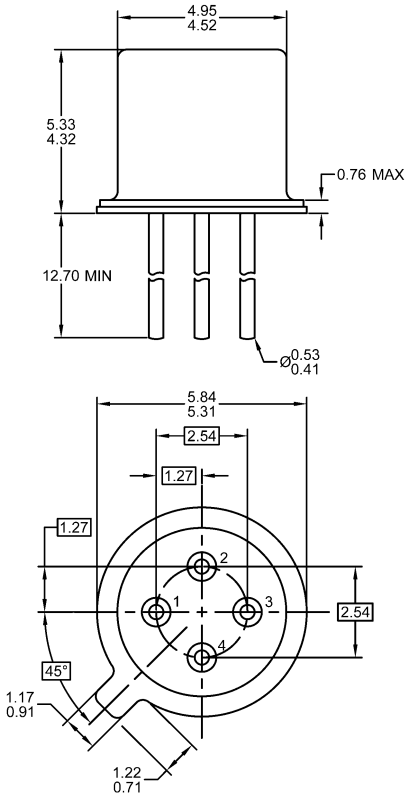
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

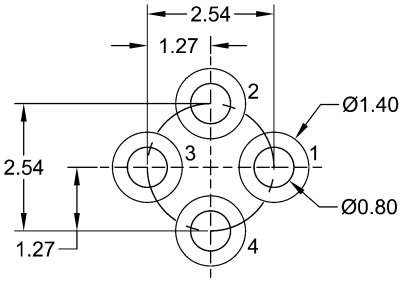
TO-72 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Four leaded device. Not all leads are shown in drawing views.
3. Package weight approximately 0.31 grams
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

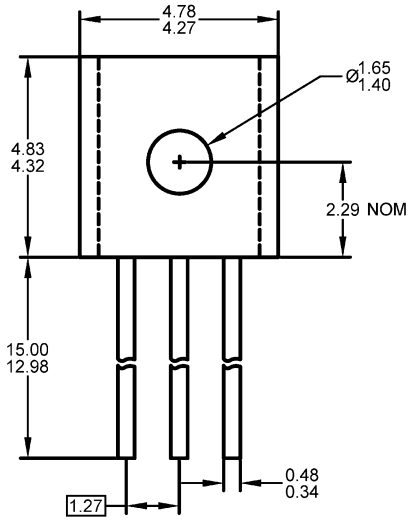
Suggested Through-Hole Layout

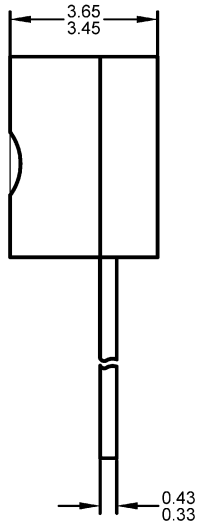


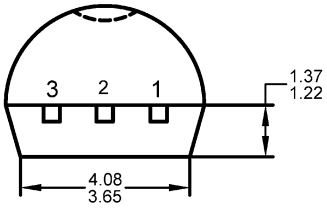
1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.

TO-92 Mechanical and Layout Data

Package Outline Data

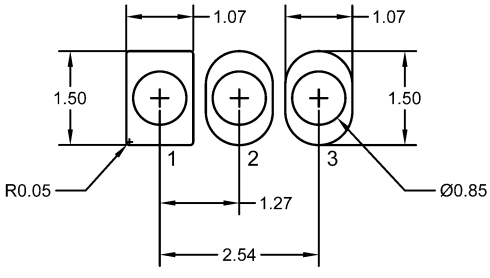






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.19 grams
3. Molded plastic case UL 94V-0 rated
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.

Compliance and Legal

Environment

InterFET parts follow the latest RoHS Compliance, REACH Compliance, Proposition 65 Statement, TSCA Statement, and Chemical Disposal and Waste Mitigation requirement and guidelines. For more on InterFET's Environmental Commitment please visit www.InterFET.com/environmental/.

Package materials

Parameters	SOT23	SOIC8	TO-92	Metal Case
Alloy	CDA194	C194 1/2H	C194 1/2H	Kovar
Cu	Balance	97% min	97% min	
Fe	2.1 – 2.6%	2.1 – 2.6%	2.1 – 2.6%	53%
Zn	0.05 – 0.2%	0.05 – 0.2%	0.05 – 0.15%	
P	0.015 – 0.15%	0.015 – 0.15%	0.015 – 0.15%	
Pb	0.03% max	0.03% max	0.03% max	
Ni				29%
Co				17%
Mn				0.3%
Si				0.2%
C				<0.01%
Au				Plating

Package tests

Parameters	SOT23	SOIC8	TO-92	Metal Case
MSL	Level 1	Level 1	N/A	N/A
ESD	Class M4 Machine Model Class 3A HBM	Class M4 Machine Model Class 3A HBM	Class M4 Machine Model Class 3A HBM	Class M4 Machine Model Class 3A HBM

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