





J232 N-Channel JFET

Support

Features

- InterFET <u>N0016SH Geometry</u>
- Low Noise: 5 nV/vHz Typical
- Low Ciss: 4pF Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

Applications

- · Audio Amplifiers
- Small Signal Amplifier ٠
- Ultrahigh Impedance Pre-Amplifier ٠

Description

The -40V InterFET J232 JFET is targeted for sensitive amplifier stages for mid-frequencies designs. Gate leakages are typically less than 10pA at room temperatures.



TO-92 Bottom View





Product Summarv

	Parameters	J232 Min	Unit	
BV _{GSS}	Gate to Source Breakdown Voltage	-40	V	
I _{DSS}	Drain to Source Saturation Current	5	mA	
V _{GS(off)}	Gate to Source Cutoff Voltage	-3	V	
GFS	Forward Transconductance	2500	μS	

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
J232	Through-Hole	TO-92	Bulk
SMPJ232	Surface Mount	SOT23	Bulk
	7" Tape and Reel: Max 3,000 Pieces		Minimum 1,000 Pieces
SMPJ232TR	13" Tape and Reel: Max 9,000 Pieces	SOT23	Tape and Reel
J232COT	Chip Orientated Tray (COT Waffle Pack)	СОТ	400/Waffle Pack
J232CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack



Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.







Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

	Parameters	Value	Unit
VRGS	Reverse Gate Source and Gate Drain Voltage	-40	V
I_{FG}	Continuous Forward Gate Current	50	mA
PD	Continuous Device Power Dissipation	360	mW
Р	Power Derating	3.27	mW/°C
Τı	Operating Junction Temperature	-55 to 125	°C
T _{STG}	Storage Temperature	-65 to 200	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

			J232			
	Parameters	Conditions	Min	Тур	Max	Unit
V(BR)GSS	Gate to Source Breakdown Voltage	V _{DS} = 0V, I _G = -1µA	-40			V
I _{GSS}	Gate to Source Reverse Current	$V_{GS} = -30V, V_{DS} = 0V$			-250	pА
V _{GS(OFF)}	Gate to Source Cutoff Voltage	$V_{DS} = 20V, I_D = 1\mu A$	-3		-6	V
I _{DSS}	Drain to Source Saturation Current	V _{GS} = 0V, V _{DS} = 20V (Pulsed)	5		10	mA
IG	Gate Operating Current	V _{DS} = 20V, I _D = 0V		-2		pА

Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

			J232			
	Parameters	Conditions	Min	Тур	Max	Unit
GFS	Forward Transconductance	V _{DS} = 20V, V _{GS} = 0V, f = 1kHz	2500		5000	μS
Gos	Output Conductance	$V_{DS} = 20V, V_{GS} = 0V, f = 1kHz$		5		μS
Ciss	Input Capacitance	V _{DS} = 20V, V _{GS} = 0V, f = 1MHz		4		pF
C _{rss}	Reverse Transfer Capacitance	V _{DS} = 20V, V _{GS} = 0V, f = 1MHz		1		pF
en	Noise Voltage	$V_{DS} = 10V, V_{GS} = 0V, f = 10Hz$ $V_{DS} = 10V, V_{GS} = 0V, f = 1kHz$		20 6	30	nV/√Hz



Technical

Support

Order

Now

SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data





Suggested Pad Layout





- 1. All linear dimensions are in millimeters.
- 2. Package weight approximately 0.12 grams
- 3. Molded plastic case UL 94V-0 rated
- For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
- 5. Bulk product is shipped in standard ESD shipping material
- 6. Refer to JEDEC standards for additional information.

- 1. All linear dimensions are in millimeters.
- 2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.





TO-92 Mechanical and Layout Data

Package Outline Data





Suggested Through-Hole Layout





- 1. All linear dimensions are in millimeters.
- 2. Package weight approximately 0.19 grams
- 3. Molded plastic case UL 94V-0 rated
- 4. Bulk product is shipped in standard ESD shipping material
- 5. Refer to JEDEC standards for additional information.

- 1. All linear dimensions are in millimeters.
- The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.