2-GHz, LOW DISTORTION, DUAL CURRENT-FEEDBACK AMPLIFIERS

Check for Samples: THS3202

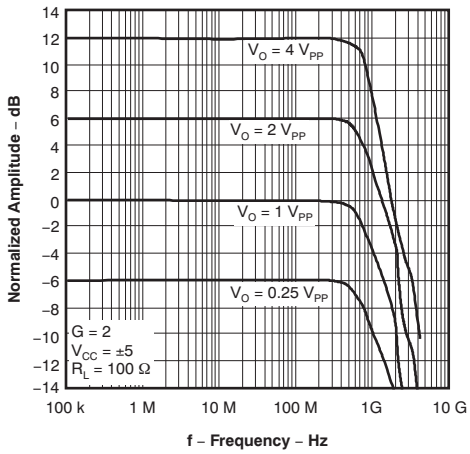
FEATURES

- **Unity-Gain Bandwidth: 2 GHz**
- **High Slew Rate: 9000 V/µs**
- **High Output Current: ±115 mA into 20 Ω R_L**
- **Power-Supply Voltage Range: 6.6 V to 15 V**

APPLICATIONS

- **High-Speed Signal Processing**
- **Test and Measurement Systems**
- **High-Voltage ADC Preamplifier**
- **RF and IF Amplifier Stages**
- **Professional Video**

LARGE-SIGNAL FREQUENCY RESPONSE



DESCRIPTION

The THS3202 is a dual current-feedback amplifier developed with BiCOM-II technology. Designed for low distortion with a high slew rate of 9000 V/µs, the THS320x family is ideally suited for applications driving loads sensitive to distortion at high frequencies.

The THS3202 provides well-regulated ac performance characteristics with power supplies ranging from single-supply 6.6-V operation up to a 15-V supply. The high unity-gain bandwidth of up to 2 GHz is a major contributor to the excellent distortion performance. The THS3202 offers an output current drive of ±115 mA and a low differential gain and phase error that make it suitable for applications such as video line drivers.

The THS3202 is available in an SOIC-8, an MSOP-8, and an MSOP-8 with PowerPAD™ packages.

RELATED DEVICES AND DESCRIPTIONS

THS3001	±15-V 420-MHz Low Distortion CFB Amplifier
THS3061/2	±15-V 300-MHz Low Distortion CFB Amplifier
THS3122	±15-V Dual CFB Amplifier With 350 mA Drive
THS4271	+15-V 1.4-GHz Low Distortion VFB Amplifier

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

NUMBER OF CHANNELS	ORDERABLE PACKAGE AND NUMBER				
	PLASTIC SOIC-8(2) (D)	PLASTIC MSOP-8(2) PowerPAD		PLASTIC MSOP-8(2)	
		(DGN)	MARKING	(DGK)	MARKING
2	THS3202D	THS3202DGN	BEP	THS3202DGK	BEV

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) This package is available taped and reeled. To order this packaging option, add an ***R*** suffix to the part number (that is, THS3202DR).

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		UNIT
Supply voltage, V_S		16.5 V
Input voltage, V_I		$\pm V_S$
Differential input voltage, V_{ID}		±3 V
Output current, I_O(2)		175 mA
Continuous power dissipation		See Package Dissipation Ratings Table
Maximum junction temperature, T_J(3)		+150°C
Maximum junction temperature, continuous operation, long-term reliability, T_J(4)		+125°C
Operating free-air temperature range, T_A		–40°C to +85°C
Storage temperature range, T_{STG}		–65°C to +150°C
ESD ratings:	HBM	3000 V
	CDM	1500 V
	MM	200 V

(1) The absolute maximum ratings under any condition is limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The THS3202 may incorporate a PowerPAD on the underside of the chip. This acts as a heat sink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical briefs SLMA002 and SLMA004 for more information about using the PowerPAD thermally-enhanced package.
(3) The absolute maximum temperature under any condition is limited by the constraints of the silicon process.
(4) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

PACKAGE DISSIPATION RATINGS

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (1) (°C/W)	POWER RATING (2)	
			$T_A \le +25°C$	$T_A = +85°C$
D (8 pin)	38.3	97.5	1.32 W	410 mW
DGN (8 pin)	4.7	58.4	1.71 W	685 mW
DGK (8 pin)	54.2	260	385 mW	154 mW

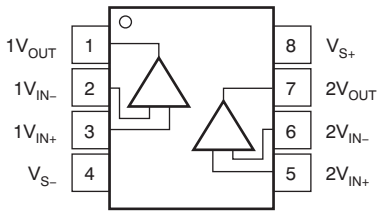
(1) These data were taken using the JEDEC standard High-K test PCB.
(2) Power rating is determined with a junction temperature of +125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below +125°C for best performance and long-term reliability.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	MAX	UNIT
Supply voltage, (V_{S+} and V_{S-})	Dual supply	±3.3	±7.5	V
	Single supply	6.6	15	
Operating free-air temperature range		–40	+85	°C

PIN ASSIGNMENTS

D, DGN, AND DGK PACKAGES
(TOP VIEW)



ELECTRICAL CHARACTERISTICS: V_S = ±5 V

V_S = ±5 V: R_F = 500 Ω, R_L = 100 Ω, and G = +2, unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS3202				UNIT	MIN/TYP/MAX
		TYP	OVER TEMPERATURE				
		+25°C	+25°C	0°C to +70°C	–40°C to +85°C		
AC PERFORMANCE							
Small-signal bandwidth, –3 dB (V_O = 100 mV_{PP})	G = +1, R_F = 500 Ω	1800				MHz	Typ
	G = +2, R_F = 402 Ω	975				MHz	Typ
	G = +5, R_F = 300 Ω	780				MHz	Typ
	G = +10, R_F = 200 Ω	550				MHz	Typ
Bandwidth for 0.1-dB flatness	G = +2, V_O = 100 mV_{PP}, R_F = 536 Ω	380				MHz	Typ
Large-signal bandwidth	G = +2, V_O = 4 V_{PP}, R_F = 536 Ω	875				MHz	Typ
Slew rate (25% to 75% level)	G = –1, 5-V step	5100				V/µs	Typ
	G = +2, 5-V step	4400				V/µs	Typ
Rise and fall time	G = +2, V_O = 5-V step	0.45				ns	Typ
Settling time to 0.1%	G = –2, V_O = 2-V step	19				ns	Typ
Settling time to 0.01%	G = –2, V_O = 2-V step	118				ns	Typ
Harmonic distortion	G = +2, f = 16 MHz, V_O = 2 V_{PP}						
2nd harmonic	R_L = 100 Ω	–64				dBc	Typ
	R_L = 500 Ω	–67				dBc	Typ
3rd harmonic	R_L = 100 Ω	–67				dBc	Typ
	R_L = 500 Ω	–69				dBc	Typ
3rd-order intermodulation distortion	G = +5, f_C = 120 MHz, Δf = 200 kHz, $V_{O(envelope)}$ = 2 V_{PP}	–64				dBc	Typ
Input voltage noise	f > 10 MHz	1.65				nV/√Hz	Typ
Input current noise (noninverting)	f > 10 MHz	13.4				pA/√Hz	Typ
Input current noise (inverting)	f > 10 MHz	20				pA/√Hz	Typ
Crosstalk	G = +2, f = 100 MHz	–60				dB	Typ
Differential gain (NTSC, PAL)	G = +2, R_L = 150 Ω	0.008				%	Typ
Differential phase (NTSC, PAL)	G = +2, R_L = 150 Ω	0.03				Degrees	Typ
DC PERFORMANCE							
Open-loop transimpedance gain	V_O = ±1 V, R_L = 1 kΩ	300	200	140	120	kΩ	Min
Input offset voltage	V_{CM} = 0 V	±0.7	±3	±3.8	±4	mV	Max
Average offset voltage drift	V_{CM} = 0 V			±10	±13	µV/°C	Typ
Input bias current (inverting)	V_{CM} = 0 V	±13	±60	±80	±85	µA	Max
Average bias current drift (–)	V_{CM} = 0 V			±300	±400	nA/°C	Typ
Input bias current (noninverting)	V_{CM} = 0 V	±14	±35	±45	±50	µA	Max
Average bias current drift (+)	V_{CM} = 0 V			±300	±400	nA/°C	Typ

ELECTRICAL CHARACTERISTICS: V_S = ±5 V (continued)

V_S = ±5 V: R_F = 500 Ω, R_L = 100 Ω, and G = +2, unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS3202				UNIT	MIN/TYP/MAX
		TYP	OVER TEMPERATURE				
		+25°C	+25°C	0°C to +70°C	–40°C to +85°C		
INPUT							
Common-mode input range		±2.6	±2.5	±2.5	±2.5	V	Min
Common-mode rejection ratio	V_{CM} = ±2.5 V	71	60	58	58	dB	Min
Input resistance	Noninverting	780				kΩ	Typ
	Inverting	11				Ω	Typ
Input capacitance	Noninverting	1				pF	Typ
OUTPUT							
Voltage output swing	R_L = 1 kΩ	±3.65	±3.5	±3.45	±3.4	V	Min
	R_L = 100 Ω	±3.45	±3.3	±3.25	±3.2	V	Min
Current output, sourcing	R_L = 20 Ω	115	105	100	100	mA	Min
Current output, sinking	R_L = 20 Ω	100	85	80	80	mA	Min
Closed-loop output impedance	G = +1, f = 1 MHz	0.01				Ω	Typ
POWER SUPPLY							
Minimum operating voltage	Absolute minimum		±3	±3	±3	V	Min
Maximum quiescent current	Per amplifier	14	16.8	19	20	mA	Max
Power-supply rejection (+PSRR)	V_{S+} = 4.5 V to 5.5 V	69	63	60	60	dB	Min
Power-supply rejection (–PSRR)	$V_{S–}$ = –4.5 V to –5.5 V	65	58	55	55	dB	Min

ELECTRICAL CHARACTERISTICS: V_S = 15 V

V_S = 15 V: R_F = 500 Ω, R_L = 100 Ω, and G = +2, unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS3202				UNITS	MIN/TYP/MAX
		TYP	OVER TEMPERATURE				
		+25°C	+25°C	0°C to +70°C	–40°C to +85°C		
AC PERFORMANCE							
Small-signal bandwidth, –3 dB (V_O = 100 mV_{PP})	G = +1, R_F = 550 Ω	2000				MHz	Typ
	G = +2, R_F = 550 Ω	1100				MHz	Typ
	G = +5, R_F = 300 Ω	850				MHz	Typ
	G = +10, R_F = 200 Ω	750				MHz	Typ
Bandwidth for 0.1-dB flatness	G = +2, V_O = 100 mV_{PP}, R_F = 536 Ω	500				MHz	Typ
Large-signal bandwidth	G = +2, V_O = 4 V_{PP}, R_F = 536 Ω	1000				MHz	Typ
Slew rate (25% to 75% level)	G = +5, 5-V step	7500				V/µs	Typ
	G = +2, 10-V step	9000				V/µs	Typ
Rise and fall time	G = +2, V_O = 10-V step	0.45				ns	Typ
Settling time to 0.1%	G = –2, V_O = 2-V step	23				ns	Typ
Settling time to 0.01%	G = –2, V_O = 2-V step	112				ns	Typ
Input voltage noise	f > 10 MHz	1.65				nV/√Hz	Typ
Input current noise (noninverting)	f > 10 MHz	13.4				pA/√Hz	Typ
Input current noise (inverting)	f > 10 MHz	20				pA/√Hz	Typ
Crosstalk	G = +2, f = 100 MHz	–60				dB	Typ
Differential gain (NTSC, PAL)	G = +2, R_L = 150 Ω	0.004				%	Typ
Differential phase (NTSC, PAL)	G = +2, R_L = 150 Ω	0.006				Degrees	Typ
DC PERFORMANCE							
Open-loop transimpedance gain	V_O = 6.5 V to 8.5 V, R_L = 1 kΩ	300	200	140	120	kΩ	Min
Input offset voltage	V_{CM} = 7.5 V	±1.3	±4	±4.8	±5	mV	Max
Average offset voltage drift	V_{CM} = 7.5 V			±10	±13	µV/°C	Typ
Input bias current (inverting)	V_{CM} = 7.5 V	±16	±60	±80	±85	µA	Max
Average bias current drift (–)	V_{CM} = 7.5 V			±300	±400	nA/°C	Typ
Input bias current (noninverting)	V_{CM} = 7.5 V	±14	±35	±45	±50	µA	Max
Average bias current drift (+)	V_{CM} = 7.5 V			±300	±400	nA/°C	Typ
INPUT							
Common-mode input range		2.4 to 12.6	2.5 to 12.5	2.5 to 12.5	2.5 to 12.5	V	Min
Common-mode rejection ratio	V_{CM} = 5 V to 10 V	69	60	58	58	dB	Min
Input resistance	Noninverting	780				kΩ	Typ
	Inverting	11				Ω	Typ
Input capacitance	Noninverting	1				pF	Typ
OUTPUT							
Voltage output swing	R_L = 1 kΩ	1.5 to 13.5	1.6 to 13.4	1.7 to 13.3	1.7 to 13.3	V	Min
	R_L = 100 Ω	1.7 to 13.3	1.8 to 13.2	2.0 to 13.0	2.0 to 13.0	V	Min
Current output, sourcing	R_L = 20 Ω	120	105	100	100	mA	Min
Current output, sinking	R_L = 20 Ω	115	95	90	90	mA	Min
Closed-loop output impedance	G = +1, f = 1 MHz	0.01				Ω	Typ
POWER SUPPLY							
Maximum quiescent current/channel	Per amplifier	15	18	21	21	mA	Max
Power-supply rejection (+PSRR)	V_{S+} = 14.50 V to 15.50 V	69	63	60	60	dB	Min
Power-supply rejection (–PSRR)	V_{S-} = –0.5 V to +0.5 V	65	58	55	55	dB	Min

TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS

SMALL-SIGNAL FREQUENCY RESPONSE

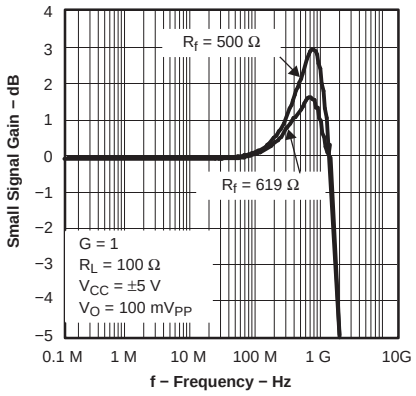


Figure 1.

SMALL-SIGNAL FREQUENCY RESPONSE

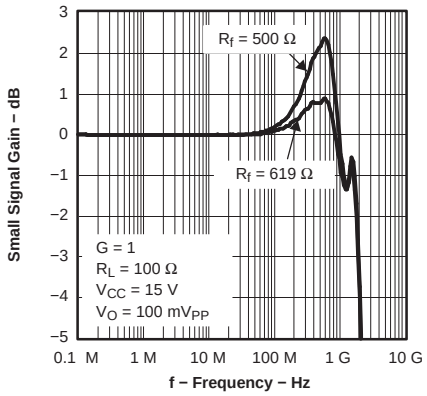


Figure 2.

SMALL-SIGNAL FREQUENCY RESPONSE

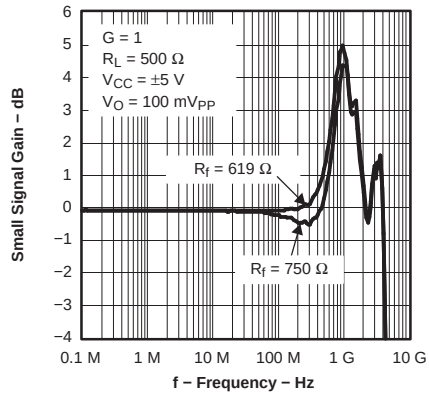


Figure 3.

SMALL-SIGNAL FREQUENCY RESPONSE

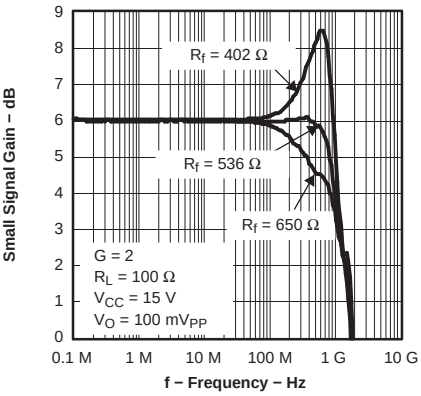


Figure 4.

SMALL-SIGNAL FREQUENCY RESPONSE

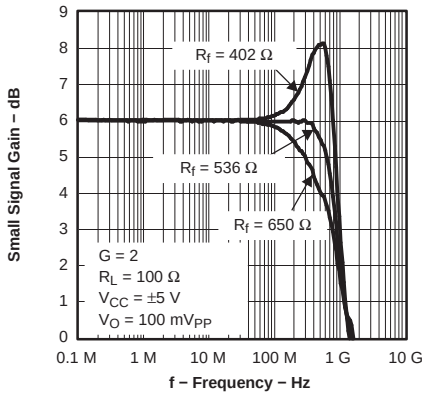


Figure 5.

SMALL-SIGNAL FREQUENCY RESPONSE

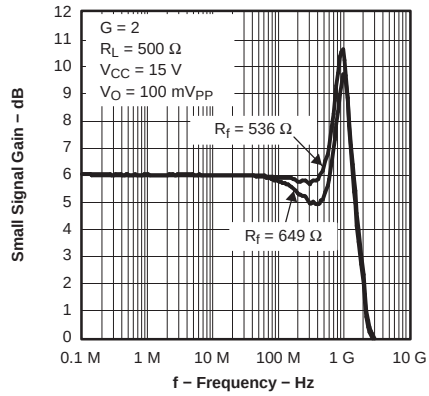


Figure 6.

SMALL-SIGNAL FREQUENCY RESPONSE

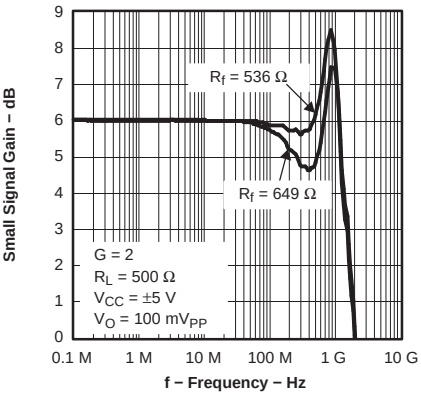


Figure 7.

SMALL-SIGNAL FREQUENCY RESPONSE

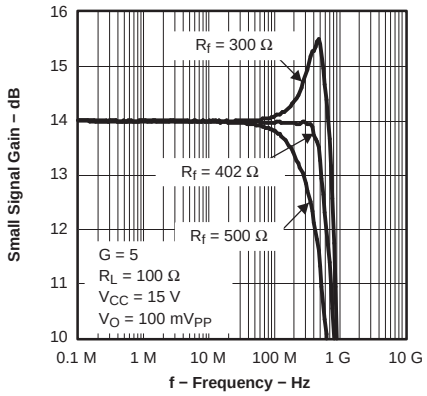


Figure 8.

SMALL-SIGNAL FREQUENCY RESPONSE

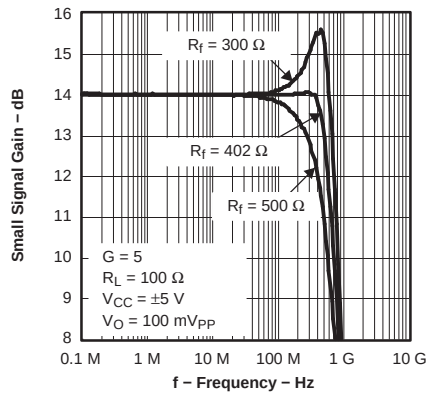


Figure 9.

TYPICAL CHARACTERISTICS (continued)

SMALL-SIGNAL FREQUENCY RESPONSE

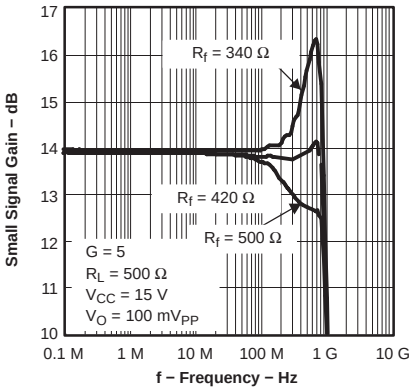


Figure 10.

SMALL-SIGNAL FREQUENCY RESPONSE

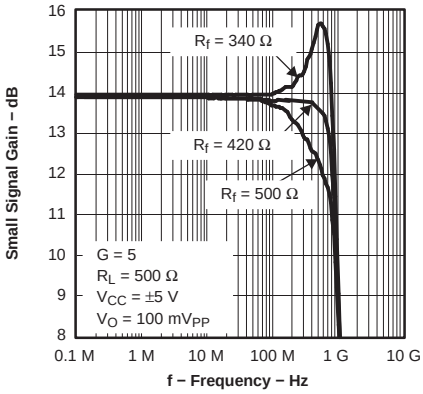


Figure 11.

SMALL-SIGNAL FREQUENCY RESPONSE

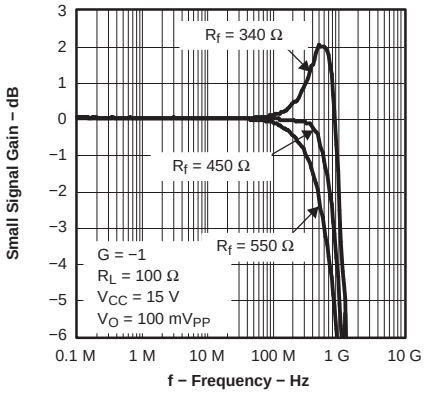


Figure 12.

SMALL-SIGNAL FREQUENCY RESPONSE

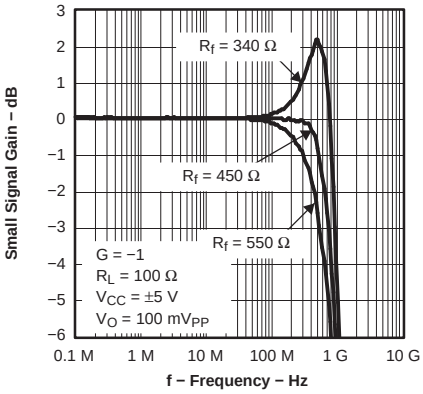


Figure 13.

SMALL-SIGNAL FREQUENCY RESPONSE

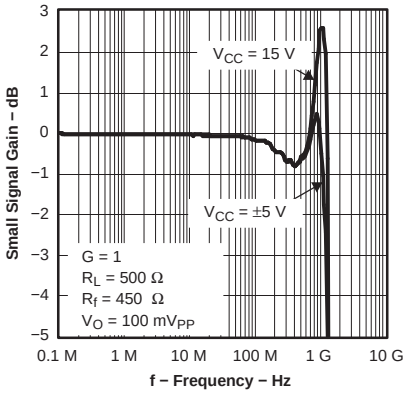


Figure 14.

LARGE-SIGNAL FREQUENCY RESPONSE

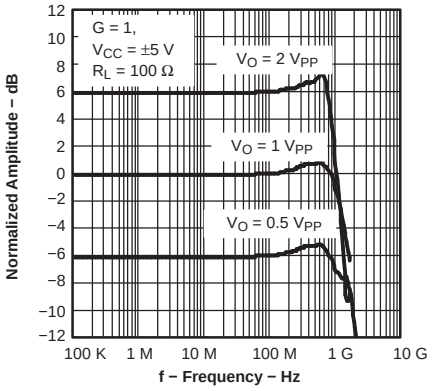


Figure 15.

LARGE-SIGNAL FREQUENCY RESPONSE

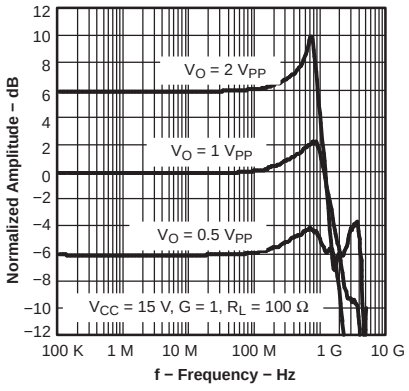


Figure 16.

LARGE-SIGNAL FREQUENCY RESPONSE

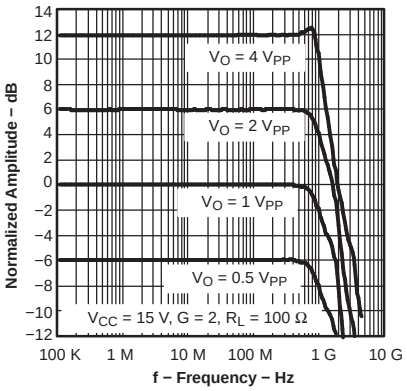


Figure 17.

LARGE-SIGNAL FREQUENCY RESPONSE

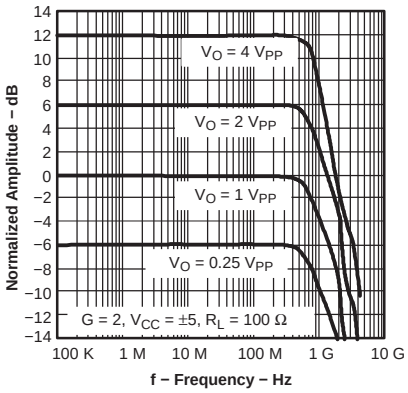


Figure 18.

TYPICAL CHARACTERISTICS (continued)

HARMONIC DISTORTION vs FREQUENCY

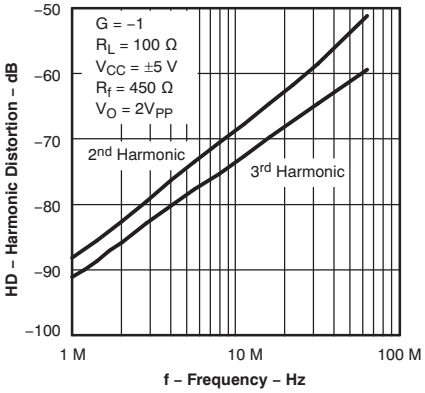


Figure 19.

HARMONIC DISTORTION vs FREQUENCY

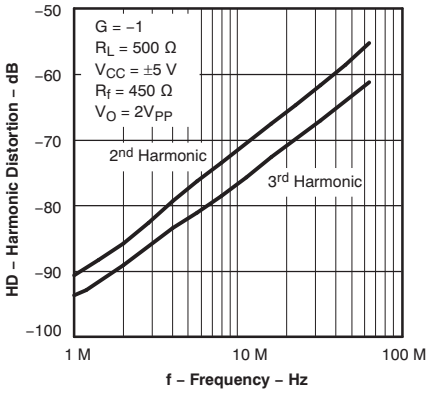


Figure 20.

HARMONIC DISTORTION vs FREQUENCY

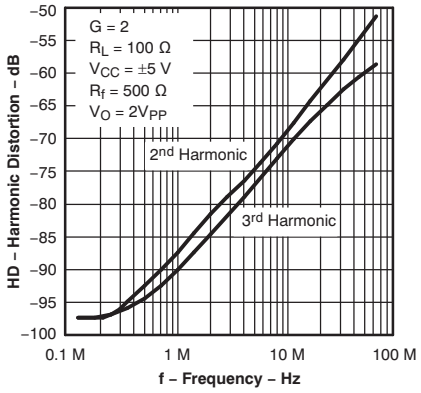


Figure 21.

HARMONIC DISTORTION vs FREQUENCY

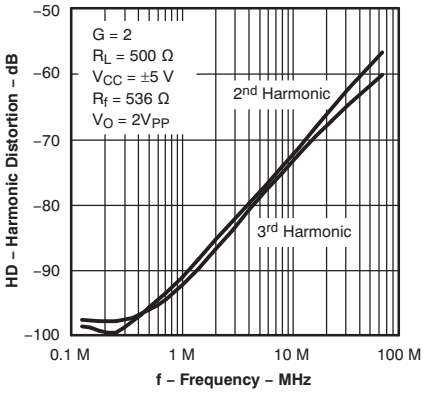


Figure 22.

HARMONIC DISTORTION vs FREQUENCY

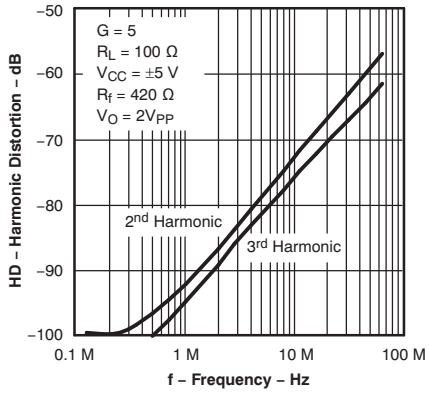


Figure 23.

HARMONIC DISTORTION vs FREQUENCY

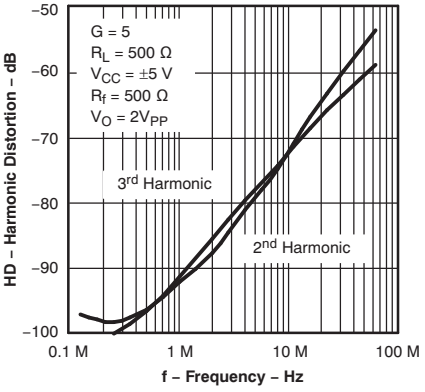


Figure 24.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

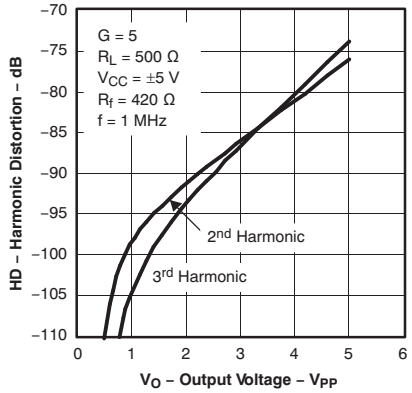


Figure 25.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

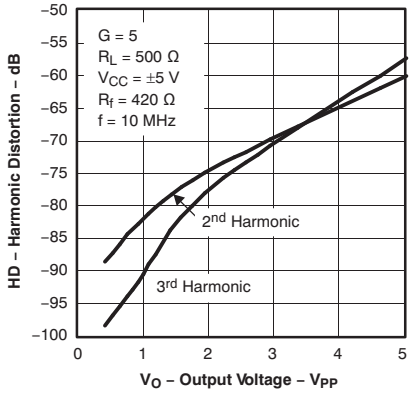


Figure 26.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

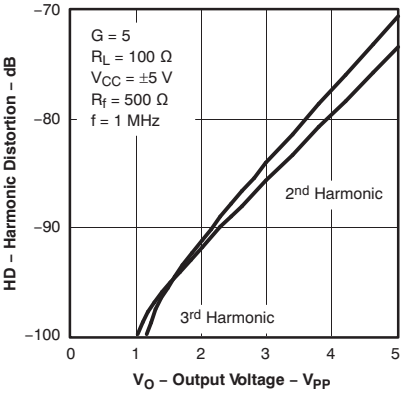


Figure 27.

TYPICAL CHARACTERISTICS (continued)

HARMONIC DISTORTION vs OUTPUT VOLTAGE

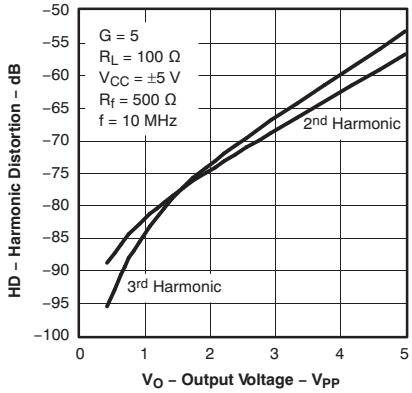


Figure 28.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

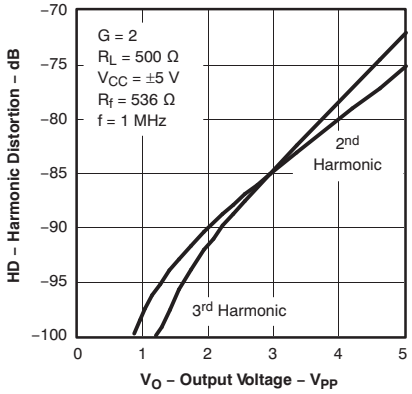


Figure 29.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

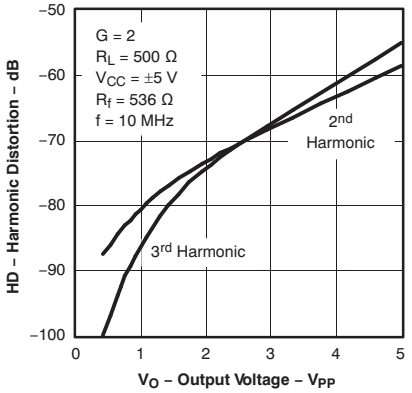


Figure 30.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

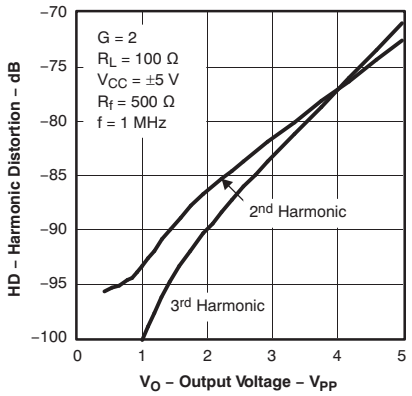


Figure 31.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

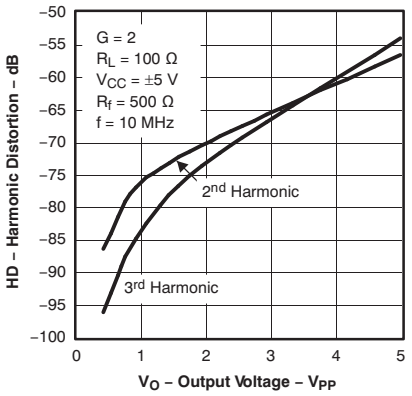


Figure 32.

THS3202 IMD3 vs FREQUENCY

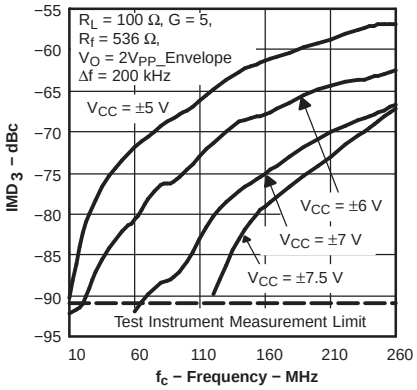


Figure 33.

THS3202 IMD3 vs FREQUENCY

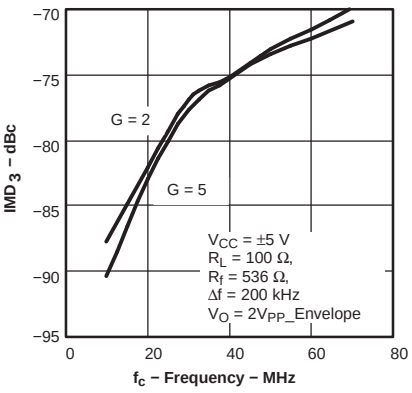


Figure 34.

THS3202 OIP3 vs FREQUENCY

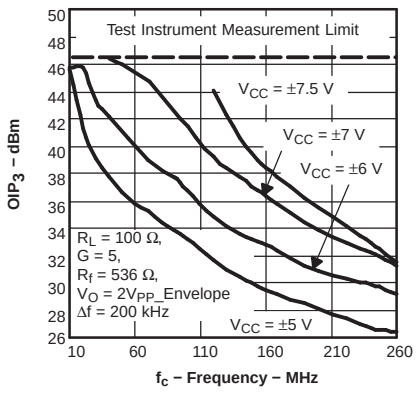


Figure 35.

THS3202 OIP3 vs FREQUENCY

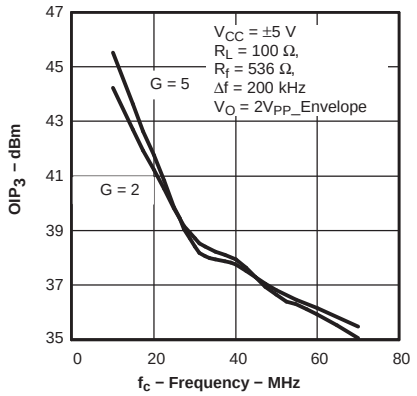
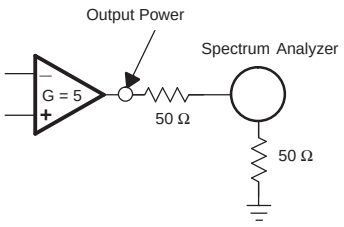


Figure 36.

TYPICAL CHARACTERISTICS (continued)

TEST CIRCUIT FOR IMD3/OIP3

TEST CIRCUIT FOR IMD_3 / OIP_3



This circuit applies to figures 46 through 49

Figure 37.

S-PARAMETER vs FREQUENCY

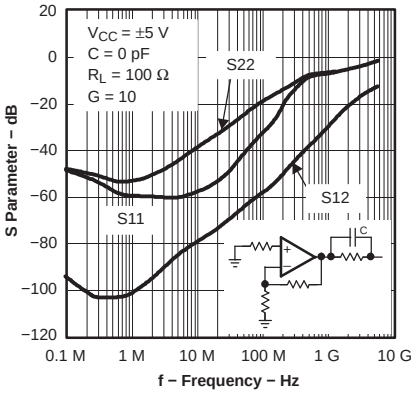


Figure 38.

S-PARAMETER vs FREQUENCY

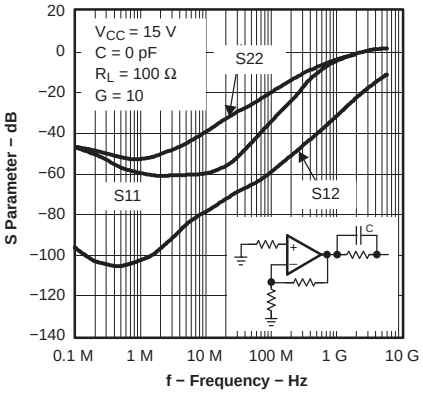


Figure 39.

S-PARAMETER vs FREQUENCY

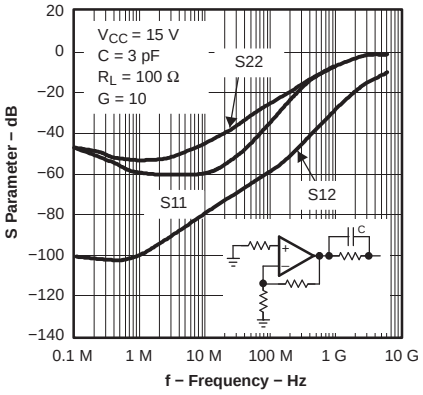


Figure 40.

S-PARAMETER vs FREQUENCY

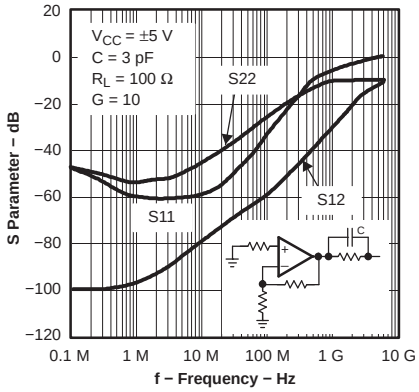


Figure 41.

INPUT CURRENT NOISE DENSITY vs FREQUENCY

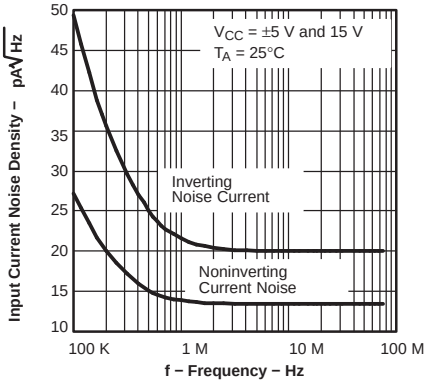


Figure 42.

VOLTAGE NOISE DENSITY vs FREQUENCY

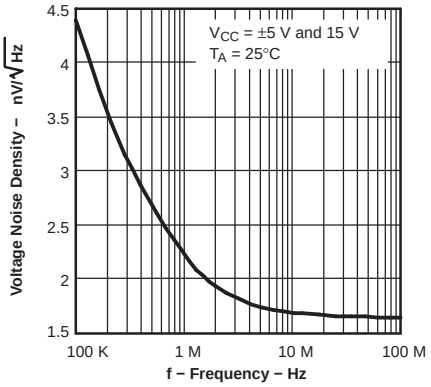


Figure 43.

TRANSIMPEDANCE vs FREQUENCY

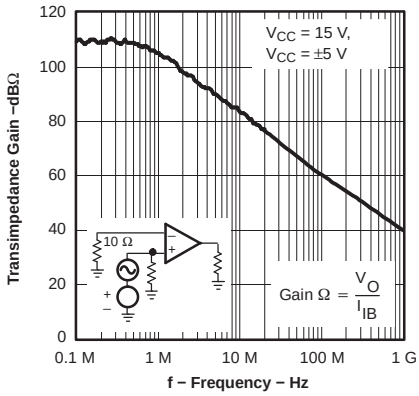


Figure 44.

OUTPUT IMPEDANCE vs FREQUENCY

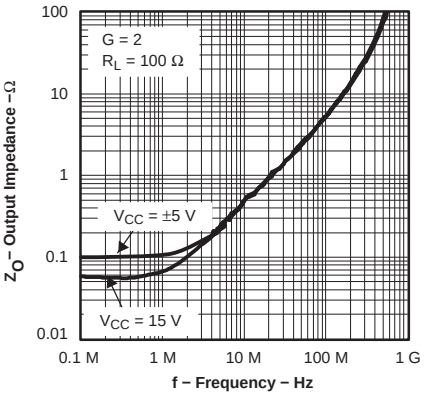


Figure 45.

TYPICAL CHARACTERISTICS (continued)

THS3202
IMPEDANCE OF INVERTING INPUT

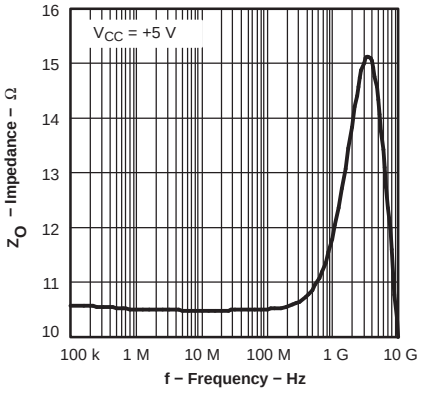


Figure 46.

SUPPLY CURRENT/CHANNEL
vs
SUPPLY VOLTAGE

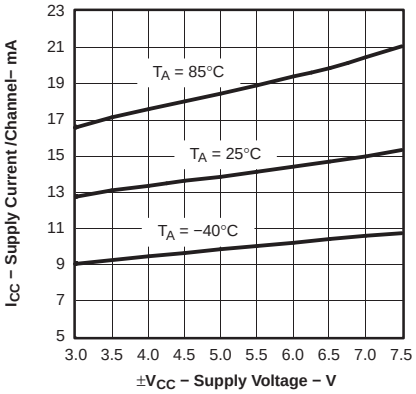


Figure 47.

INPUT OFFSET VOLTAGE
vs
FREE-AIR TEMPERATURE

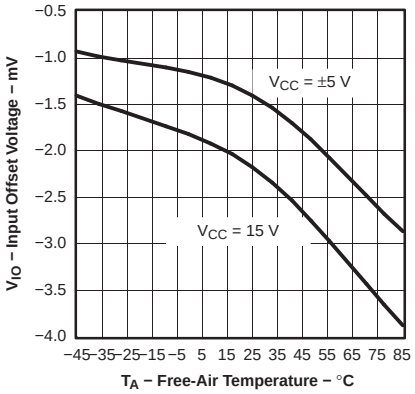


Figure 48.

OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE RANGE

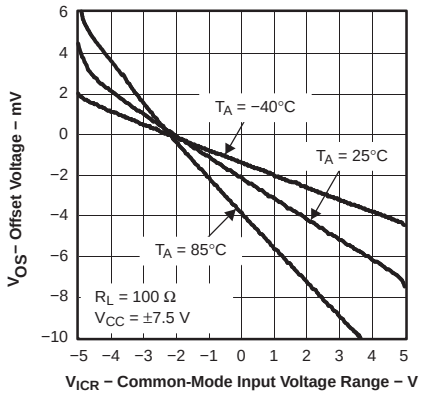


Figure 49.

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

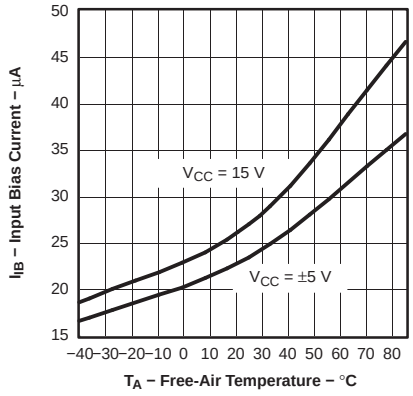


Figure 50.

INPUT BIAS CURRENT
vs
INPUT COMMON-MODE RANGE

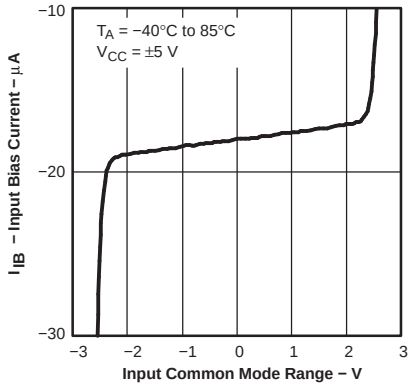


Figure 51.

POSITIVE POWER-SUPPLY REJECTION RATIO vs POSITIVE POWER SUPPLY

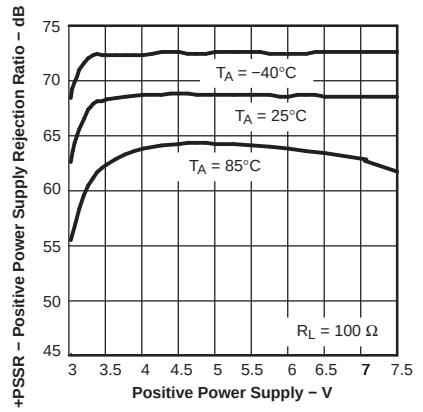


Figure 52.

NEGATIVE POWER-SUPPLY REJECTION RATIO vs NEGATIVE POWER SUPPLY

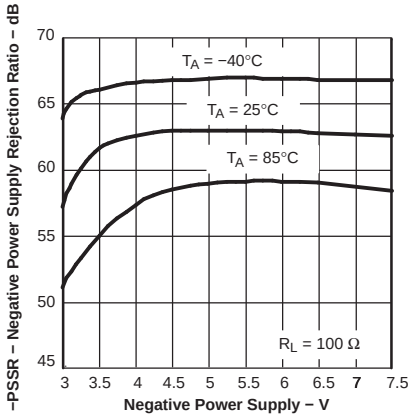


Figure 53.

POSITIVE OUTPUT VOLTAGE SWING vs FREE-AIR TEMPERATURE

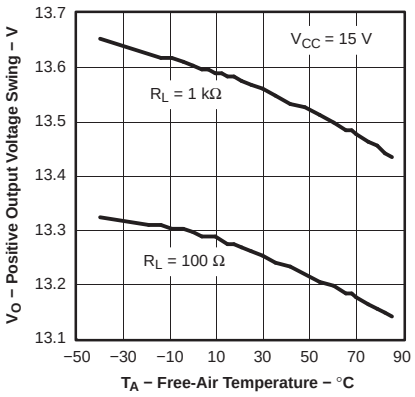


Figure 54.

TYPICAL CHARACTERISTICS (continued)

POSITIVE OUTPUT VOLTAGE SWING vs FREE-AIR TEMPERATURE

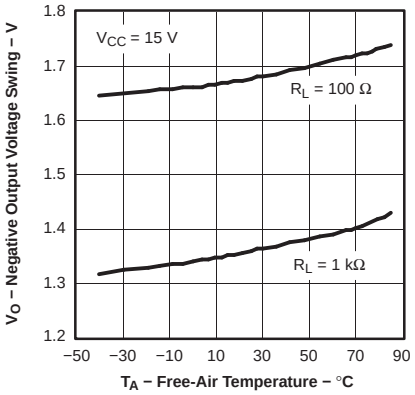


Figure 55.

NEGATIVE OUTPUT VOLTAGE SWING vs FREE-AIR TEMPERATURE

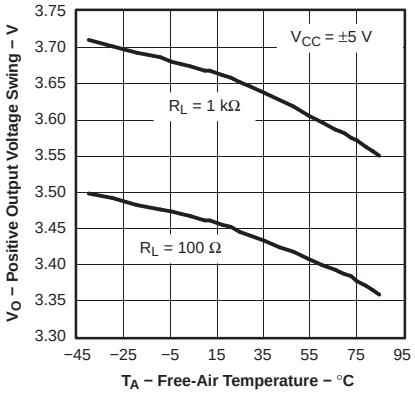


Figure 56.

NEGATIVE OUTPUT VOLTAGE SWING vs FREE-AIR TEMPERATURE

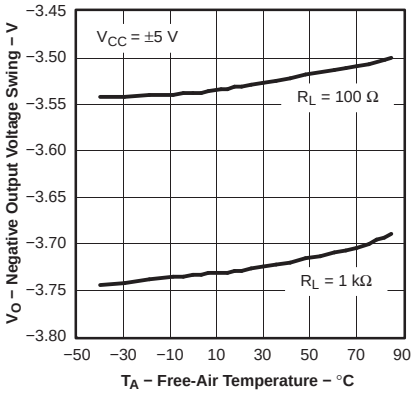


Figure 57.

OUTPUT CURRENT SINKING vs POWER SUPPLY

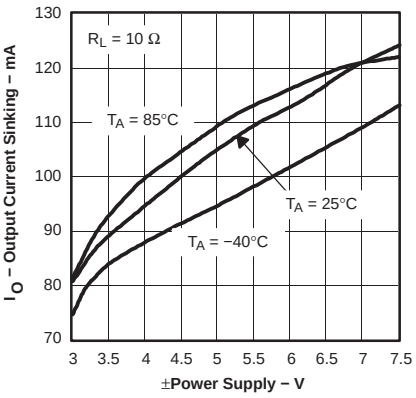


Figure 58.

OUTPUT CURRENT SOURCING vs POWER SUPPLY

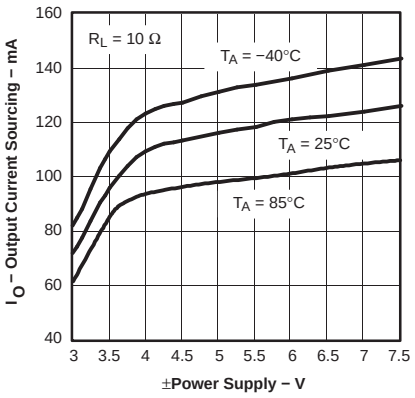


Figure 59.

OVERDRIVE RECOVERY TIME

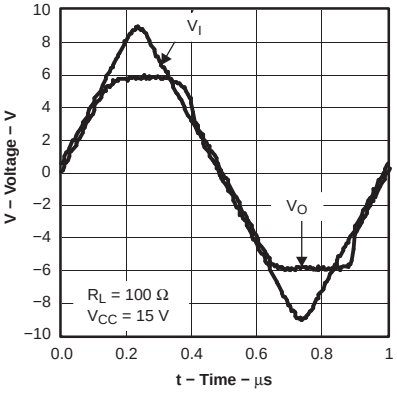


Figure 60.

OVERDRIVE RECOVERY TIME

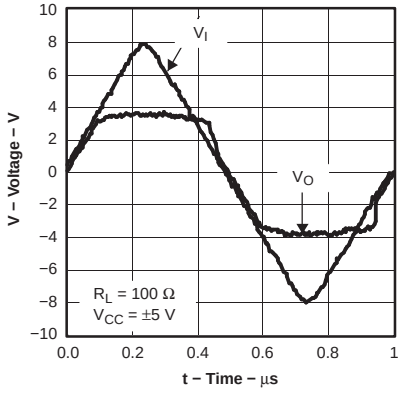


Figure 61.

SLEW RATE vs OUTPUT VOLTAGE

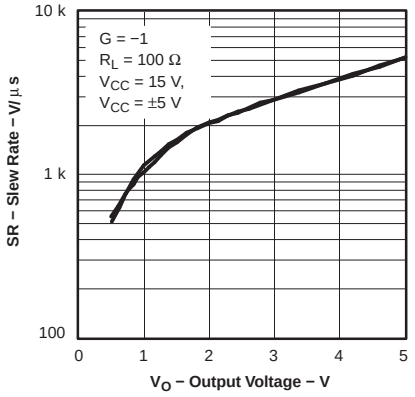


Figure 62.

SLEW RATE vs OUTPUT VOLTAGE

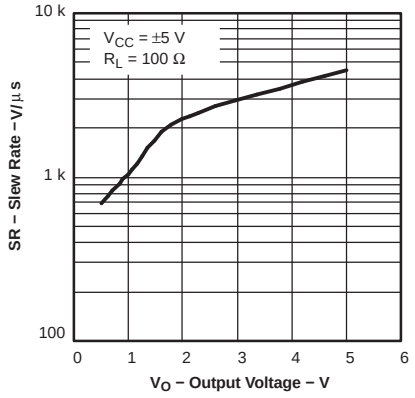


Figure 63.

TYPICAL CHARACTERISTICS (continued)

SLEW RATE vs OUTPUT VOLTAGE

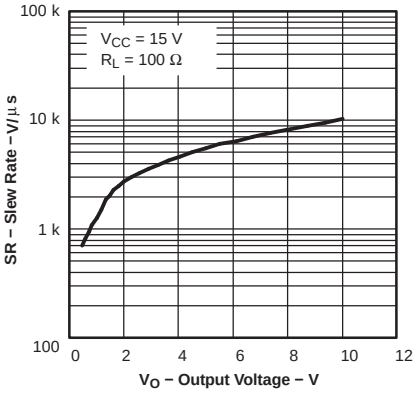


Figure 64.

OUTPUT VOLTAGE TRANSIENT RESPONSE

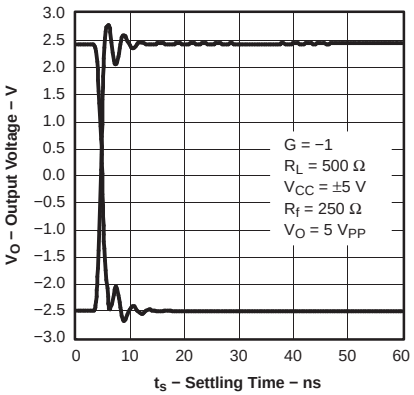


Figure 65.

SETTLING TIME

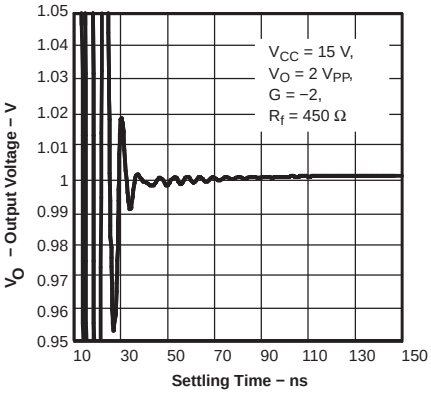


Figure 66.

SETTLING TIME

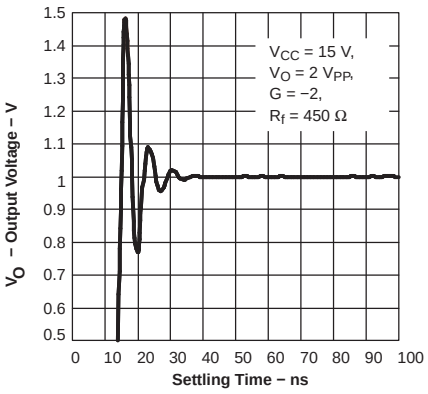


Figure 67.

DC COMMON-MODE REJECTION RATIO HIGH vs INPUT COMMON-MODE RANGE

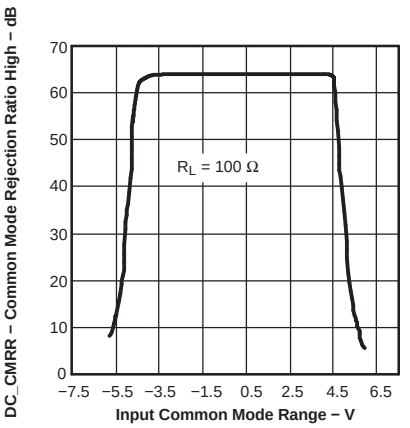


Figure 68.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

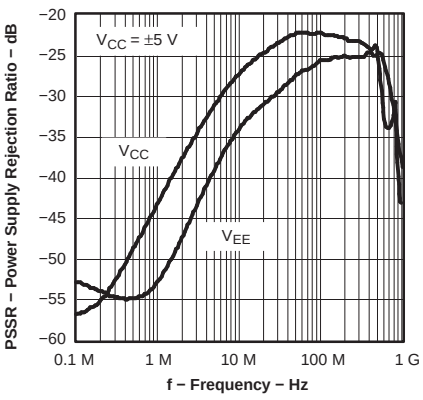


Figure 69.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

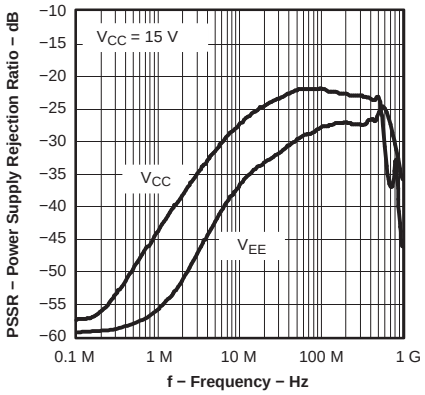


Figure 70.

DIFFERENTIAL GAIN ERROR vs 150-Ω LOADS

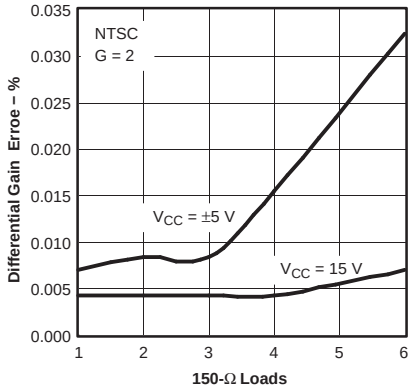


Figure 71.

DIFFERENTIAL GAIN ERROR vs 150-Ω LOADS

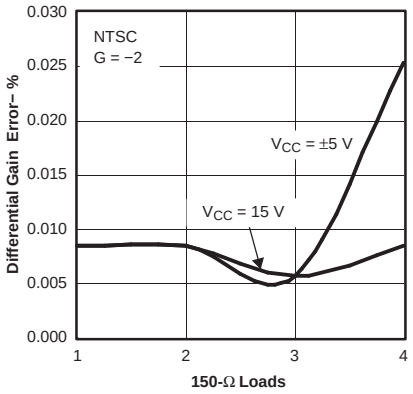


Figure 72.

TYPICAL CHARACTERISTICS (continued)

DIFFERENTIAL PHASE ERROR vs 150-Ω LOADS

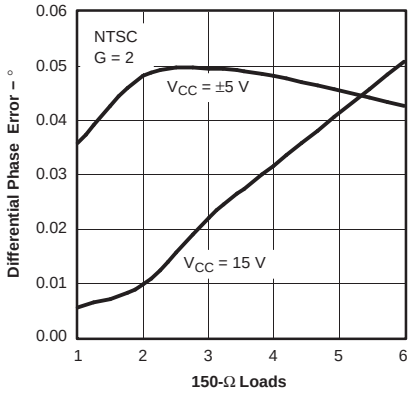


Figure 73.

DIFFERENTIAL PHASE ERROR vs 150-Ω LOADS

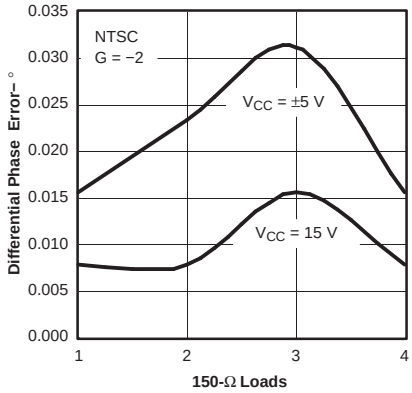


Figure 74.

DIFFERENTIAL GAIN ERROR vs 150-Ω LOADS

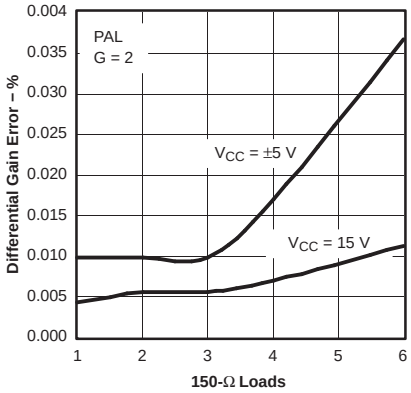


Figure 75.

DIFFERENTIAL PHASE ERROR vs 150-Ω LOADS

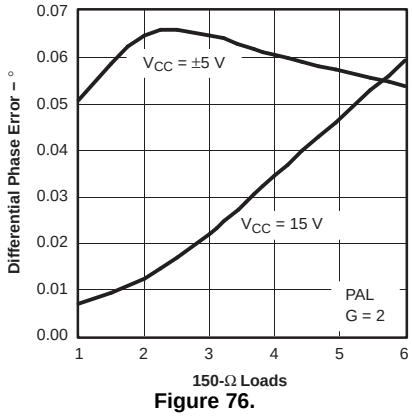


Figure 76.

APPLICATION INFORMATION

INTRODUCTION

The THS3202 is a high-speed, operational amplifier configured in a current-feedback architecture. The device is built using Texas Instruments BiCOM-II process, a 15-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing f_Ts of several GHz. This configuration implements an exceptionally high-performance amplifier that has a wide bandwidth, high slew rate, fast settling time, and low distortion.

RECOMMENDED FEEDBACK AND GAIN RESISTOR VALUES

As with all current-feedback amplifiers, the bandwidth of the THS3202 is an inversely proportional function of the value of the feedback resistor. The recommended resistors for the optimum frequency response are shown in Table 1. These should be used as a starting point and once optimum values are found, 1% tolerance resistors should be used to maintain frequency response characteristics. For most applications, a feedback resistor value of 750 Ω is recommended—a good compromise between bandwidth and phase margin that yields a very stable amplifier.

Table 1. Recommended Resistor Values for Optimum Frequency Response

THS3202 R_F FOR AC WHEN R_{LOAD} = 100 Ω			
GAIN	V_{SUP}	PEAKING	R_F VALUE
1	15	Optimum	619
	±5	Optimum	619
2	15	Optimum	536
	±5	Optimum	536
5	15	Optimum	402
	±5	Optimum	402
10	15	Optimum	200
	±5	Optimum	200
–1	15	Optimum	450
	±5	Optimum	450

As shown in Table 1, to maintain the highest bandwidth with an increasing gain, the feedback resistor is reduced. The advantage of dropping the feedback resistor (and the gain resistor) is that the noise of the system is also reduced compared to no reduction of these resistor values (see the *Noise Calculations* section). Thus, keeping the bandwidth as high as possible maintains very good distortion performance of the amplifier by keeping the excess loop gain as high as possible.

Care must be taken to not drop these values too low. The amplifier output must drive the feedback resistance (and gain resistance) and may place a burden on the amplifier. The end result is that distortion may actually increase due to the low impedance load presented to the amplifier. Careful management of the amplifier bandwidth and the associated loading effects must be examined by the designer for optimum performance.

The THS3202 amplifier exhibits very good distortion performance and bandwidth with the capability of utilizing up to 15-V supplies. Their excellent current drive capability of up to 115 mA driving into a 20-Ω load allows for many versatile applications. One application is driving a twisted pair line (for example, a telephone line). Figure 77 shows a simple circuit for driving a twisted pair differentially.

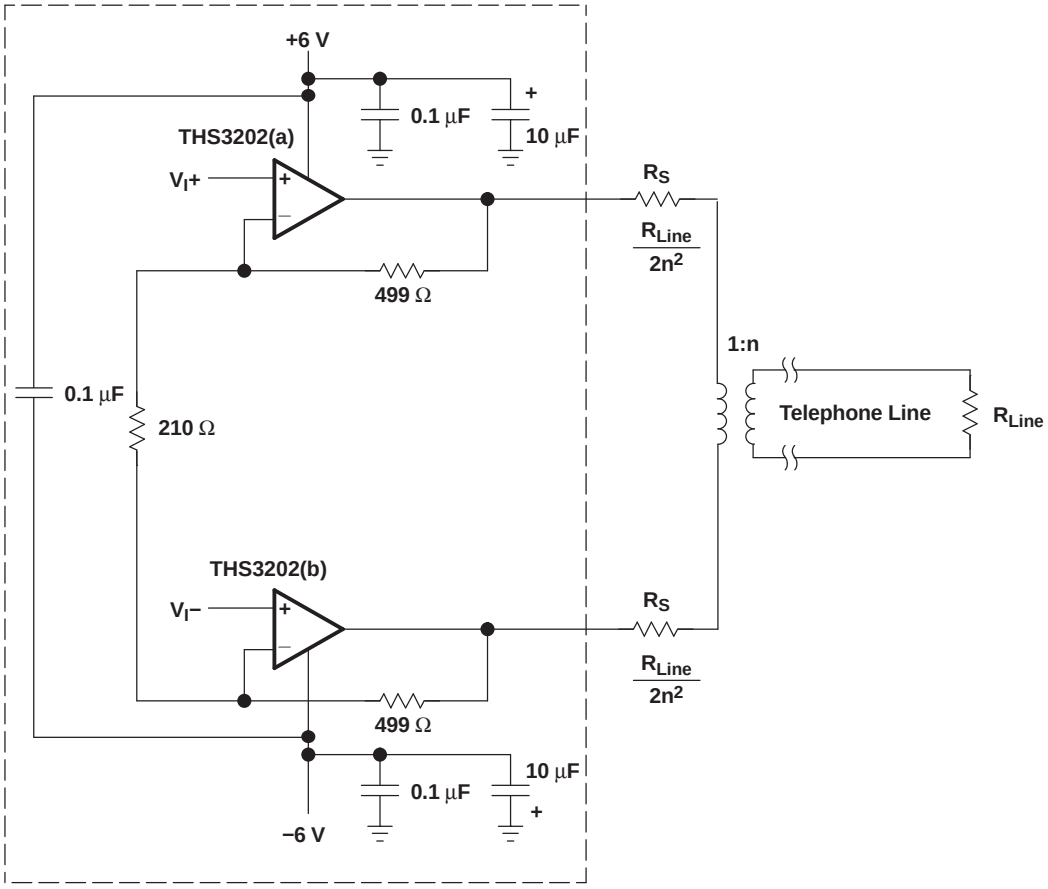


Figure 77. Simple Line Driver With THS3202

Due to the large power-supply voltages and the large current drive capability, power dissipation of the amplifier must not be neglected. To have as much power dissipation as possible in a small package, the THS3202 is available in an MSOP-8 package (DGK), an MSOP-8 PowerPAD package (DGN), and an SOIC-8 package (D). Again, power dissipation of the amplifier must be carefully examined or else the amplifiers could become too hot and performance can be severely degraded. See the *Power Dissipation and Thermal Considerations* section for more information on thermal management.

NOISE CALCULATIONS

Noise can cause errors on very small signals. This is especially true for amplifying small signals coming over a transmission line or an antenna. The noise model for current-feedback amplifiers (CFB) is the same as for voltage feedback amplifiers (VFB). The only difference between the two is that CFB amplifiers generally specify different current-noise parameters for each input, while VFB amplifiers usually only specify one noise-current parameter. The noise model is shown in Figure 78. This model includes all of the noise sources as follows:

- e_n = Amplifier internal voltage noise (nV/$\sqrt{Hz}$)
- IN+ = Noninverting current noise (pA/$\sqrt{Hz}$)
- IN− = Inverting current noise (pA/$\sqrt{Hz}$)
- e_{Rx} = Thermal voltage noise associated with each resistor (e_{Rx} = 4 kTR_x)

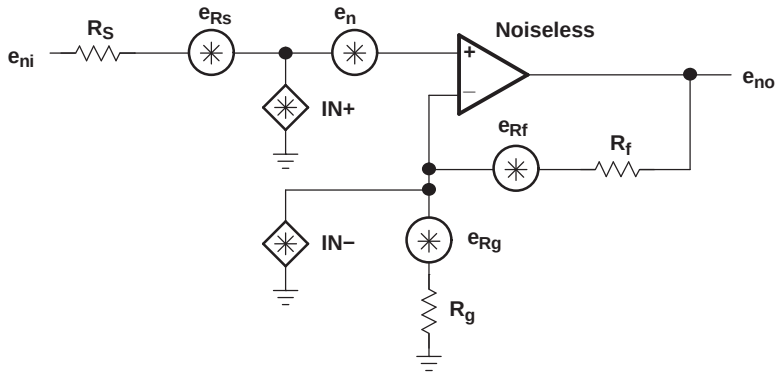


Figure 78. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN+ \times R_S\right)^2 + \left(IN- \times \left(R_f \parallel R_g\right)\right)^2 + 4\,kTR_S + 4\,kT\left(R_f \parallel R_g\right)}$$

where:

k = Boltzmann's constant = 1.380658×10^{-23}
T = Temperature in degrees Kelvin (273 +°C)
$R_f \parallel R_g$ = Parallel resistance of R_f and R_g

To get the equivalent output noise of the amplifier, multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\,A_V = e_{ni}\left(1 + \frac{R_f}{R_g}\right) \text{ (Noninverting Case)}$$

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing R_F and R_G), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier.

This brings up another noise measurement usually preferred in RF applications, the noise figure (NF). Noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

$$NF = 10\log\left[\frac{e_{ni}^2}{e_{Rs}^2}\right]$$

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate the noise figure as:

$$NF = 10\log\left[1 + \frac{\left[\left(e_n\right)^2 + \left(IN + \times R_S\right)^2\right]}{4\,kTR_S}\right]$$

PRINTED-CIRCUIT BOARD LAYOUT TECHNIQUES FOR OPTIMAL PERFORMANCE

Achieving optimum performance with high-frequency amplifier-like devices in the THS320x family requires careful attention to board layout parasitic and external component types.

Recommendations that optimize performance include:

- Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and input pins can cause instability. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.
- Minimize the distance (< 0.25” or < 6,35 mm) from the power-supply pins to high-frequency 0.1-µF and 100 pF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. Larger (6.8 µF or more) tantalum decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the printed circuit board (PCB). The primary goal is to minimize the impedance seen in the differential-current return paths. For driving differential loads with the THS3202, adding a capacitor between the power-supply pins improves 2nd order harmonic distortion performance. This also minimizes the current loop formed by the differential drive.
- Careful selection and placement of external components preserve the high-frequency performance of the THS320x family. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Again, keep their leads and PCB trace length as short as possible. Never use wirewound type resistors in a high-frequency application. Because the output pin and inverting input pins are the most sensitive to parasitic capacitance, always position the feedback and series output resistors, if any, as close as possible to the inverting input pins and output pins. Other network components, such as input termination resistors, should be placed close to the gain-setting resistors. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values greater than 2.0 kΩ, this parasitic capacitance can add a pole and/or a zero that can affect circuit operation. Keep resistor values as low as possible, consistent with load driving considerations.
- Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils or 1,27 mm to 2,54 mm) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and determine if isolation resistors on the outputs are necessary. Low parasitic capacitive loads (less than 4 pF) may not need an R_S because the THS320x family is nominally compensated to operate with a 2-pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated

transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques).

A 50-Ω environment is not necessary onboard, and in fact, a higher impedance environment improves distortion as shown in the distortion versus load plots. With a characteristic board trace impedance based on board material and trace dimensions, a matching series resistor into the trace from the output of the THS320x is used as well as a terminating shunt resistor at the input of the destination device.

Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. If the 6-dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case. This does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there is some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

- Socketing a high-speed part like the THS320x family is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the THS320x family devices directly onto the board.

PowerPAD DESIGN CONSIDERATIONS

The THS320x family is available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted [see Figure 79(a) and Figure 79(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 79(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.

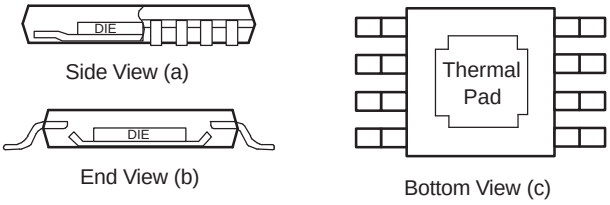


Figure 79. Views of Thermally-Enhanced Package

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

PowerPAD PCB LAYOUT CONSIDERATIONS

1. Prepare the PCB with a top side etch pattern as shown in Figure 80. There should be etch for the leads as well as etch for the thermal pad.

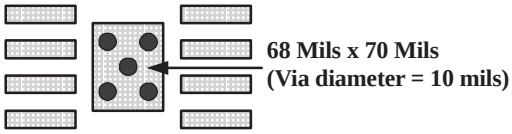


Figure 80. DGN PowerPAD PCB Etch and Via Pattern

2. Place five holes in the area of the thermal pad. These holes should be 10 mils (0,254 mm) in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the THS320x family IC. These additional vias may be larger than the 10-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS320x family PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

POWER DISSIPATION AND THERMAL CONSIDERATIONS

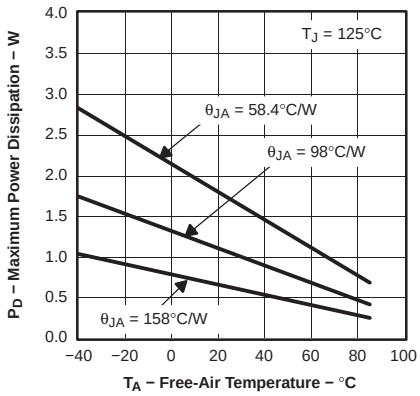
To maintain maximum output capabilities, the THS3202 does not incorporate automatic thermal shutoff protection. The designer must take care to ensure that the design does not violate the absolute maximum junction temperature of the device. Failure may result if the absolute maximum junction temperature of +150°C is exceeded. For best performance, design for a maximum junction temperature of +125°C. Between +125°C and +150°C, damage does not occur, but the performance of the amplifier begins to degrade.

The thermal characteristics of the device are dictated by the package and the PCB. Maximum power dissipation for a given package can be calculated using the following formula.

$$P_{Dmax} = \frac{T_{max} - T_A}{\theta_{JA}}$$

where:
P_{Dmax} is the maximum power dissipation in the amplifier (W).
T_{max} is the absolute maximum junction temperature (°C).
T_A is the ambient temperature (°C).
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} is the thermal coefficient from the silicon junctions to the case (°C/W).
θ_{CA} is the thermal coefficient from the case to ambient air (°C/W).

For systems where heat dissipation is more critical, the THS320x family of devices is offered in an MSOP-8 with PowerPAD. The thermal coefficient for the PowerPAD packages are substantially improved over the traditional SOIC. Maximum power dissipation levels are depicted in the graph for the available packages. The data for the PowerPAD packages assume a board layout that follows the PowerPAD layout guidelines referenced above and detailed in the PowerPAD application note number SLMA002. The following graph also illustrates the effect of not soldering the PowerPAD to a PCB. The thermal impedance increases substantially which may cause serious heat and performance issues. Be sure to always solder the PowerPAD to the PCB for optimum performance.



Results are With No Air Flow and PCB Size = 3”x3”
θ_{JA} = 58.4°C/W for 8-Pin MSOP w/PowerPad (DGN)
θ_{JA} = 98°C/W for 8-Pin SOIC High Test PCB (D)
θ_{JA} = 158°C/W for 8-Pin MSOP w/PowerPad w/o Solder

Figure 81. Maximum Power Dissipation vs Ambient Temperature

When determining whether or not the device satisfies the maximum power dissipation requirement, it is important to not only consider quiescent power dissipation, but also dynamic power dissipation. Often times, this is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation can provide visibility into a possible problem.

DRIVING A CAPACITIVE LOAD

Driving capacitive loads with high-performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS3202 has been internally compensated to maximize its bandwidth and slew-rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output decreases the device's phase margin leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 82. A minimum value of 10 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

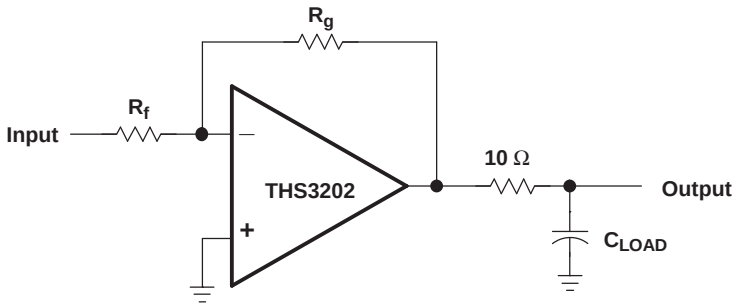
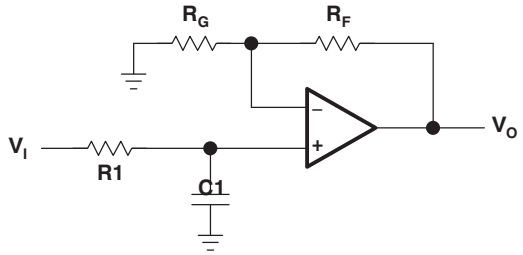


Figure 82. Driving a Capacitive Load

GENERAL CONFIGURATIONS

A common error for the first-time CFB user is creating a unity-gain buffer amplifier by shorting the output directly to the inverting input. A CFB amplifier in this configuration oscillates and is *not* recommended. The THS3202, like all CFB amplifiers, *must* have a feedback resistor for stable operation. Additionally, placing capacitors directly from the output to the inverting input is not recommended. This is because, at high frequencies, a capacitor has a very low impedance. This results in an unstable amplifier and should not be considered when using a current-feedback amplifier. Because of this, integrators and simple low-pass filters, which are easily implemented on a VFB amplifier, have to be designed slightly differently. If filtering is required, simply place an RC-filter at the noninverting terminal of the operational amplifier, as shown in Figure 83.

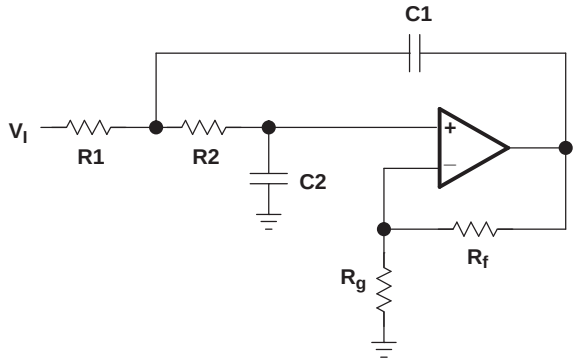


$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

Figure 83. Single-Pole Low-Pass Filter

If a multiple-pole filter is required, the use of a Sallen-Key filter can work very well with CFB amplifiers. This is because the filtering elements are not in the negative feedback loop and stability is not compromised. Because of their high slew-rates and high bandwidths, CFB amplifiers can create very accurate signals and help minimize distortion. An example is shown in Figure 84.



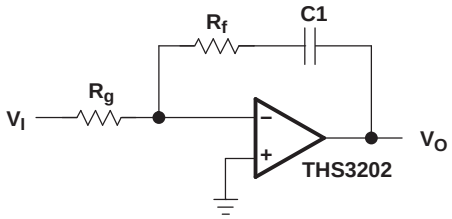
R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_g = \frac{R_f}{\left(2 - \frac{1}{Q}\right)}$$

Figure 84. 2-Pole Low-Pass Sallen-Key Filter

There are two simple ways to create an integrator with a CFB amplifier. The first, shown in Figure 85, adds a resistor in series with the capacitor. This is acceptable because at high frequencies, the resistor is dominant and the feedback impedance never drops below the resistor value. The second, shown in Figure 86, uses positive feedback to create the integration. Caution is advised because oscillations can occur due to the positive feedback.



$$\frac{V_O}{V_I} = \left(\frac{R_f}{R_g}\right)\left(\frac{S + \frac{1}{R_f C1}}{S}\right)$$

Figure 85. Inverting CFB Integrator

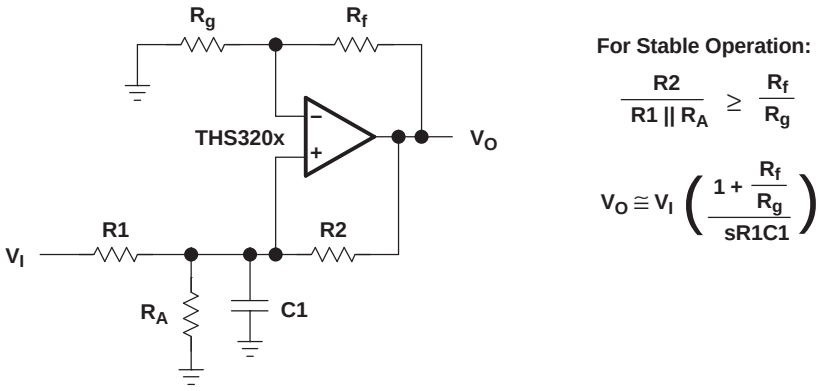


Figure 86. Noninverting CFB Integrator

The THS3202 may also be employed as a very good video distribution amplifier. One characteristic of distribution amplifiers is the fact that the differential phase (DP) and the differential gain (DG) are compromised as the number of lines increase and the closed-loop gain increases. Be sure to use termination resistors throughout the distribution system to minimize reflections and capacitive loading.

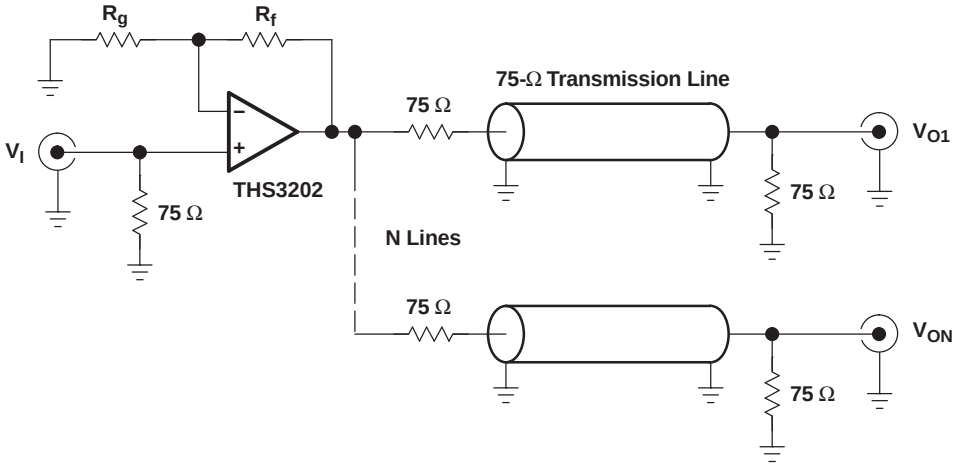


Figure 87. Video Distribution Amplifier Application

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (April 2009) to Revision F **Page**

- Updated document format to current standards 1
- Deleted *lead temperature* specification from Absolute Maximum Ratings table 2
- Changed first sentence of third paragraph of *Power Dissipation and Thermal Considerations* section 23

Changes from Revision D (January 2009) to Revision E **Page**

- Deleted feature bullets relating to IMD3 and OIP3 at V_{CC} = 15 V 1
- Replaced figures 1
- Changed text in first sentence of *Description* section 1
- Deleted harmonic distortion specifications in *AC Performance* subsection for V_{CC} = 15 V 6
- Deleted harmonic distortion graphs for V_{CC} = 15 V 10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS3202D	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3202	
THS3202DGK	NRND	VSSOP	DGK	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BEV	
THS3202DGN	NRND	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BEP	
THS3202DGNG4	NRND	HVSSOP	DGN	8	80	TBD	Call TI	Call TI	-40 to 85		
THS3202DGNR	NRND	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BEP	
THS3202DGNRG4	NRND	HVSSOP	DGN	8	2500	TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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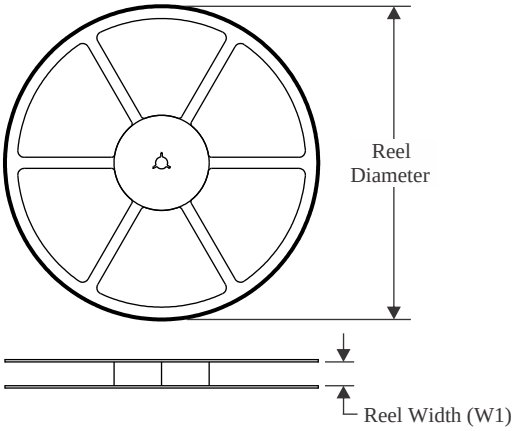
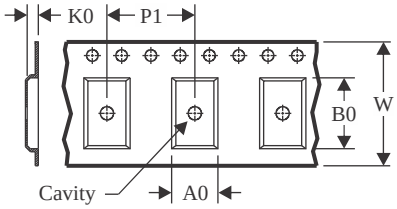
TAPE AND REEL INFORMATION

REEL DIMENSIONS

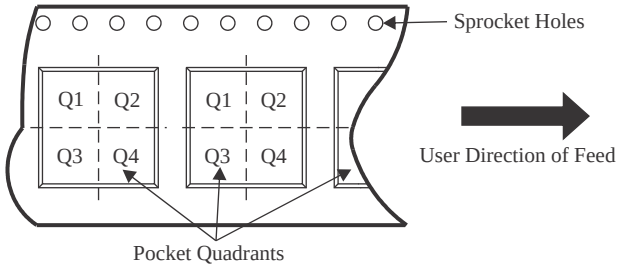


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

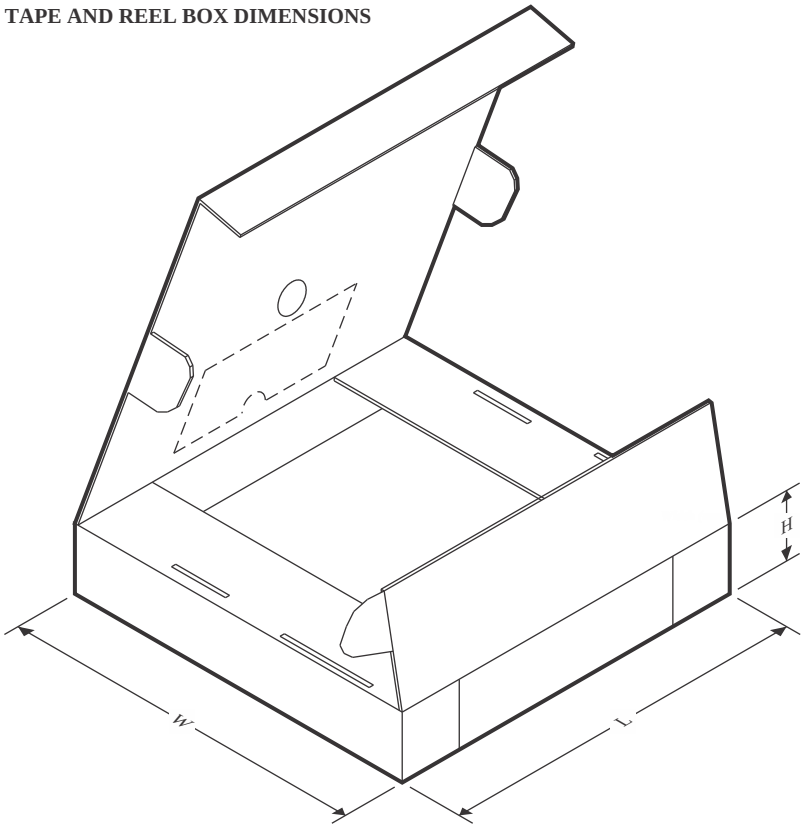
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS3202DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS3202DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

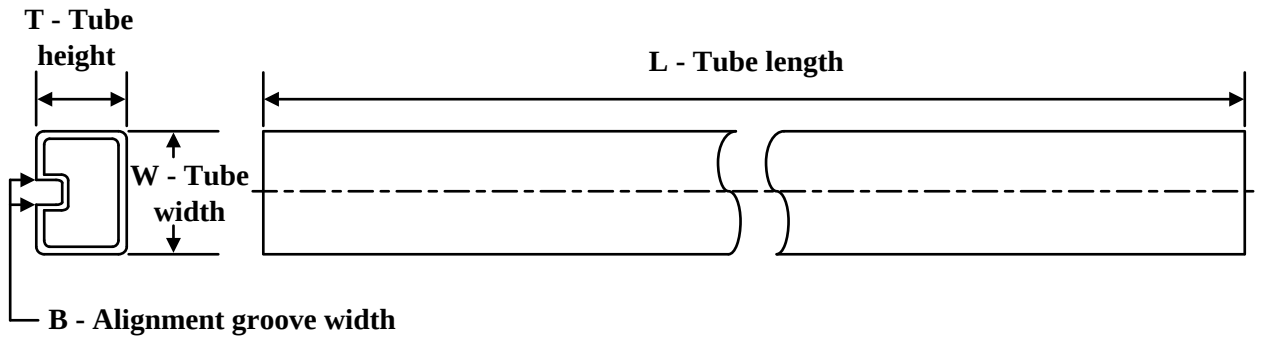
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS3202DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS3202DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS3202D	D	SOIC	8	75	505.46	6.76	3810	4
THS3202DGN	DGN	HVSSOP	8	80	330	6.55	500	2.88

GENERIC PACKAGE VIEW

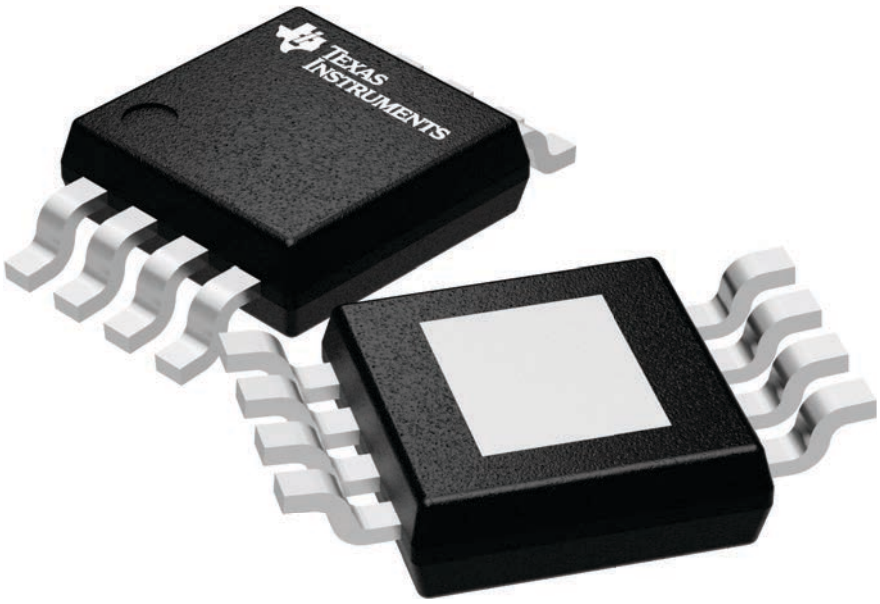
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

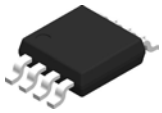
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

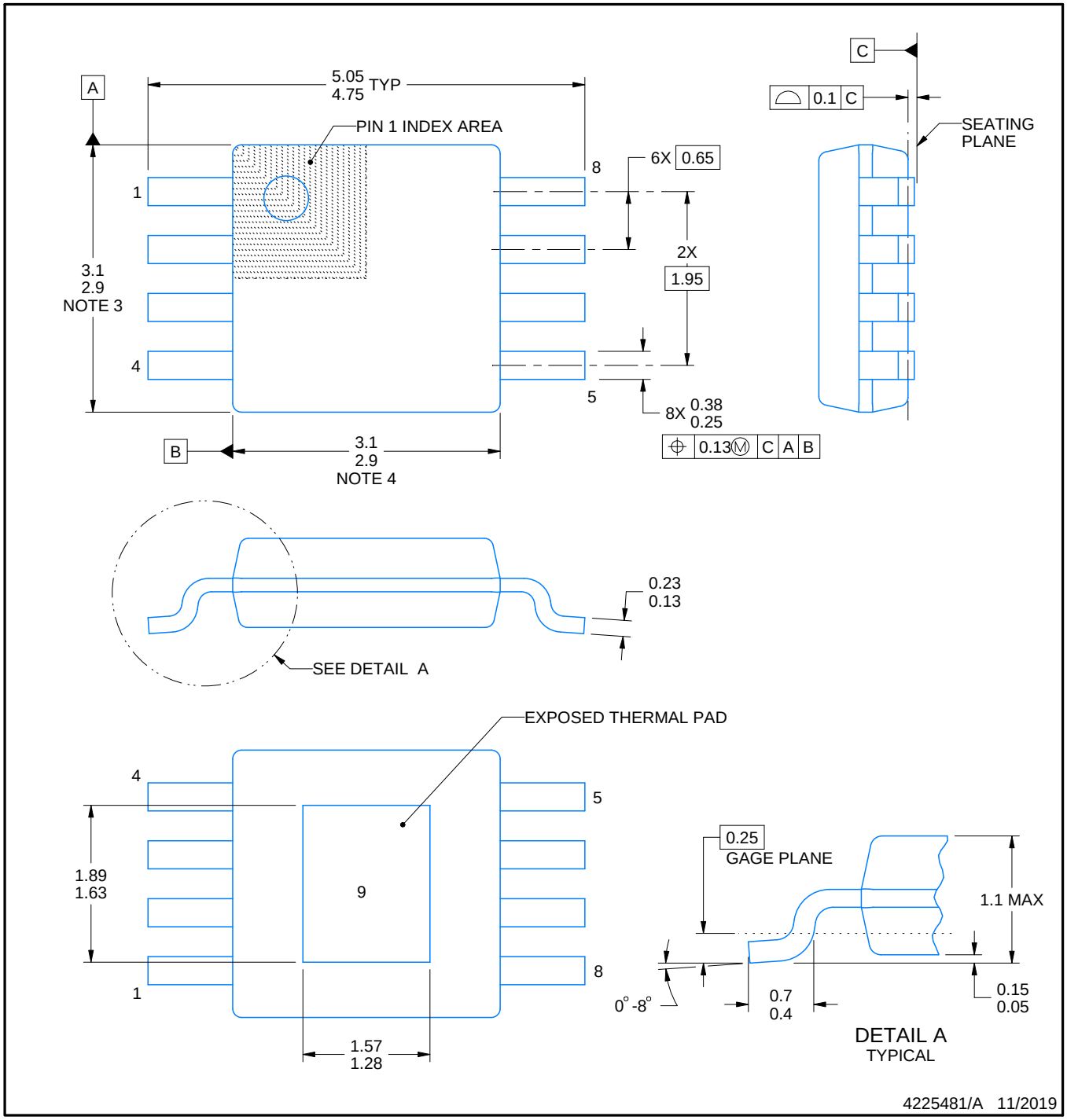
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

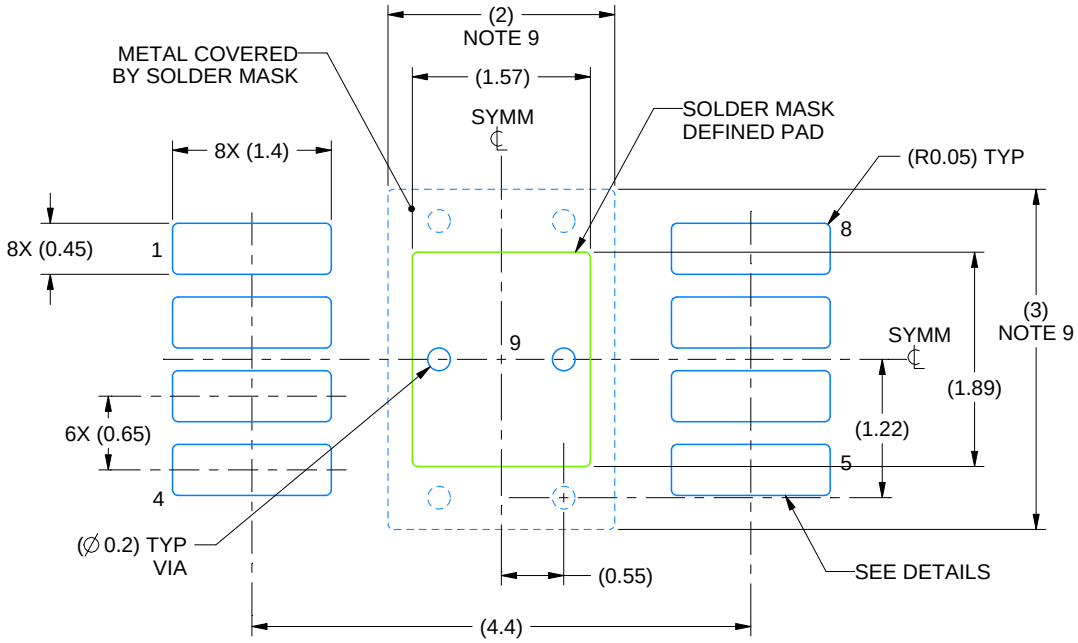
SMALL OUTLINE PACKAGE



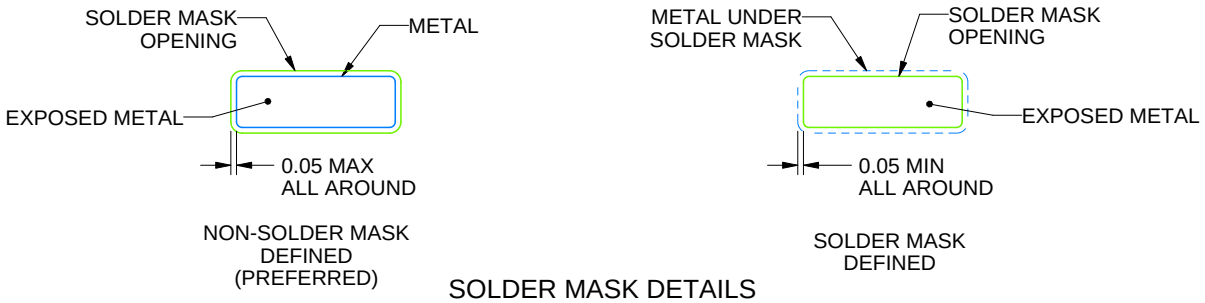
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

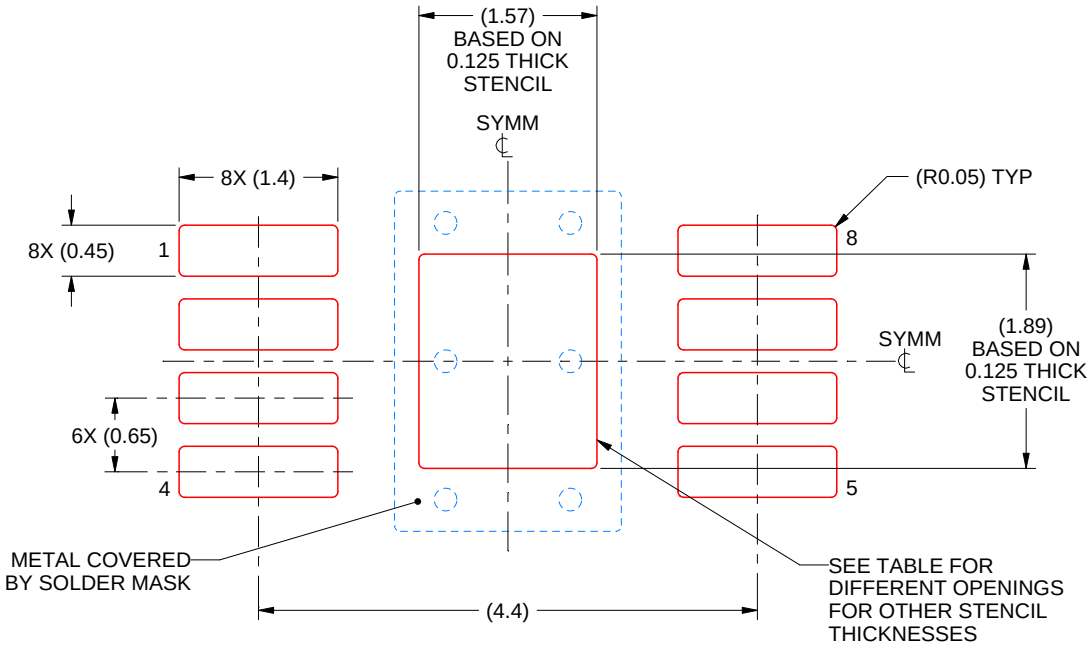


SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

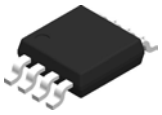
4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

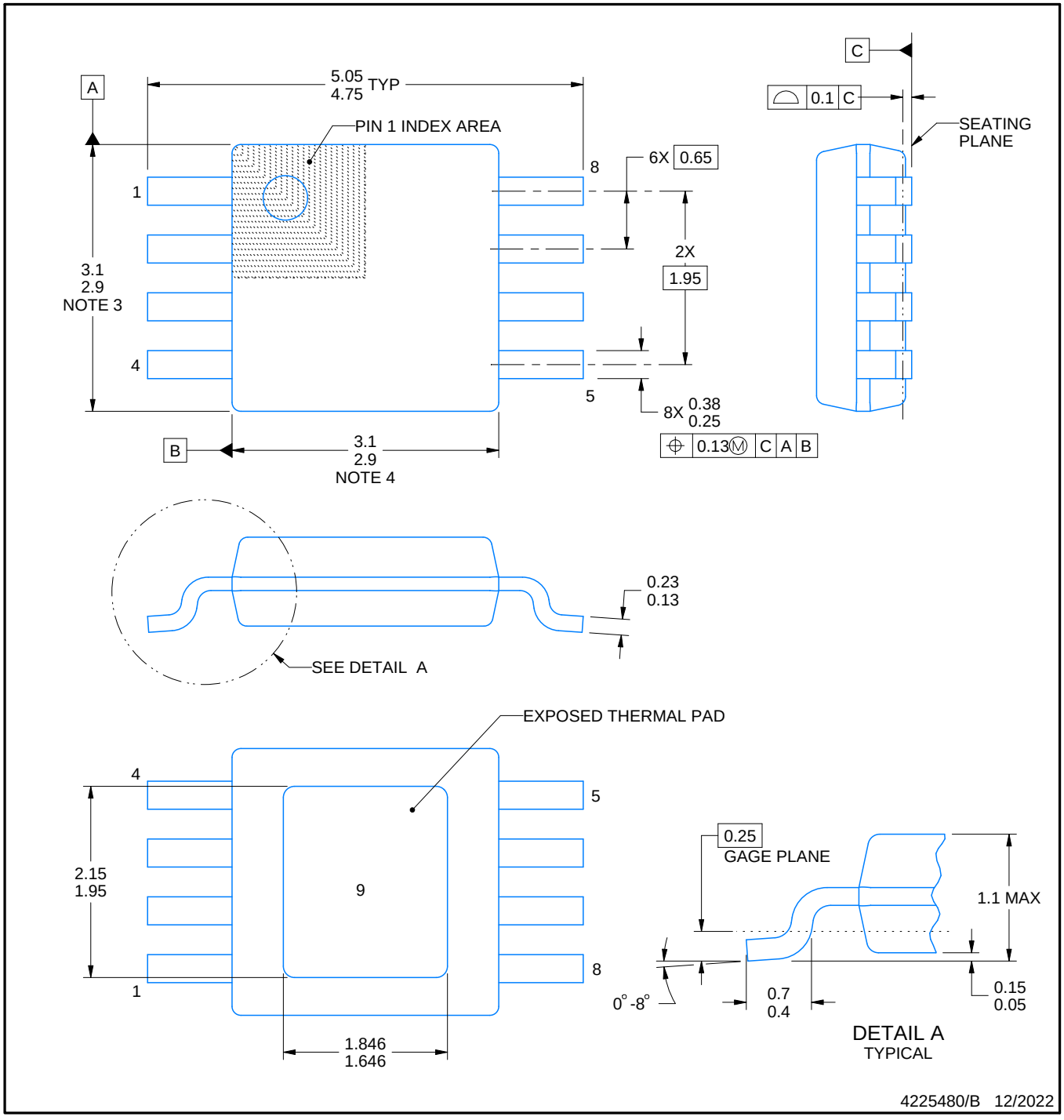
PACKAGE OUTLINE

DGN0008G



PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
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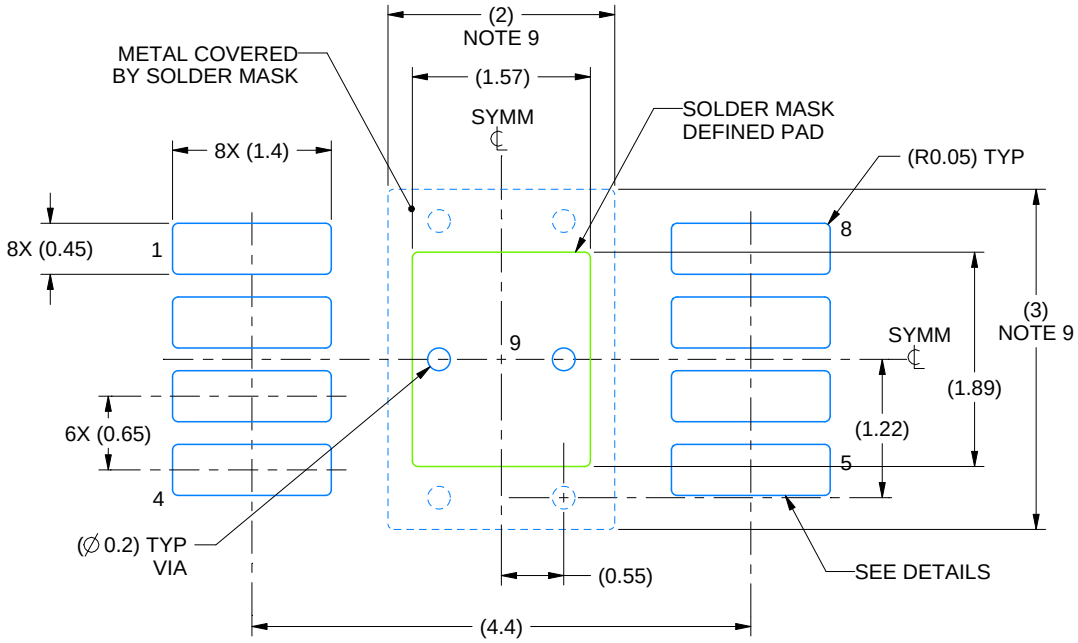
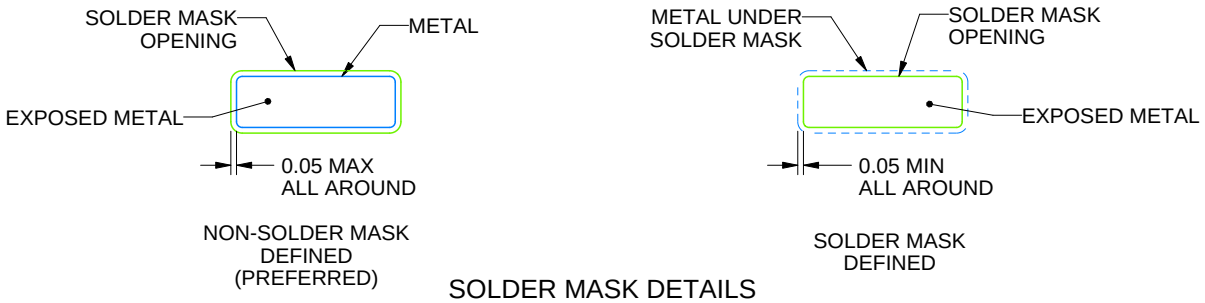
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

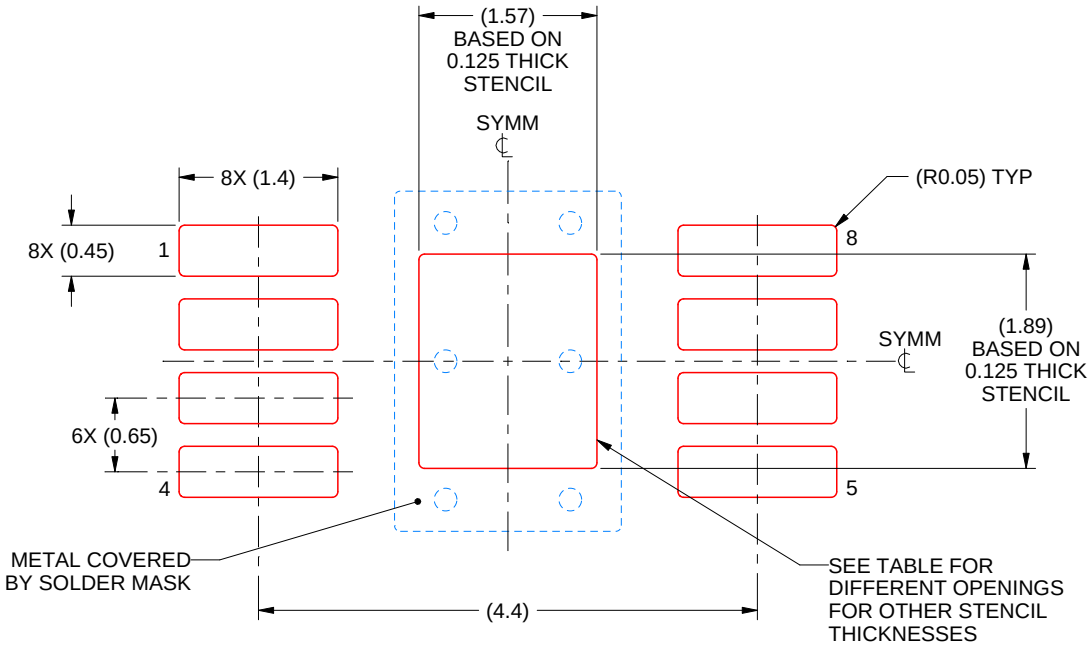


SOLDER MASK DETAILS

4225480/B 12/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



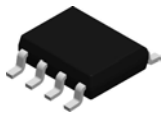
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225480/B 12/2022

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

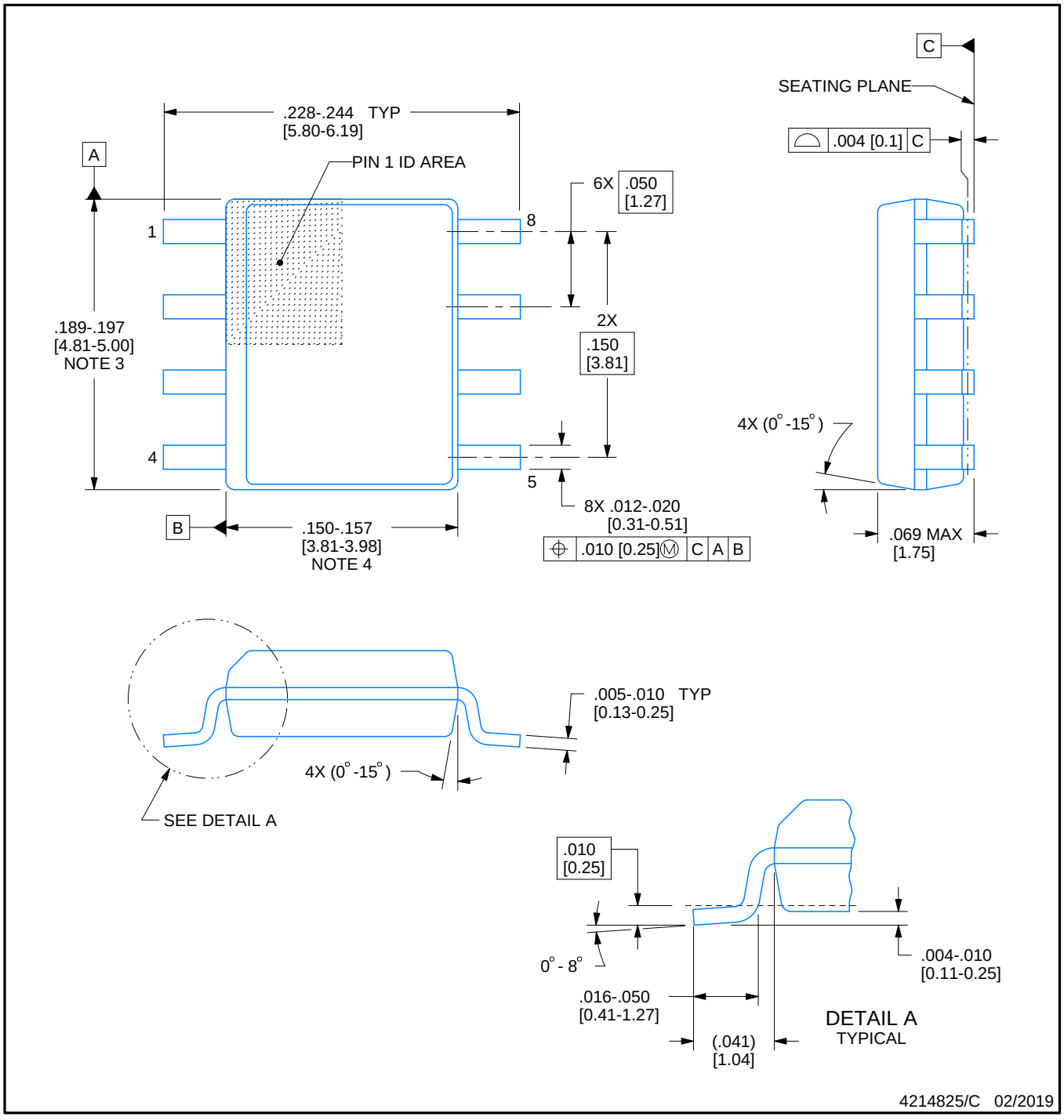


PACKAGE OUTLINE

D0008A

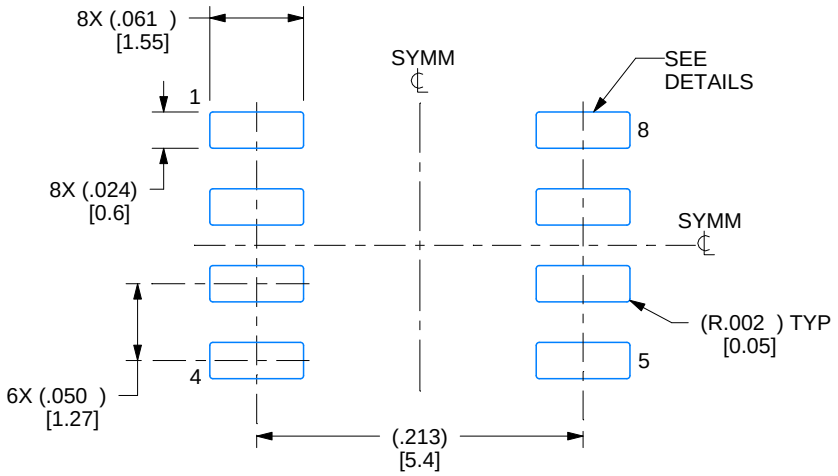
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

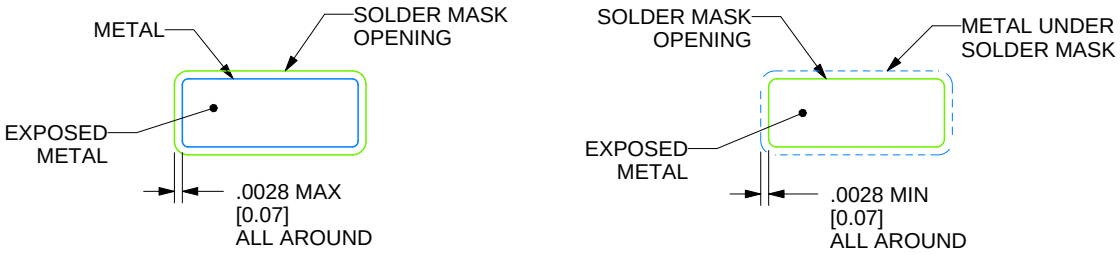


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

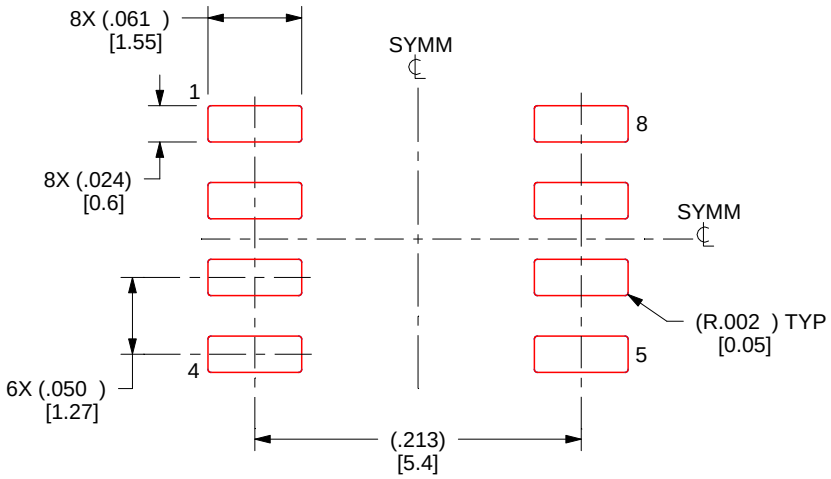
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

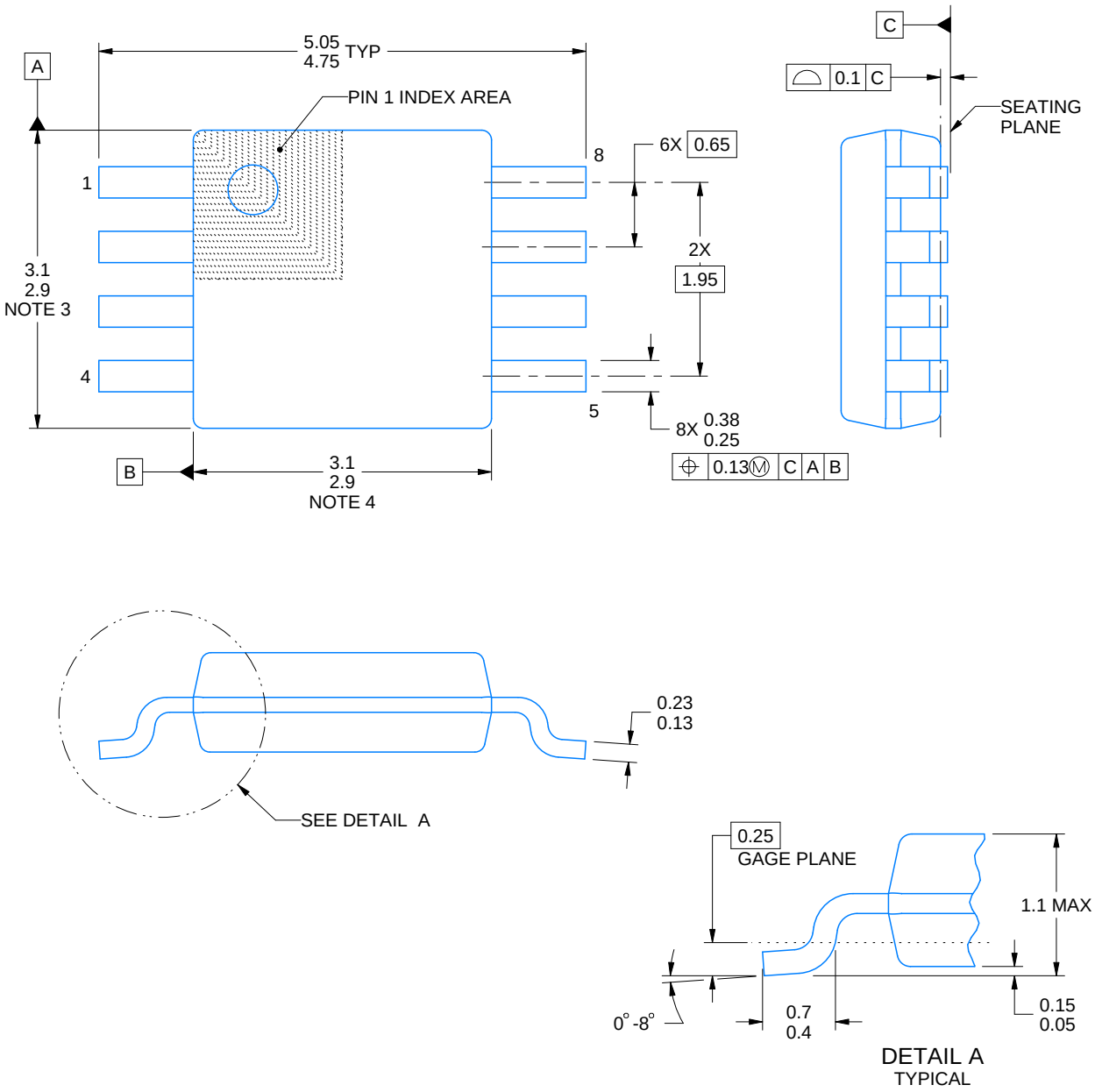
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

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2. This drawing is subject to change without notice.
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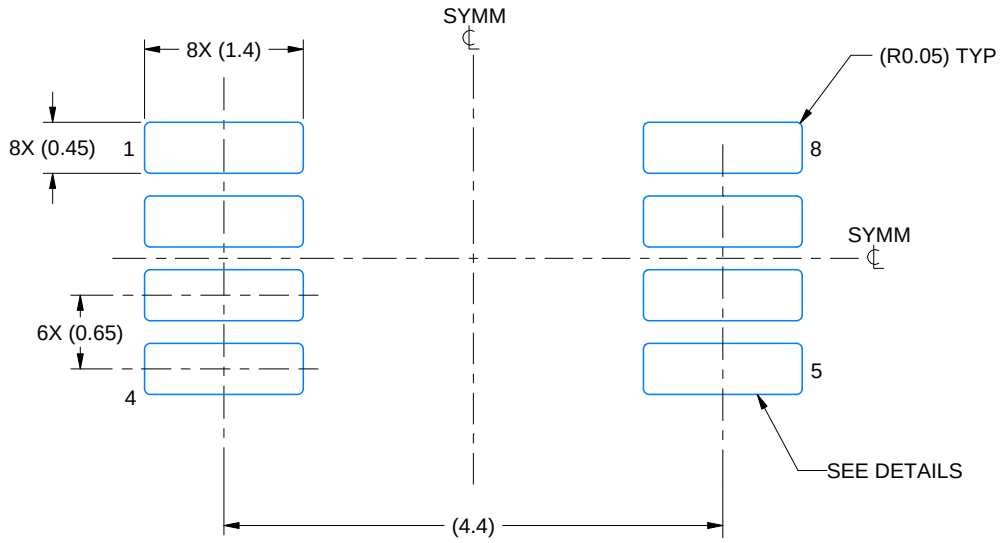
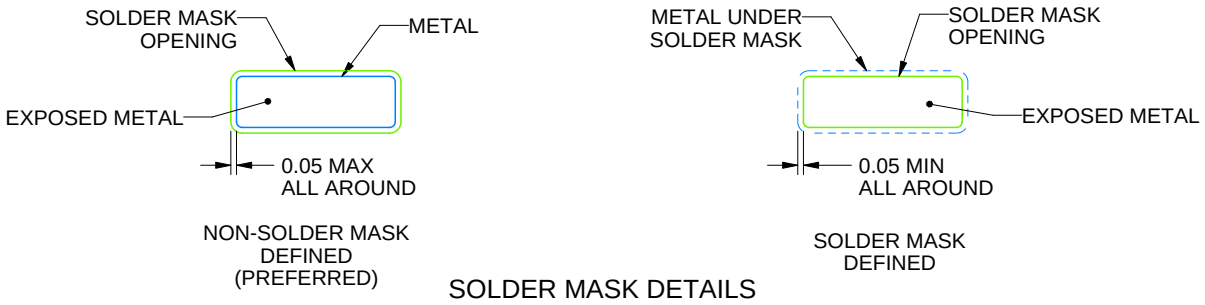
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

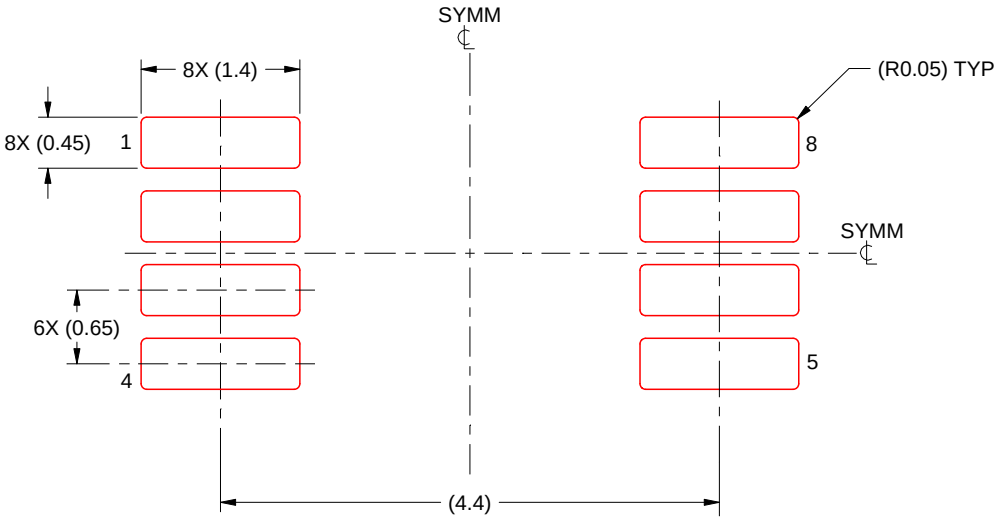


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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