PCN Number:			2024021		PCN Date: Febru			February 16, 2024		
Title:	Conversi	on to T	SMC 0.6/	0.5u	m Hybrid	l Proces	S			
Custon	ner Cont	act:	Change	Mana	agement	team	Dept:			Quality Services
Proposed 1 st Ship Date: May 16, 2024							ample juests March 17, 2024*			17, 2024*
*Samp	le reque	sts ree	c <mark>eive</mark> d af	ter I	March 17	<mark>7, 202</mark> 4	l will n	ot b	e sı	upported.
Change										
	sembly Si				Design					afer Bump Material
	embly Pr			$ \square $	Data Sh					afer Bump Process
	embly M				Part nun		ange			fer Fab Site
	chanical S				Test Site					fer Fab Material
Pac	king/Shi	pping/l	abeling		Test Pro	cess			Wa	afer Fab Process
					PCN D	Detail	5			
This cha end met	tallization for the s	fication /REB E electec Chang	is to ann Etch Back I devices J e From	proc listed	ess to th in the "I	e TSMC	n from t 0.5um Affecte	Tung d" se	gste ectio Cha	nge To
This cha end met process	ange notif tallizatior for the s 0.6um T 1D layer:	fication /REB E elected Chang SMC B PEOX	is to ann Etch Back I devices	proc listed roces EP+	ess to th d in the "l	e TSMC Product	n from t 0.5um Affecter 0.5um IMD	Tung d" se C TSI laye	gste ectio Cha MC er: I	en plug back end on.
This cha end met process	ange notif tallizatior for the s 0.6um T 1D layer:	fication /REB E elected Chang SMC B PEOX	is to ann Etch Back devices ge From ackend Pi + SOG D	proc listed roces EP+	ess to th d in the "l	e TSMC Product	n from t 0.5um Affecter 0.5um IMD +PEOX+	Tung d″ se TSI laye SOC	gste ectio MC MC er: I 6 de	en plug back end on. nge To Backend Process PEOX+SACVD-
This cha end met process	ange notif tallizatior for the s 0.6um T 1D layer:	fication /REB E elected Chang SMC B PEOX al: Ti /	is to ann Etch Back devices ge From ackend Pi + SOG D	proc listed roces EP+	ess to th d in the "l	e TSMC Product	n from t 0.5um Affecter 0.5um IMD +PEOX+	Tung d″ se TSI laye SOC	gste ectio MC MC er: I 6 de	en plug back end on. nge To Backend Process PEOX+SACVD- ep. & Etch back+PEO
This cha end met process IN Reason	ange notif tallizatior for the s 0.6um T 1D layer: Met	fication (REB E elected Chang SMC B PEOX al: Ti / nge:	is to ann Etch Back devices ge From ackend Pi + SOG D	proc listed roces EP+	ess to th d in the "l	e TSMC Product	n from t 0.5um Affecter 0.5um IMD +PEOX+	Tung d″ se TSI laye SOC	gste ectio MC MC er: I 6 de	en plug back end on. nge To Backend Process PEOX+SACVD- ep. & Etch back+PEO
This cha end met process IN Reason Quality Anticip	onge notificallization for the s 0.6um T 1D layer: Met for Cha Improver ated im	fication (REB E elected SMC B PEOX al: Ti / nge: ment.	is to ann Etch Back I devices ge From ackend Pr + SOG D AlSiCu /	proc listed roces EP+ TiN	ess to th d in the "l ss PEOX	e TSMC Product	n from t 0.5um Affecter 0.5um IMD +PEOX+ letal: Vi	Tung d″ se TSI laye SOC a Plu	gste ectio MC er: I 6 de	en plug back end on. nge To Backend Process PEOX+SACVD- ep. & Etch back+PEO
This cha end met process IN Reason Quality Anticip negativ	onge notificallization for the s 0.6um T 1D layer: Met for Cha Improver ated im	fication (REB E elected SMC B PEOX al: Ti / nge: ment.	is to ann Etch Back I devices ge From ackend Pr + SOG D AlSiCu /	proc listed roces EP+ TiN	ess to th d in the "l ss PEOX	e TSMC Product	n from t 0.5um Affecter 0.5um IMD +PEOX+ letal: Vi	Tung d″ se TSI laye SOC a Plu	gste ectio MC er: I 6 de	en plug back end on. nge To Backend Process PEOX+SACVD- ep. & Etch back+PEO iN/WCVD/AlCu /TiN
This cha end met process IN Reason Quality Anticip negativ None.	onge notif tallization for the s 0.6um T 1D layer: Met for Cha Improver ated imp /e):	fication /REB E elected SMC B PEOX al: Ti / nge: ment. pact of	is to ann Etch Back I devices ge From ackend Pr + SOG D AlSiCu /	proc isted roces EP+ TiN	ess to th d in the "I ss PEOX	e TSMC Product OX- M	n from t 0.5um Affecter 0.5ur IMD +PEOX+ letal: Vi	Tung d″ se TSI laye SOC a Plu eliat	gste ectio MC er: I G de ug T	en plug back end on. nge To Backend Process PEOX+SACVD- ep. & Etch back+PEO iN/WCVD/AlCu /TiN y (positive /
This cha end met process IN Reason Quality Anticip negativ None. Change	onge notif tallization for the s 0.6um T 1D layer: Met for Cha Improver ated imp /e):	fication /REB E elected SMC B PEOX al: Ti / nge: ment. pact of	is to ann Etch Back I devices ge From ackend Pr + SOG D AlSiCu /	proc isted roces EP+ TiN	ess to th d in the "I ss PEOX	e TSMC Product OX- M	n from t 0.5um Affecter 0.5ur IMD +PEOX+ letal: Vi	Tung d″ se TSI laye SOC a Plu eliat	gste ectio MC er: I G de ug T	en plug back end on. nge To Backend Process PEOX+SACVD- ep. & Etch back+PEO iN/WCVD/AlCu /TiN y (positive /
This cha end met process IN Reason Quality Anticip negativ None. Change None.	onge notif tallization for the s 0.6um T 1D layer: Met for Cha Improver ated imp /e):	fication /REB E elected SMC B PEOX al: Ti / nge: ment. pact of duct in	is to ann Etch Back I devices ge From ackend Pr + SOG D AlSiCu /	proc isted roces EP+ TiN	ess to th d in the "I ss PEOX	e TSMC Product OX- M	n from t 0.5um Affecter 0.5ur IMD +PEOX+ letal: Vi	Tung d″ se TSI laye SOC a Plu eliat	gste ectio MC er: I G de ug T	en plug back end on. nge To Backend Process PEOX+SACVD- ep. & Etch back+PEO iN/WCVD/AlCu /TiN y (positive /
This cha end met process IN Reason Quality Anticip negativ None. Change None. Produc	onge notif tallization for the s 0.6um T 4D layer: Met for Cha Improver ated imp ye):	fication /REB E elected SMC B PEOX al: Ti / nge: ment. pact of duct id ed:	is to ann Etch Back I devices ge From ackend Pr + SOG D AlSiCu /	proc isted roces EP+ TiN m, F	ess to th d in the "I ss PEOX Function, resultin	e TSMC Product OX- M , Qualit	n from t 0.5um Affecter 0.5ur IMD +PEOX+ letal: Vi	Tung d″ se TSI laye SOC a Plu eliat	gste ectio MC er: I G de ug T	en plug back end on. nge To Backend Process PEOX+SACVD- ep. & Etch back+PEO iN/WCVD/AlCu /TiN y (positive /

Туре	#	Test Spec	Min Lot Qty	SS/ Lot	Test Name	Condition	Duration	Qual Device: OPA2348AQDRQ1	QBS Package Reference: UCC28C56HQDRQ1	QBS Process Reference: OPAS56AQDBVRQ1	QBS Package Reference: TLV2314QDRQ1	QBS Package Reference: SN65HVD1781AQDRQ1	QBS Product Reference: OPA348AQDRQ1	QBS Package Reference: SN74AHCT244QDWRQ1
Test Group	Test Group A - Accelerated Environment Stress Tests													
PC	A1	JEDEC J- STD-020 JESD22- A113	3	77	Preconditioning	MSL1 260C		1/Pass	1/Pass	-	1/Pass	3/Pass	-	3/Pass
PC	A1	JEDEC J- STD-020 JESD22- A113	3	77	Preconditioning	MSL2 260C	•	-		3/Pass	-		-	
HAST	A2	JEDEC JESD22- A110	3	77	Biased HAST	130C/85%RH	96 Hours	1/77/0	1/77/0	3/77/0	1/77/0	3/231/0	1/77/0	

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Туре	#	Test Spec	Min Lot Qty	SS/ Lot	Test Name	Condition	Duration	Qual Device: OPA2348AQDRQ1	QBS Package Reference: UCC28C56HQDRQ1	QBS Process Reference: OPA356AQDBVRQ1	QBS Package Reference: TLV2314QDRQ1	QBS Package Reference: SN65HVD1781AQDRQ1	QBS Product Reference: OPA348AQDRQ1	QBS Package Reference: SN74AHCT244QDWRQ1
AC/UHAST	A3	JEDEC JESD22- A102/JEDEC JESD22- A118	3	77	Autoclave	121C/15psig	96 Hours	-	1/77/0	3/77/0	1/77/0	3/231/0	-	3/231/0
AC/UHAST	A3	JEDEC JESD22- A102/JEDEC JESD22- A118	3	77	Unbiased HAST	130C/85%RH	96 Hours	1/77/0		-		-	-	
тс	A4	JEDEC JESD22- A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	1/77/0	1/77/0	3/77/0	1/77/0	3/231/0	-	3/231/0
TC-BP	Α4	MIL-STD883 Method 2011	1	5	Post Temp Cycle Bond Pull	-		1/5/0	1/5/0	1/5/0	1/5/0	1/50/0	1/30/0	3/15/0
HTSL	A6	JEDEC JESD22- A103	1	45	High Temperature Storage Life	150C	1000 Hours		4/308/0	-	-	-	-	
HTSL	A6	JEDEC JESD22- A103	1	45	High Temperature Storage Life	175C	500 Hours	1/45/0	-	1/45/0	1/45/0	1/45/0	-	3/135/0
Test Group B - Accelerated Lifetime Simulation Tests														
HTOL	81	JEDEC JESD22- A108	3	77	Life Test	125C	1000 Hours	-	1/77/0	3/77/0	1/77/0	2/154/0	-	
HTOL	81	JEDEC JESD22- A108	3	77	Life Test	140C	480 Hours		-	-		1/77/0	-	
HTOL	81	JEDEC JESD22- A108	3	77	Life Test	150C	300 Hours	1/77/0	-	-	-	-	-	
ELFR	82	AEC Q100- 008	3	800	Early Life Failure Rate	125C	48 Hours	-		3/800/0				
Test Group (C - Pack	age Assembly I	Integrity	Tests										
WBS	C1	AEC Q100- 001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cplo>1.67	Wires	1/30/0	3/90/0	1/30/0	1/30/0	3/228/0	-	3/90/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	3/90/0	1/30/0	1/30/0	3/228/0	-	3/90/0
SD	сз	JEDEC J- STD-002	1	15	PB Solderability	>95% Lead Coverage		•	1/15/0	-	1/15/0	•	-	3/35/0
SD	C3	JEDEC J- STD-002	1	15	PB-Free Solderability	>95% Lead Coverage			1/15/0	-	1/15/0		-	3/45/0
PD	C4	JEDEC JESD22- B100 and B108	3	10	Physical Dimensions	Cpk>1.67		1/10/0	3/30/0	1/10/0	3/30/0	3/30/0	-	3/30/0

Туре	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: OPA2348AQDRQ1	QBS Package Reference: UCC28C56HQDRQ1	QBS Process Reference: OPA356AQDBVRQ1	QBS Package Reference: TLV2S14QDRQ1	QBS Package Reference: SN65HVD1781AQDRQ1	QBS Product Reference: OPA348AQDRQ1	QBS Package Reference: SN74AHCT244QDWRQ1
ЕМ	D1	JESD61			Electromigration		•	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDDB	D2	JESD35	-		Time Dependent Dielectric Breakdown		-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
нсі	D3	JESD60 & 28			Hot Carrier Injection			Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
вті	D4	-			Bias Temperature Instability		-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-			Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group	p E - Elec	trical Verificatio	n Tests											
ESD	E2	AEC Q100- 002	1	3	ESD HBM		16000 Volts	-		-	-	1/3/0	-	-
ESD	E2	AEC Q100- 002	1	з	ESD HBM	•	2000 Volts	1/3/0	•	1/3/0	1/3/0		1/3/0	
ESD	E2	AEC Q100- 002	1	3	ESD HBM	•	2500 Volts	-	1/3/0	-	•	•	-	
	E2 E2		1	3 3	ESD HBM ESD HBM				1/3/0	- -		- 1/3/0	•	
ESD		002 AEC Q100-	-	-		- -	Volts 4000	• •	1/3/0 •	- - -	- -	1/3/0 1/3/0	• •	• •
ESD ESD ESD ESD	E2	002 AEC Q100- 002 AEC Q100-	1	3	ESD HBM	- - -	Volts 4000 Volts 1500	• • •	1/3/0 - 1/3/0	• •	• • •		- - -	•
ESD ESD	E2 E3	002 AEC Q100- 002 AEC Q100- 011 AEC Q100-	1	3	ESD HBM ESD CDM	• • •	Volts 4000 Volts 1500 Volts 2000		•	· · · · · · · · · · · · · · · · · · ·	- - - 1/3/0		- - - 1/3/0	• • •
ESD ESD ESD	E2 E3 E3	002 AEC Q100- 002 AEC Q100- 011 AEC Q100- 011 AEC Q100-	1	3 3 3	ESD HBM ESD CDM ESD CDM		Volts 4000 Volts 1500 Volts 2000 Volts 500	- - - 1/3/0 1/77/0	•	1/3/0 1/6/0	- - - 1/3/0 2/12/0		1/3/0	• • • •

al Tests

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
The following are equivalent HTOL options based on an activation energy of 0.7eV i 1250/LK hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
The following are equivalent HTSL option based on an activation energy of 0.7eV i 1350/LK hours, and 170C/240 Hours, and 155C/240 Hours
The following are equivalent HTSL option based on an activation energy of 0.7eV i 1350/LK hours, and 170C/240 Hours, and 155C/240 Hours
The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -55C/150C/500 Cycles

Ambient Operating Temperature by Automotive Grade Level:

- Grade 0 (or E): -40C to +150C
- Grade 1 (or Q): -40C to +125C
- Grade 2 (or T): -40C to +105C
- Grade 3 (or I) : -40C to +85C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

- Room/Hot/Cold : HTOL, ED
- Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
- Room : AC/uHAST

Quality and Environmental data is available at TI's external Web site: http://www.ti.com/

TI Qualification ID: R-CHG-2301-048

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Туре	#	Test Name	Condition	Duration	Qual Device: INA331IDGKT	QBS Reference: <u>OPA356AQDBVRQ1</u>	QBS Reference: OPA348AIDCKR
HAST	A2	Biased HAST	130C/85%RH	96 Hours	-	3/231/0	-
UHAST	A3	Autoclave	121C/15psig	96 Hours	-	3/230/0	1/77/0
тс	A4	Temperature Cycle	-65C/150C	500 Cycles	-	3/230/0	1/77/0
HTSL	A6	High Temperature Storage Life	175C	500 Hours	-	1/45/0	-
HTOL	B1	Life Test	125C	1000 Hours	-	3/231/0	-
ELFR	B2	Early Life Failure Rate	125C	48 Hours	-	3/2400/0	-
ESD	E2	ESD CDM	-	500 Volts	1/3/0	1/3/0	1/3/0
ESD	E2	ESD HBM	-	2000 Volts	1/3/0	1/3/0	1/3/0
LU	E4	Latch-Up	Per JESD78	-	1/3/0	1/6/0	1/6/0
CHAR	E5	Electrical Characterization	Per Datasheet Parameters	-	1/30/0	3/90/0	1/30/0

• QBS: Qual By Similarity

Qual Device INA331IDGKT is qualified at MSL2 260C

• Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours

The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Quality and Environmental data is available at TI's external Web site: http://www.ti.com/

TI Qualification ID: R-CHG-2210-015

For questions regarding this notice, e-mails can be sent to the Change Management team or your local Field Sales Representative.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (<u>www.ti.com/legal/termsofsale.html</u>) or other applicable terms available either on <u>ti.com</u> or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.