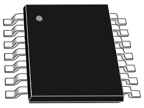
TSB621, TSB622, TSB624

Datasheet

Low power, 1.7 MHz, rail-to-rail output, 36 V operational amplifier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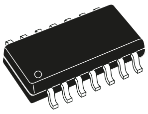
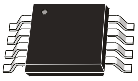
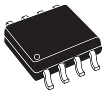

SO14


MiniSO8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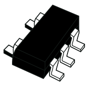
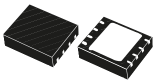

SOT23-5


DFN8 (3 x 3 mm)

Maturity status link
TSB621, TSB622, TSB624

Related products	
TSB611, TSB612	For lower power consumption
TSB571, TSB572, TSB514	For higher speed and rail-to-rail inputs
TSB711, TSB712	For a higher precision and speed

Features

- Low offset voltage: 1 mV max. @ 25 °C
- Low current consumption: 375 µA max. / operator @ 36 V
- Wide supply voltage: 2.7 to 36 V
- Gain bandwidth product: 1.7 MHz
- Unity gain stable
- Rail-to-rail output
- Input common mode voltage incudes ground
- High ESD tolerance: 4 kV HBM
- EMI hardened
- Extended temperature range: -40 to 125 °C
- Automotive qualification

Applications

- Industrial
- Power supplies
- Automotive

Description

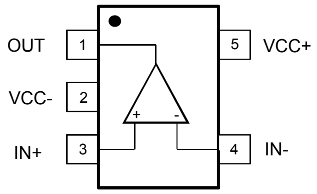
The TSB621, TSB622, TSB624 are general purpose operational amplifiers featuring an extended supply voltage operating range and rail-to-rail output. They also offer an excellent speed/power consumption ratio with 1.7 MHz gain bandwidth product while consuming less than 375 µA per operator at 36 V supply voltage.

The TSB621, TSB622, TSB624 operate over a wide temperature range from -40 °C to 125 °C making these devices ideal for industrial and automotive applications with the associated qualification.

Thanks to the small package size, the TSB621, TSB622, TSB624 can be used in applications where space on the board is limited. It can thus reduce the overall cost of the PCB.

1 Pin connections

Figure 1. **TSB621 pin connections (top view)**

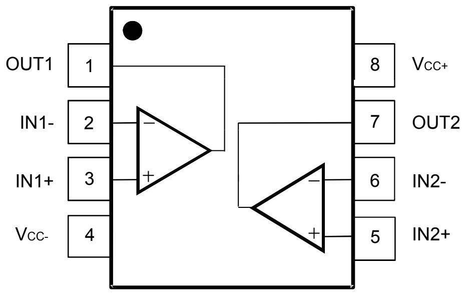


SOT23-5

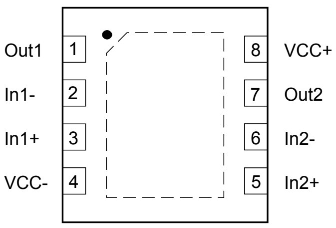
Table 1. **TSB621 pin description**

Pin n°	Pin name	Description
1	OUT1	Output
2	VCC -	Negative supply voltage
3	IN +	Positive input voltage
4	IN -	Negative input voltage
5	VCC	Positive supply voltage

Figure 2. **TSB622 pin connections (top view)**



SO8 - MiniSO8



DFN8 (3 x 3)[1]

[1] Exposed pad can be left floating or connected to ground.

Table 2. **TSB622 pin description**

Pin n°	Pin name	Description
1	OUT1	Output
2	IN1 -	Negative input voltage
3	IN1 +	Positive input voltage
4	VCC -	Negative supply voltage
5	IN2 +	Positive input voltage
6	IN2 -	Negative input voltage
7	OUT2	Output
8	VCC +	Positive supply voltage

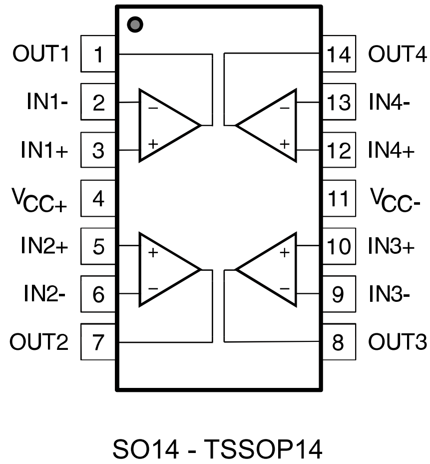


Figure 3. **TSB624 pin connections (top view)**

Table 3. **TSB624 pin description**

Pin n°	Pin name	Description
1	OUT1	Output
2	IN1 -	Negative input voltage
3	IN1 +	Positive input voltage
4	VCC +	Positive supply voltage
5	IN2 +	Positive input voltage
6	IN2 -	Negative input voltage
7	OUT2	Output
8	OUT3	Output
9	IN3 -	Negative input voltage
10	IN3 +	Positive input voltage
11	VCC -	Negative supply voltage
12	IN4 +	Positive input voltage
13	IN4 -	Negative input voltage
14	OUT4	Output

2 Absolute maximum ratings and operating conditions

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{cc}	Supply voltage [1]	40	V
V_{id}	Differential input voltage [2]	± V_{cc}	V
V_{in}	Input voltage	(V_{cc-}) -0.2 to (V_{cc+}) +0.2	V
I_{in}	Input current [3]	10	mA
T_{stg}	Storage temperature	-65 to 150	°C
T_j	Junction temperature	150	°C
R_{th-ja}	Thermal resistance junction to ambient [4] [5] SO8 MiniSO8 DFN8 3x3 WF SOT23-5 SO14 TSSOP14	 125 190 40 250 105 100	°C/W
ESD	Human Body Model (HBM TSB621, TSB622) [6] Human Body Model (HBM TSB624) [6]	4000 3000	V
	Charged Device Model (CDM) [7]	1500	

1. *All voltage values, except differential voltage, are with respect to network ground terminal.*
2. *The differential voltage is the non-inverting input terminal with respect to the inverting input terminal.*
3. *Input current must be limited by a resistor in series with the inputs.*
4. *R_{th} are typical values.*
5. *Short-circuits can cause excessive heating and destructive dissipation.*
6. *According to JEDEC standard JESD22-A114F.*
7. *According to ANSI/ESD STM5.3.1.*

Table 5. Operating conditions

Symbol	Parameter	Value	Unit
V_{cc}	Supply voltage	2.7 to 36	V
V_{icm}	Common mode voltage on input pins	(V_{cc-}) -0.1 to (V_{cc+}) -1	V
T	Operating free-air temperature range	-40 to 125	°C

3 Electrical characteristics

Table 6. Electrical characteristics V_{CC+} = 2.7 V, V_{cc-} = 0 V, V_{icm} = V_{CC}/2, T = 25 °C, R_L = 10 kΩ connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
		DC performance				
V_{IO}	Input offset voltage	T = 25 °C	-1		1	mV
		Tmin < T < Tmax	-1.6		1.6	
$\|\Delta V_{IO}/\Delta T\|$	Input offset voltage drift	Tmin < T < Tmax		2		μV/°C
I_{IB}	Input bias current	T = 25 °C		15	30	nA
		Tmin < T < Tmax			45	
I_{IO}	Input offset current	T = 25 °C		3	10	
		Tmin < T < Tmax			15	
CMR	Common mode rejection ratio: 20 log ($\Delta V_{icm}/\Delta V_{io}$)	V_{icm} = - 0.1 to V_{CC} -1 V, V_{OUT} = V_{CC}/2	90	115		dB
		Tmin < T < Tmax	85			
A_{VD}	Large signal voltage gain	V_{OUT} = 0.5 V to (V_{CC} -0.5 V)	90	105		dB
		Tmin < T < Tmax	82			
V_{OH}	High-level output voltage, V_{OH} = V_{CC} - V_{OUT}	T = 25 °C		35	46	mV
		Tmin < T < Tmax			55	
V_{OL}	Low-level output voltage	T = 25 °C		50	60	
		Tmin < T < Tmax			75	
I_{OUT}	I_{sink}	V_{OUT} = V_{CC}	20	27		mA
		Tmin < T < Tmax	10			
	I_{source}	V_{OUT} = 0 V	20	28		
		Tmin < T < Tmax	8			
I_{CC}	Supply current (per channel)	No load, V_{OUT} = V_{CC}/2		280	330	μA
		Tmin < T < Tmax			400	
		AC performance				
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	1	1.45		MHz
		Tmin < T < Tmax	0.7			
Φ_m	Phase margin	R_L = 10 kΩ, C_L = 100 pF		45		degrees
G_m	Gain margin			18		dB
SR	Slew rate	T = 25 °C	0.30	0.53		V/μs
		Tmin < T < Tmax	0.20			
E_N	Equivalent input noise voltage	f = 1 kHz		30		nV/√Hz
THD+N	Total harmonic distortion + noise	f_{in} = 1 kHz, Gain = 1, R_L = 100 kΩ, V_{icm} = (V_{cc} -1 V) / 2, BW = 22 kHz, V_{OUT} = 1 Vpp		0.005		%
C_S	Channel separation	f = 1 kHz		120		dB
t_{rec}	Overload recovery time			2		μs

Table 7. Electrical characteristics V_{CC+} = 12 V, V_{CC-} = 0 V, V_{icm} = V_{CC}/2, T = 25 °C, R_L = 10 kΩ connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
		DC performance				
V_{IO}	Input offset voltage	T = 25 °C	-1		1	mV
		Tmin < T < Tmax	-1.6		1.6	
$\|\Delta V_{IO}/\Delta T\|$	Input offset voltage drift	Tmin < T < Tmax		2		µV/°C
I_{IB}	Input bias current	T = 25 °C		15	30	nA
		Tmin < T < Tmax			45	
I_{IO}	Input offset current	T = 25 °C		3	10	
		Tmin < T < Tmax			15	
CMR	Common mode rejection ratio: 20 log ($\Delta V_{icm}/\Delta V_{io}$)	V_{icm} = - 0.1 to V_{CC} -1 V, V_{OUT} = V_{CC}/2	100	130		dB
		Tmin < T < Tmax	95			
A_{VD}	Large signal voltage gain	V_{OUT} = 0.5 V to (V_{CC} -0.5 V)	98	115		dB
		Tmin < T < Tmax	90			
V_{OH}	High-level output voltage, V_{OH} = V_{CC} - V_{OUT}	T = 25 °C		68	80	mV
		Tmin < T < Tmax			95	
V_{OL}	Low-level output voltage	T = 25 °C		86	100	
		Tmin < T < Tmax			125	
I_{OUT}	I_{sink}	V_{OUT} = V_{CC}	25	35		mA
		Tmin < T < Tmax	10			
	I_{source}	V_{OUT} = 0 V	30	37		
		Tmin < T < Tmax	15			
I_{CC}	Supply current (per channel)	No load, V_{OUT} = V_{CC}/2		295	345	µA
		Tmin < T < Tmax			420	
		AC performance				
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	1.1	1.55		MHz
		Tmin < T < Tmax	0.8			
Φ_m	Phase margin	R_L = 10 kΩ, C_L = 100 pF		45		degrees
G_m	Gain margin			18		dB
SR	Slew rate	T = 25 °C	0.35	0.58		V/µs
		Tmin < T < Tmax	0.20			
E_N	Equivalent input noise voltage	f = 1 kHz		30		nV/√Hz
THD+N	Total harmonic distortion + noise	f_{in} = 1 kHz, Gain = 1, R_L = 100 kΩ, V_{icm} = (V_{CC} -1 V) / 2, BW = 22 kHz, V_{OUT} = 1 Vpp		0.005		%
C_S	Channel separation	f = 1 kHz		120		dB
t_{rec}	Overload recovery time			2		µs

Table 8. **Electrical characteristics V_{CC+} = 36 V, V_{CC-} = 0 V, V_{icm} = V_{CC}/2, T = 25 °C, R_L = 10 kΩ connected to Vcc/2 (unless otherwise specified)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{IO}	Input offset voltage	T = 25 °C	-1		1	mV
		Tmin < T < Tmax	-1.6		1.6	
$\|\Delta V_{IO}/\Delta T\|$	Input offset voltage drift	Tmin < T < Tmax		2		µV/°C
I_{IB}	Input bias current	T = 25 °C		15	30	nA
		Tmin < T < Tmax			45	
I_{IO}	Input offset current	T = 25 °C		3	10	
		Tmin < T < Tmax			15	
CMR	Common mode rejection ratio: 20 log ($\Delta V_{icm}/\Delta V_{io}$)	V_{icm} = -0.1 to V_{CC} -1 V, V_{OUT} = V_{CC}/2	105	135		dB
		Tmin < T < Tmax	100			
SVR	Supply voltage rejection ratio: 20 log ($\Delta V_{CC}/\Delta V_{io}$)	V_{CC} = 4.5 to 36 V, V_{icm} = 0 V	100	124		dB
		Tmin < T < Tmax	95			
A_{VD}	Large signal voltage gain	V_{OUT} = 0.5 V to (V_{CC} -0.5 V)	105	120		dB
		Tmin < T < Tmax	100			
V_{OH}	High-level output voltage, V_{OH} = V_{CC} - V_{OUT}	T = 25 °C		110	140	mV
		Tmin < T < Tmax			180	
V_{OL}	Low-level output voltage	T = 25 °C		125	150	
		Tmin < T < Tmax			195	
I_{OUT}	I_{sink}	V_{OUT} = V_{CC}	35	45		mA
		Tmin < T < Tmax	15			
	I_{source}	V_{OUT} = 0 V	35	45		
		Tmin < T < Tmax	25			
I_{CC}	Supply current (per channel)	No load, V_{OUT} = V_{CC}/2		310	375	µA
		Tmin < T < Tmax			420	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	1.2	1.7		MHz
		Tmin < T < Tmax	0.95			
Φ_m	Phase margin	R_L = 10 kΩ, C_L = 100 pF		45		degrees
G_m	Gain margin			18		dB
SR	Slew rate	T = 25 °C	0.35	0.60		V/µs
		Tmin < T < Tmax	0.25			
E_N	Equivalent input noise voltage	f = 1 kHz		25		nV/√Hz
THD+N	Total harmonic distortion + noise	f_{in} = 1 kHz, Gain = 1, R_L = 100 kΩ, V_{icm} = (V_{CC} - 1 V) / 2, BW = 22 kHz, V_{OUT} = 1 Vpp		0.005		%
C_S	Channel separation	f = 1 kHz		120		dB
t_{rec}	Overload recovery time			2		µs

4 Typical performance characteristics

Figure 4. Supply current vs. supply voltage

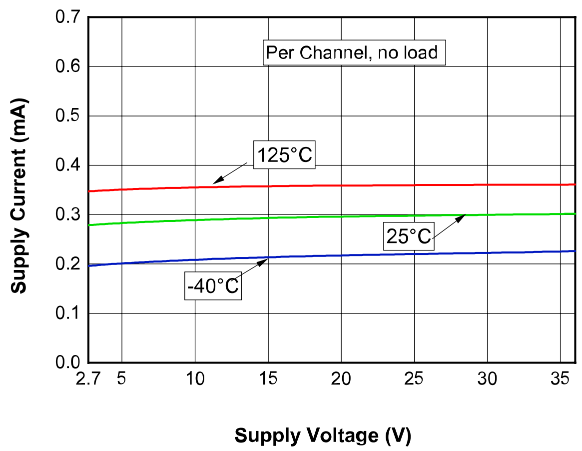


Figure 5. Input offset voltage distribution at V_{CC} = 2.7 V

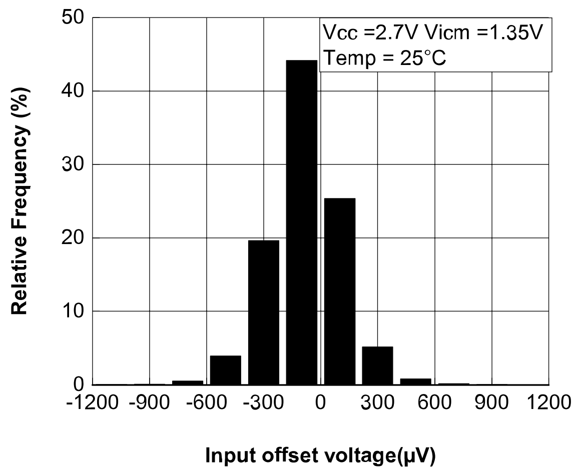


Figure 6. Input offset voltage distribution at V_{CC} = 12 V

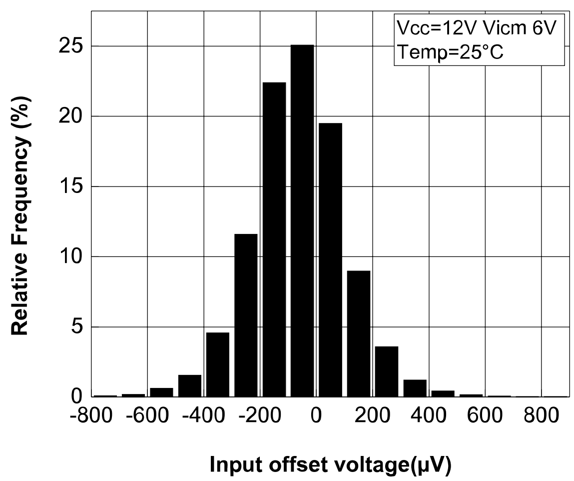
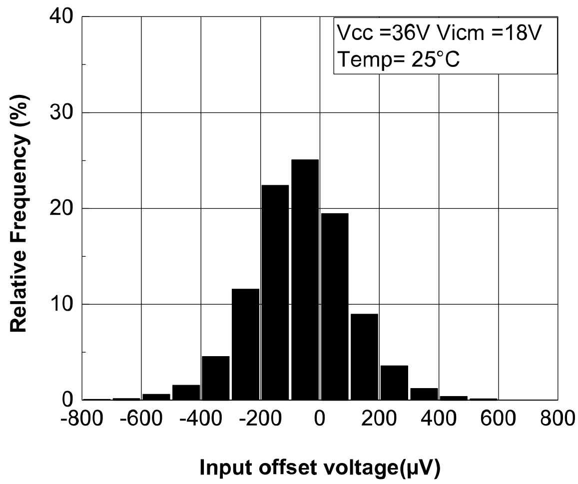


Figure 7. Input offset voltage distribution at V_{CC} = 36 V



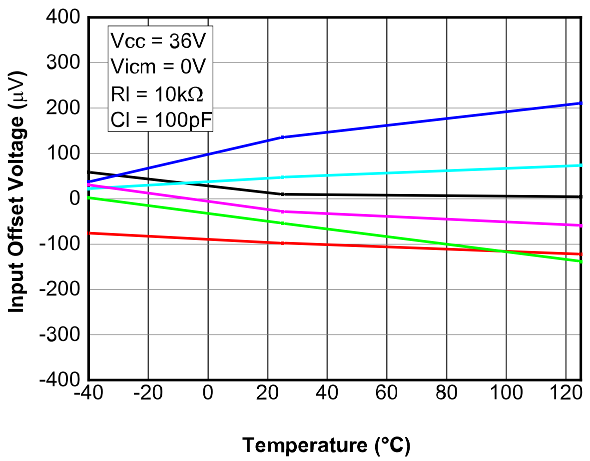


Figure 8. Input offset voltage vs. temperature at V_{CC} = 36 V

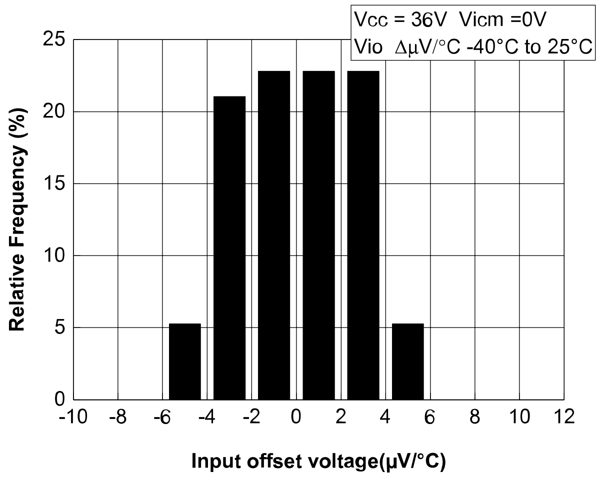


Figure 9. Input offset voltage temperature variation distribution at V_{CC} = 36 V

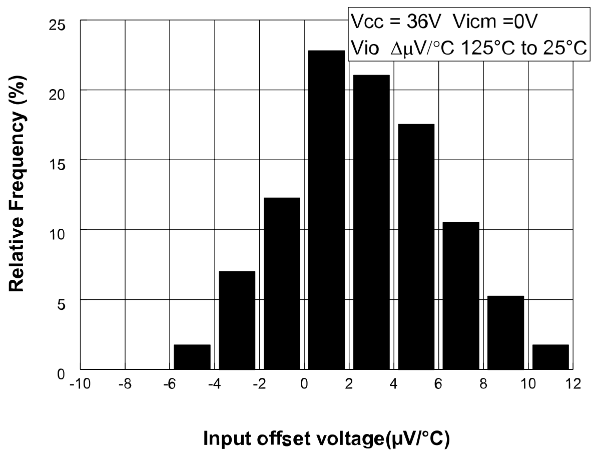


Figure 10. Input offset voltage temperature variation distribution at V_{CC} = 36 V

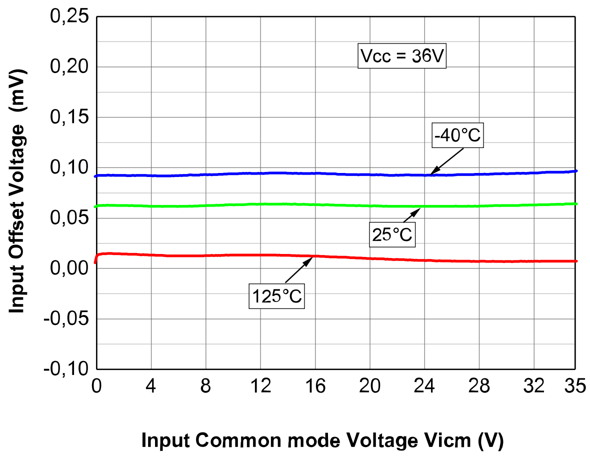


Figure 11. Input offset voltage vs. common-mode voltage at V_{CC} = 36 V

Figure 12. Common-mode reject. ratio CMR at V_{CC} = 5 V

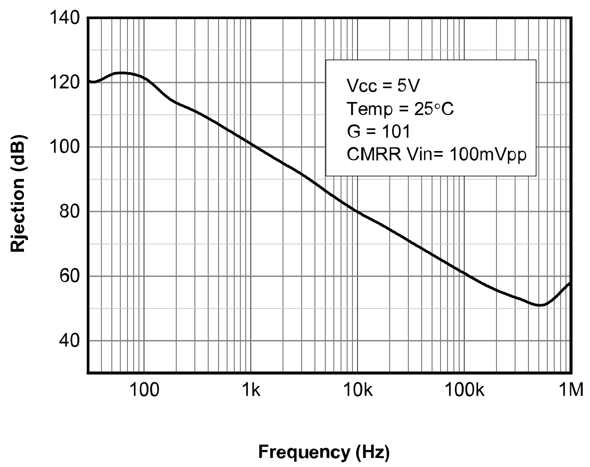


Figure 13. Supply voltage rejection ratio SVR at V_{CC} = 5 V

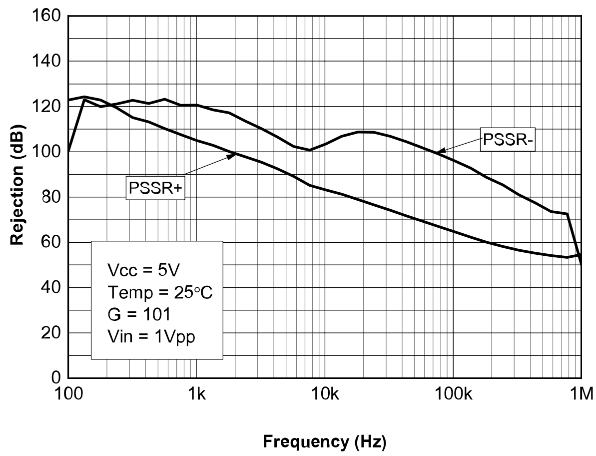


Figure 14. Input bias current vs. temperature

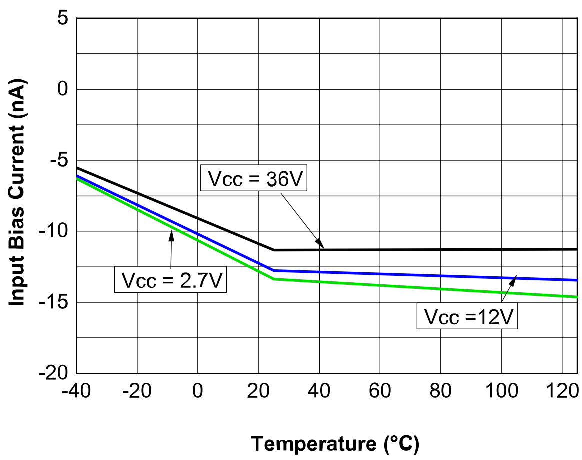


Figure 15. Bode diagram at V_{CC} = 2.7 V

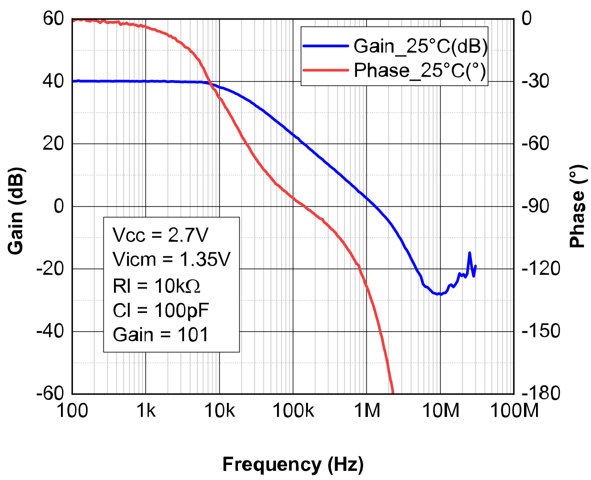


Figure 16. Bode diagram at V_{CC} = 12 V

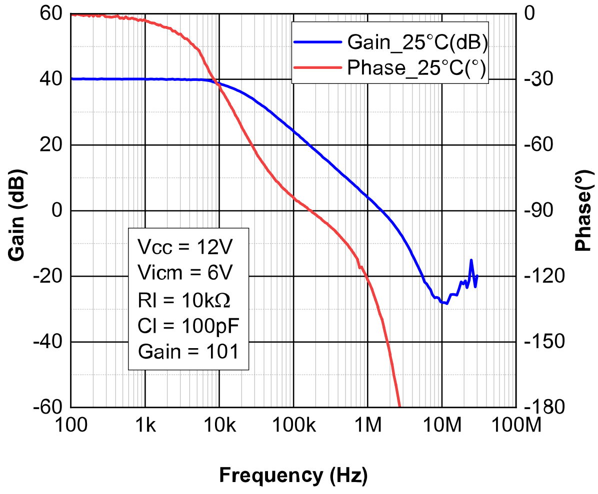


Figure 17. Bode diagram at V_{CC} = 36 V

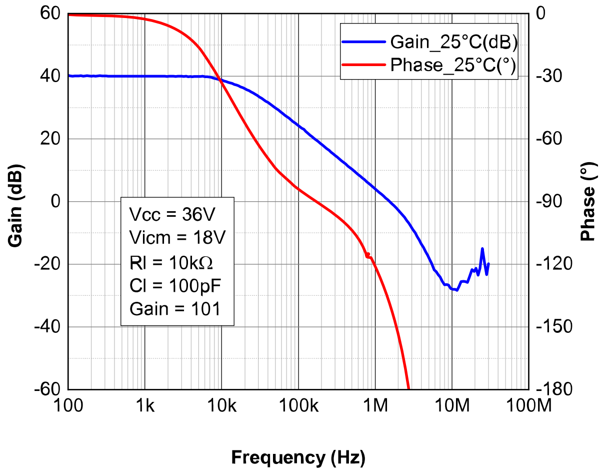


Figure 18. Overshoot vs. capacitive load at V_{CC} = 36 V

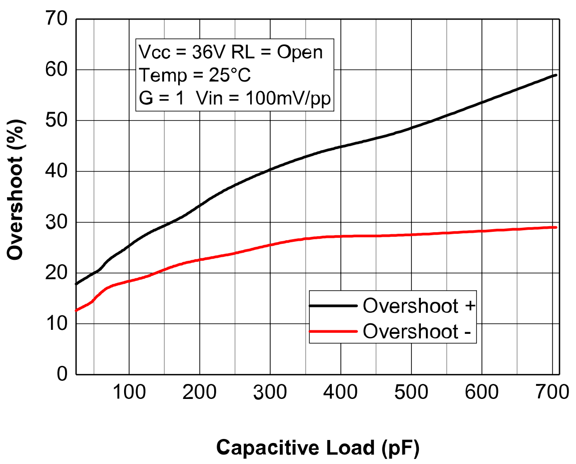


Figure 19. Phase margin vs. capacitive load at V_{CC} = 2.7 V

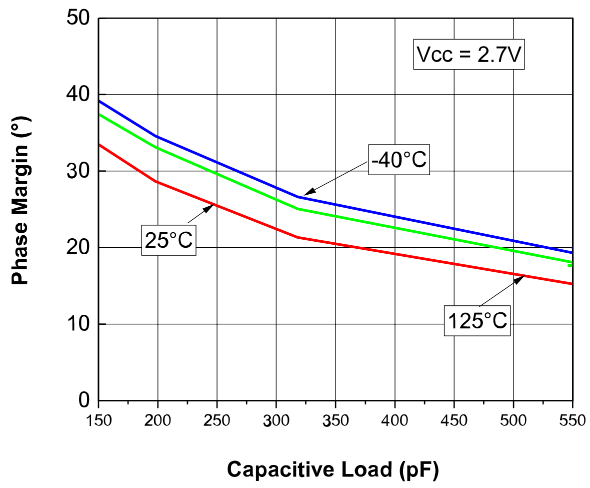


Figure 20. Phase margin vs. capacitive load at V_{CC} = 12 V

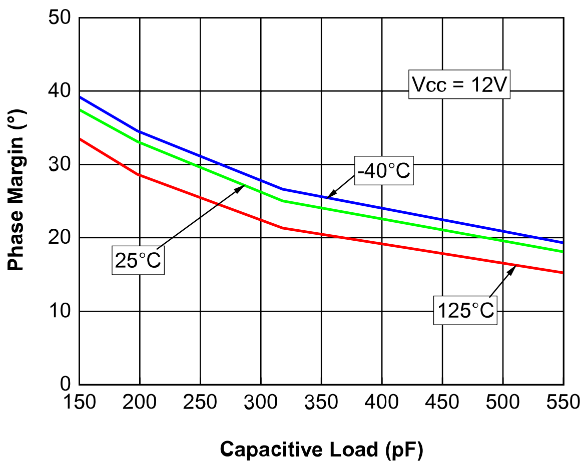


Figure 21. Phase margin vs. capacitive load at V_{CC} = 36 V

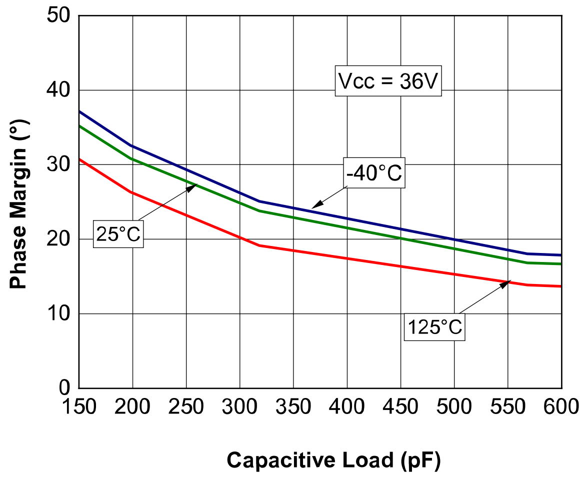


Figure 22. Short-circuit current vs. temperature

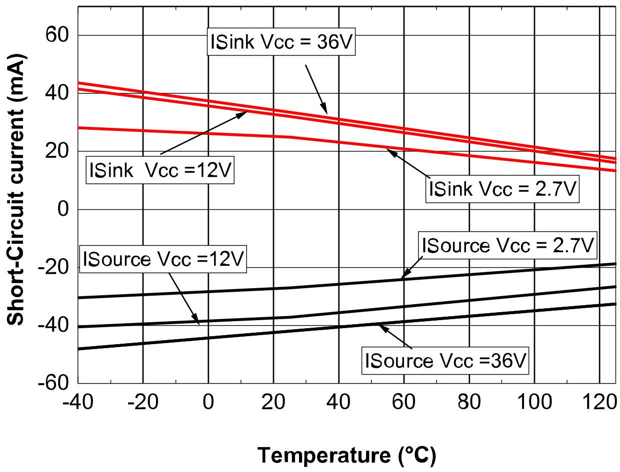


Figure 23. Output source current vs. output voltage at V_{CC} = 2.7 V

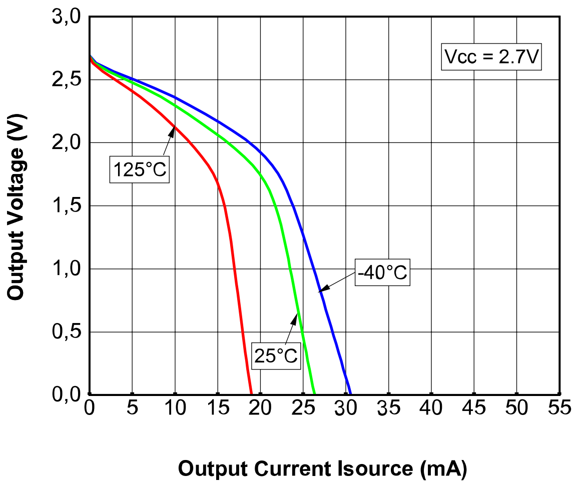


Figure 24. Output source current vs. output voltage at V_{CC} = 12 V

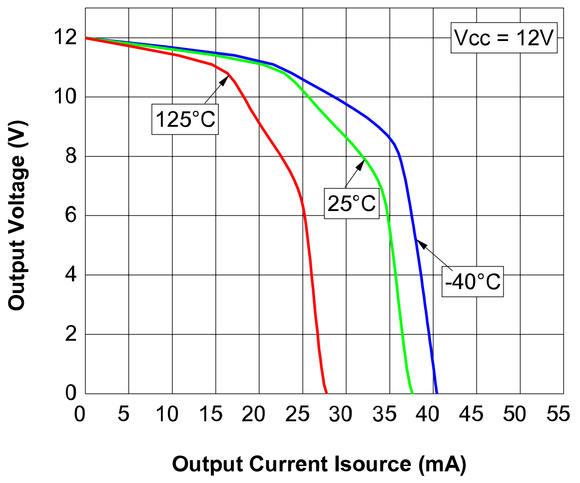


Figure 25. Output source current vs. output voltage at V_{CC} = 36 V

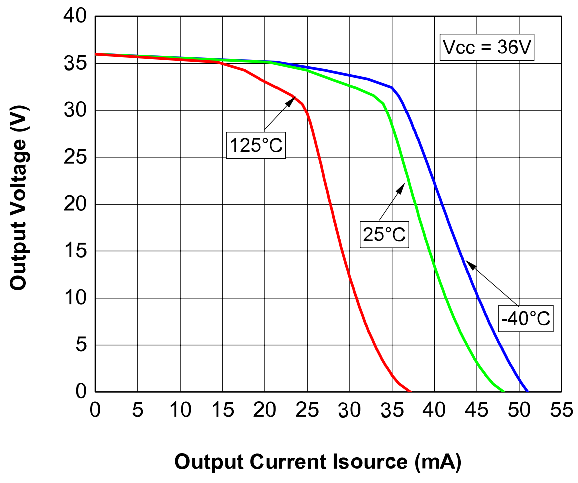


Figure 26. Output sink current vs. output voltage at V_{CC} = 2.7 V

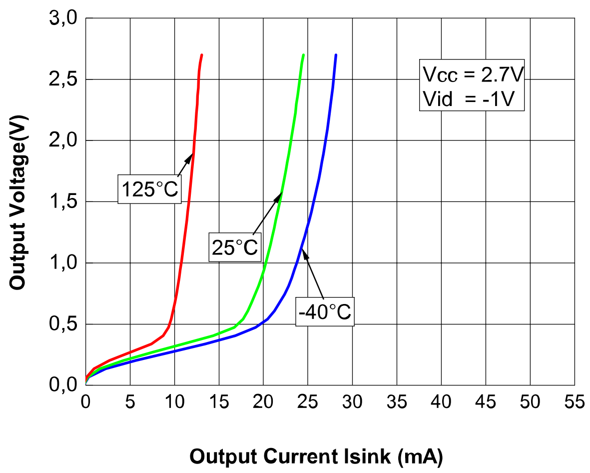


Figure 27. Output sink current vs. output voltage at V_{CC} = 12 V

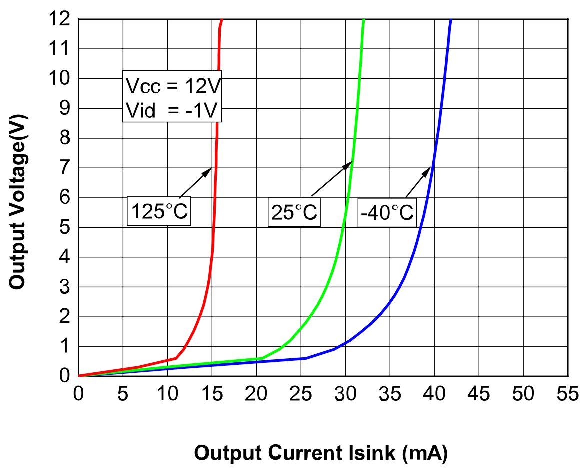


Figure 28. **Output sink current vs. output voltage at V_{CC} = 36 V**

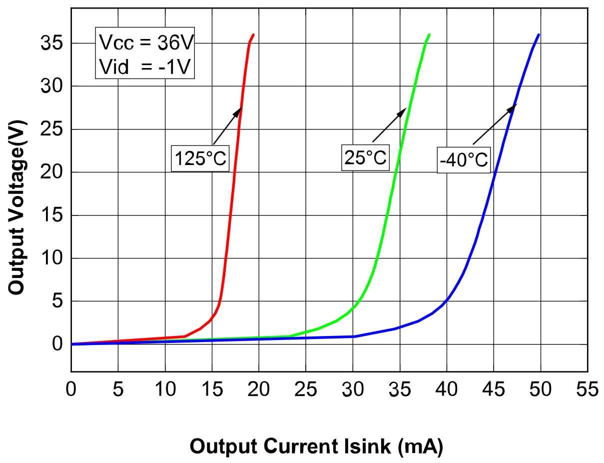


Figure 29. **Slew rate at V_{CC} = 2.7 V**

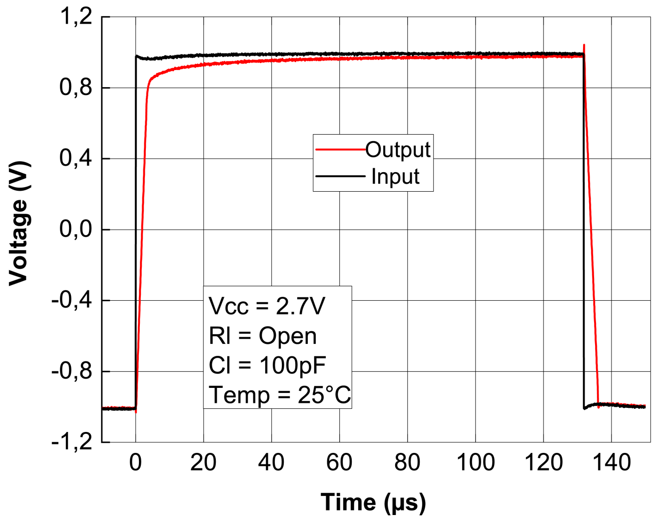


Figure 30. **Slew rate at V_{CC} = 12 V**

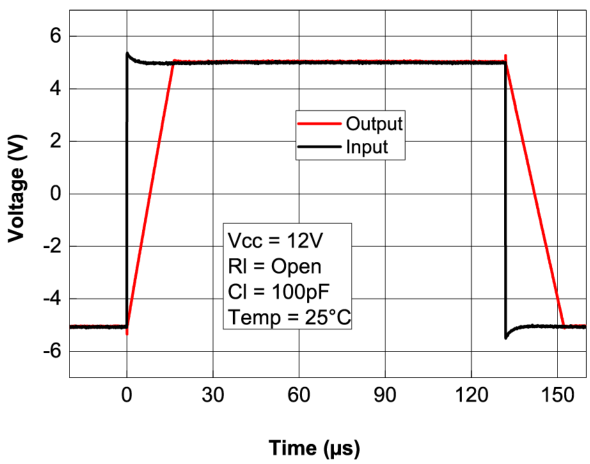


Figure 31. **Slew rate at V_{CC} = 36 V**

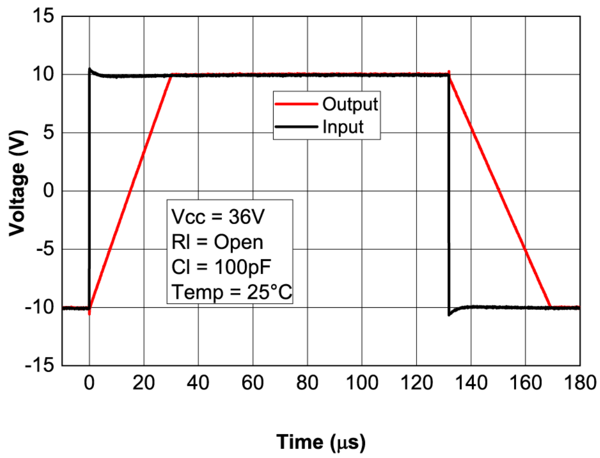


Figure 32. Slew rate vs. temperature at V_{CC} = 36 V

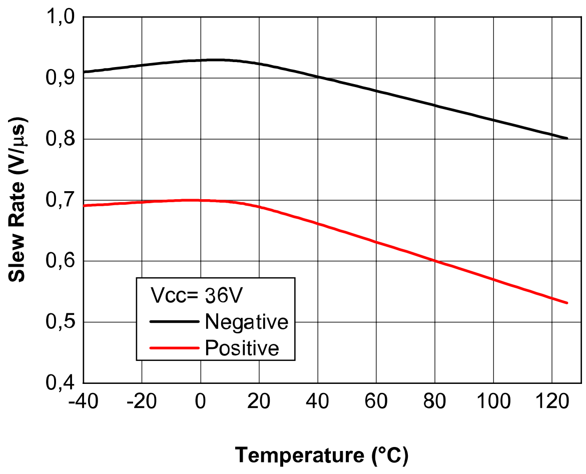


Figure 33. Small signal step response

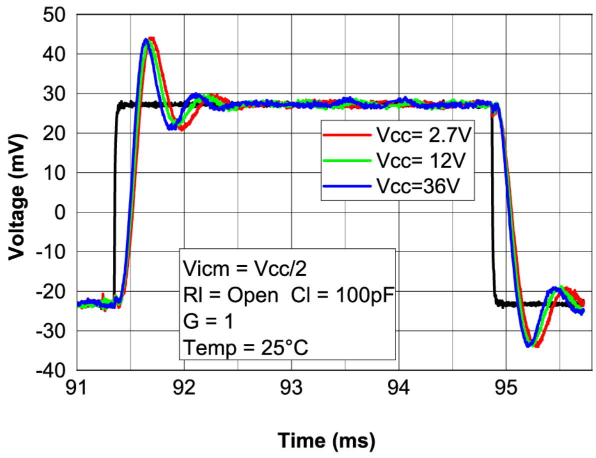


Figure 34. Maximum output voltage vs. frequency

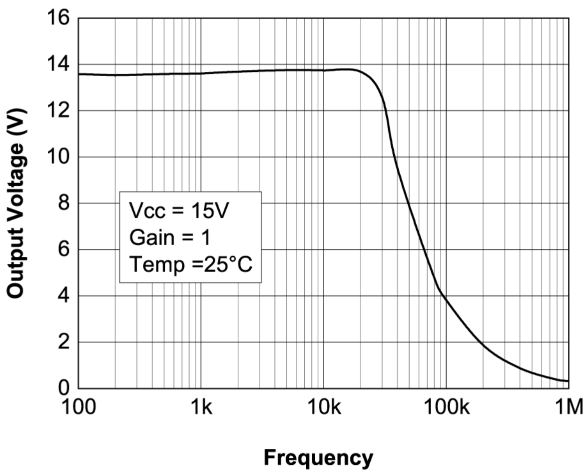


Figure 35. THD+Noise vs. frequency

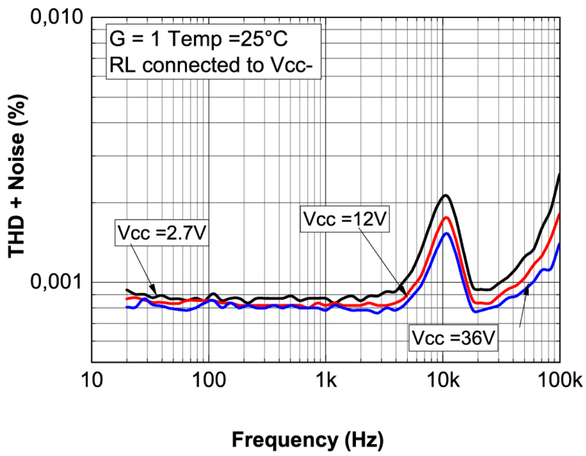


Figure 36. THD+Noise vs. output voltage

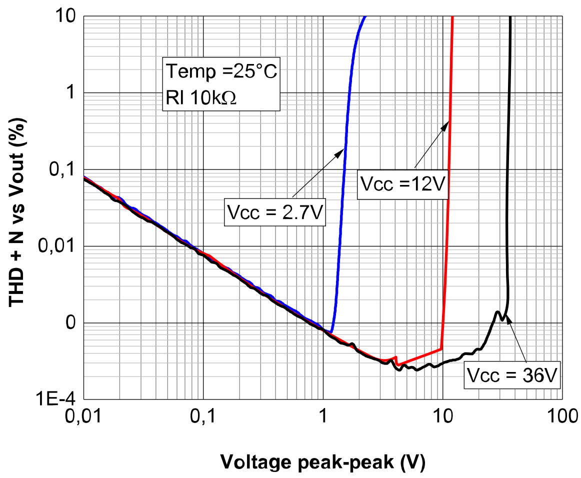


Figure 37. Cross talk vs. frequency

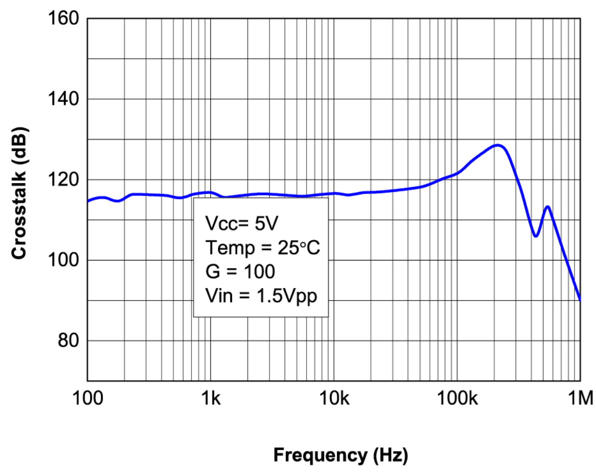
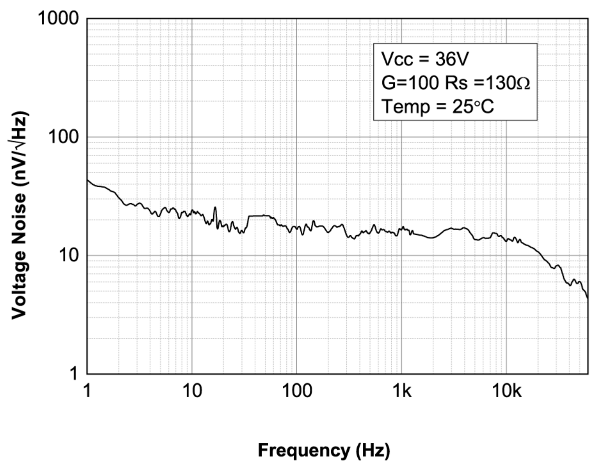


Figure 38. Equivalent input noise voltage vs. frequency



5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 SOT23-5 package information

Figure 39. **SOT23-5 package outline**

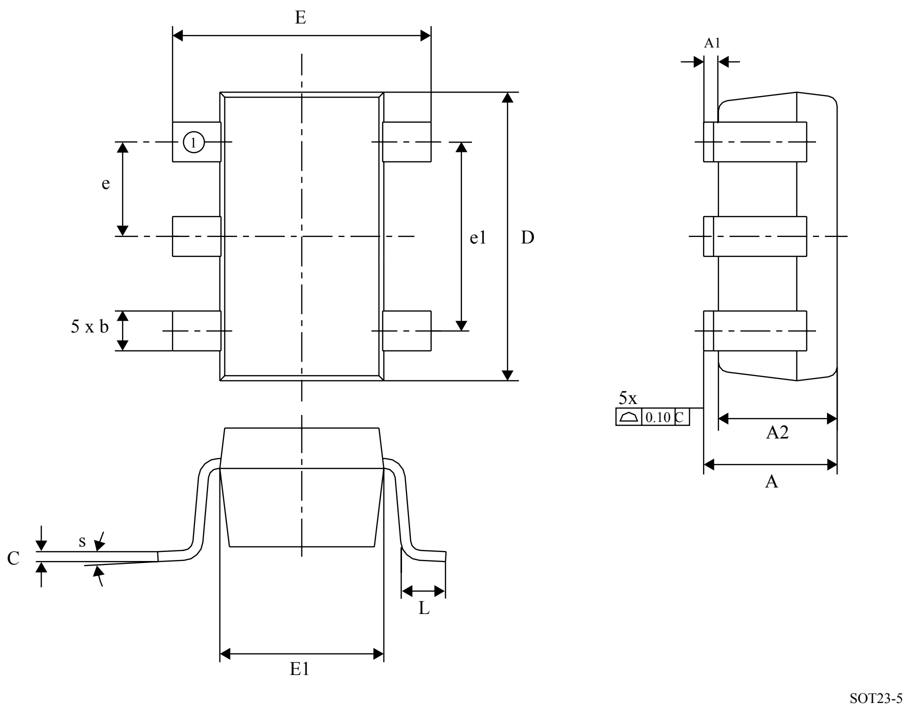


Table 9. **SOT23-5 mechanical data**

Symbol	Milimeters			Inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.45			0.057
A1	0.00		0.15	0.000		0.006
A2	0.90	1.15	1.30	0.035	0.045	0.051
b	0.30		0.50	0.012		0.020
c	0.08		0.22	0.003		0.009
D		2.90			0.114	
E		2.80			0.110	
E1		1.60			0.063	
e		0.95			0.037	
e1		1.90			0.075	
L	0.30	0.45	0.60	0.012	0.018	0.024
θ	0	4	8	0	4	8

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*

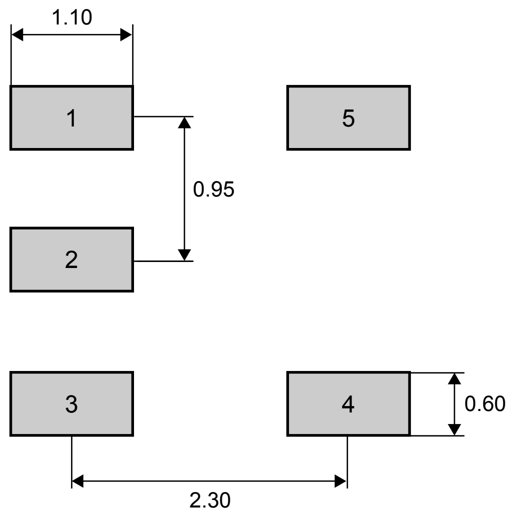


Figure 40. SOT23-5 recommended footprint

5.2 SO8 package information

Figure 41. SO8 package outline

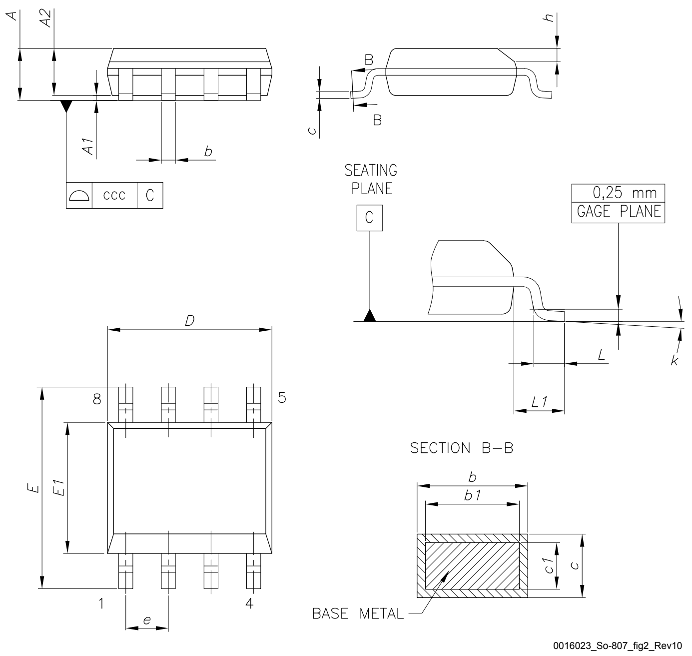


Table 10. SO8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

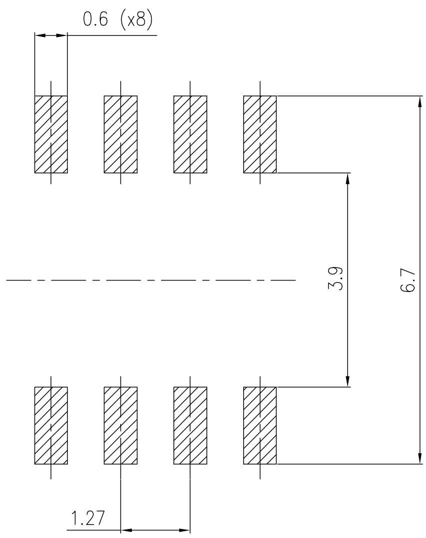


Figure 42. **SO8 recommended footprint**

5.3 MiniSO8 package information

Figure 43. MiniSO8 package outline

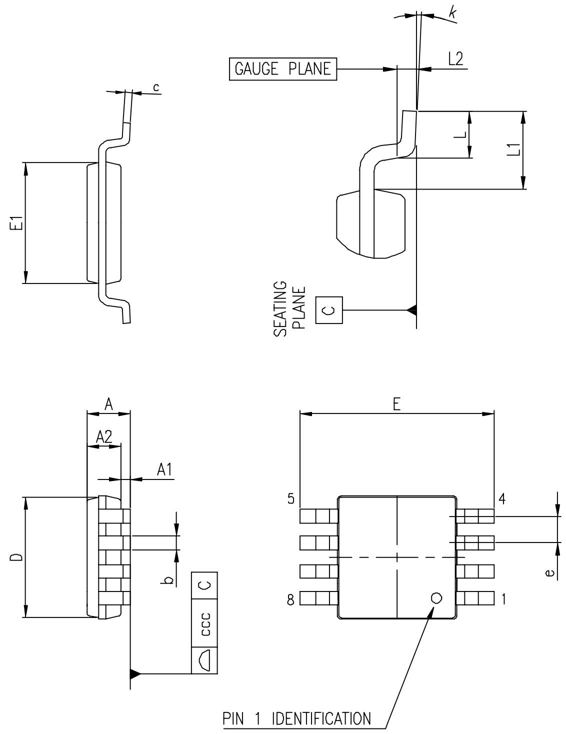
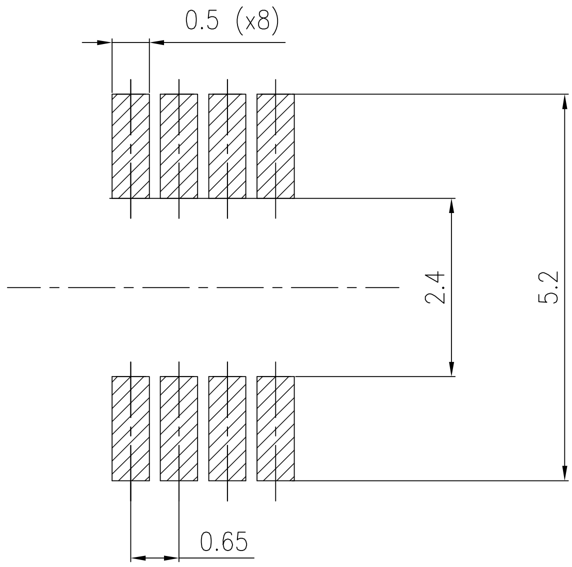


Table 11. MiniSO8 mechanical data

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.03	0.033	0.037
b	0.22		0.4	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.8	3	3.2	0.11	0.118	0.126
E	4.65	4.9	5.15	0.183	0.193	0.203
E1	2.8	3	3.1	0.11	0.118	0.122
e		0.65			0.026	
L	0.4	0.6	0.8	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.01	
k	0°		8°	0°		8°
ccc			0.1			0.004

Figure 44. MiniSO8 recommended footprint



5.4 DFN8 3x3 wettable flanks package information (package code: A03Y)

Figure 45. DFN8 3x3 package outline and mechanical data

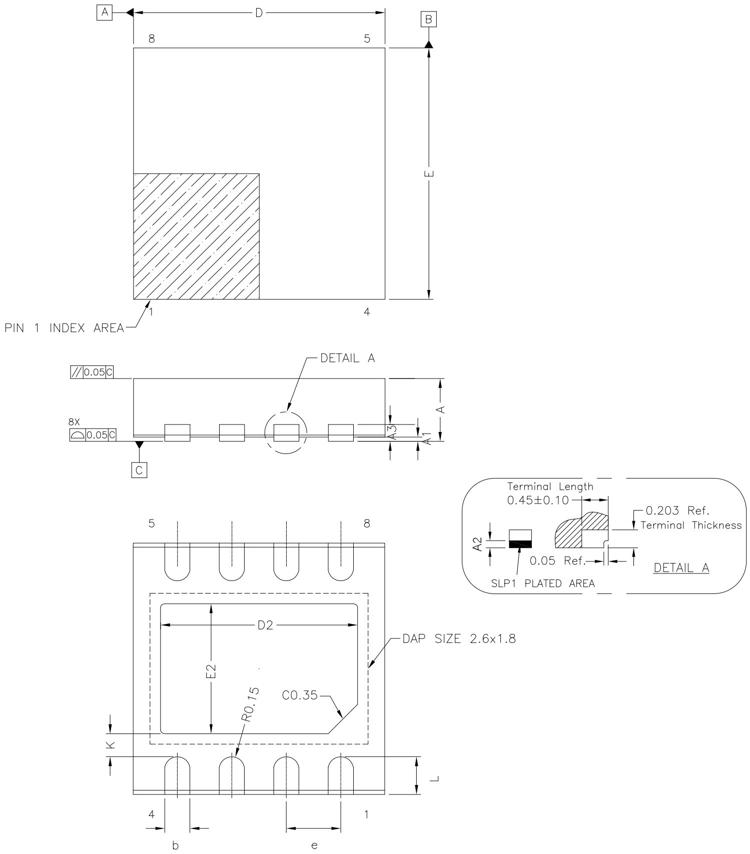


Table 12. DFN8 3x3 mechanical data

Symbol	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.0		0.05
A2	0.10		
A3	0.20 Ref.		
b	0.25	0.30	0.35
D	2.95	3.00	3.05
D2	2.25	2.35	2.45
e	0.65 BSC		
E	2.95	3.00	3.05
E2	1.45	1.55	1.65
L	0.35	0.45	0.55
K	0.275 Ref.		

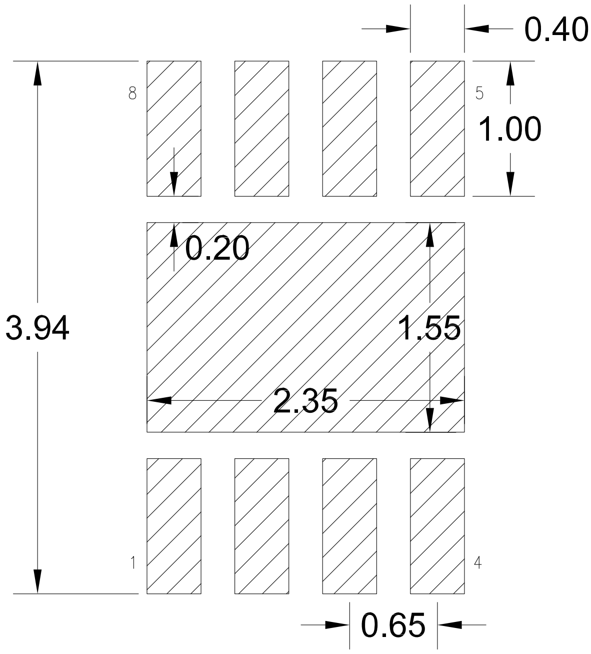


Figure 46. **DFN8 3x3 footprint data**

5.5 SO14 package information

Figure 47. SO14 package outline

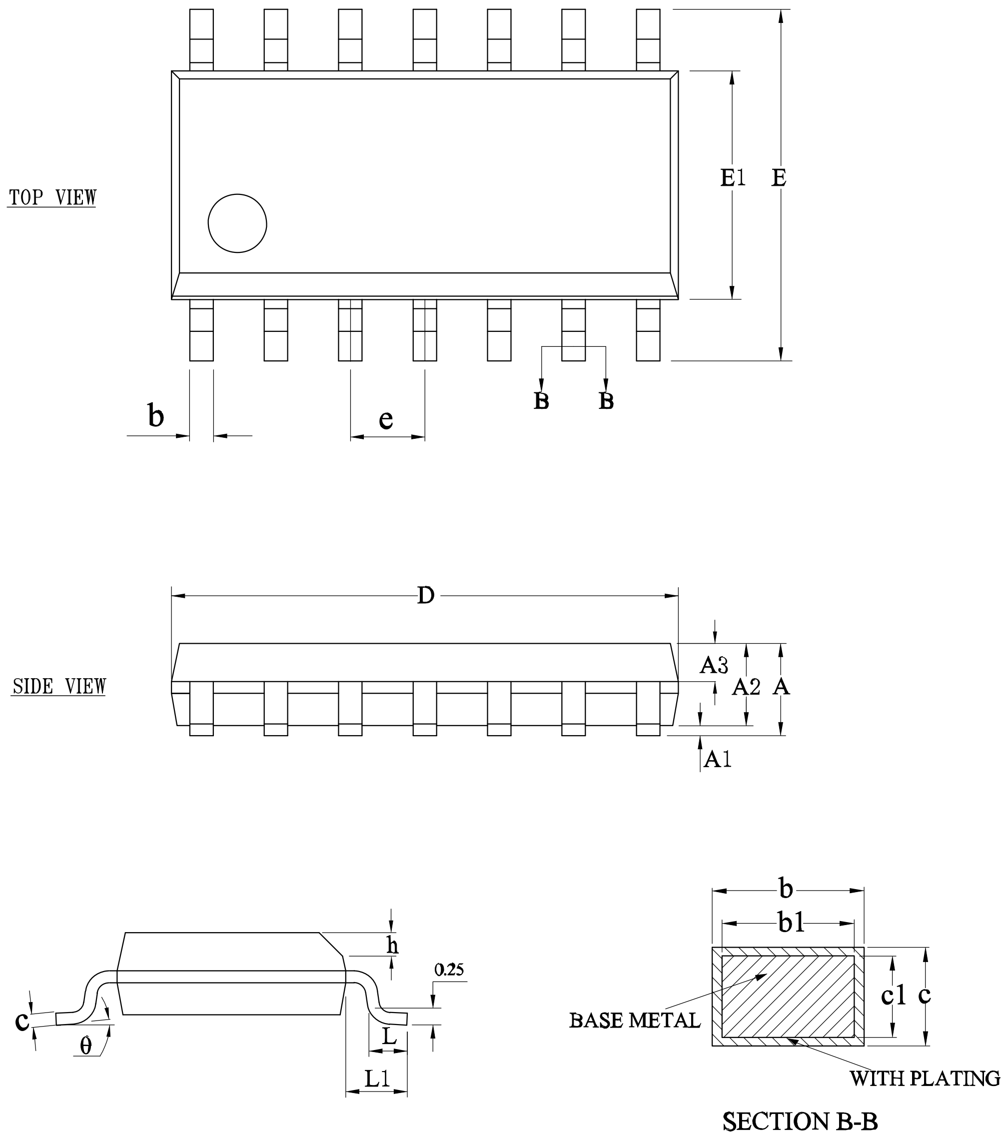
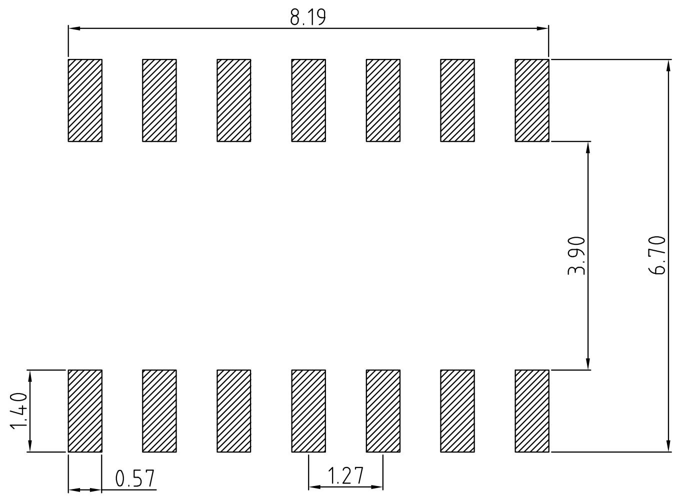


Table 13. **SO14 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39		0.47
b1	0.38	0.41	0.44
c	0.20		0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
h	0.25		0.50
L	0.50		0.80
L1	1.05 REF		
	0		8°

Figure 48. **SO14 recommended footprint**



5.6 TSSOP14 package information

Figure 49. TSSOP14 package outline

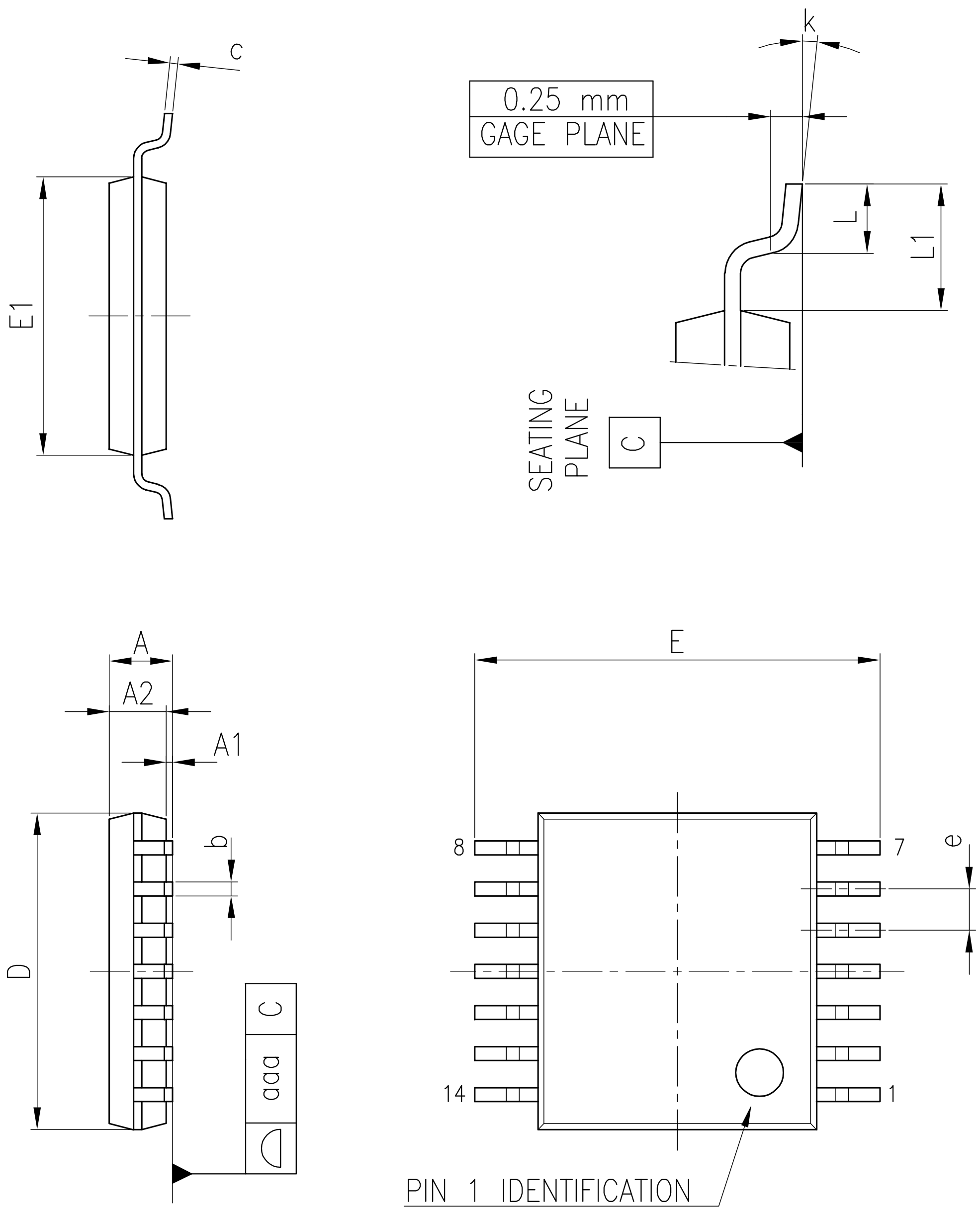


Table 14. **TSSOP14 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.20
A1	0.05		0.15
A2	0.80	1.00	1.05
b	0.19		0.30
c	0.09		0.20
D	4.90	5.00	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e		0.65	
L	0.45	0.60	0.75
L1		1.00	
k	0°		8°
aaa			0.10

6 Ordering information

Table 15. **Order code**

Order code	Package	Packaging	Marking
TSB621ILT	SOT23-5	Tape & Reel	K2K
TSB621IYLT [(1)]			K2L
TSB622IDT	SO8		TSB622I
TSB622IYDT [(1)]			TSB622IY
TSB622IST	MiniSO8		K2K
TSB622IYST [(1)]			K2L
TSB622IQ3T	DFN8 3x3 WF		K2K
TSB622IYQ3T [(1)]			K2L
TSB624IDT	SO14		TSB624I
TSB624IYDT [(1)]			TSB624IY
TSB624IPT	TSSOP14		TSB624I
TSB624IYPT [(1)]			TSB624IY

1. *Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.*

Revision history

Table 16. Document revision history

Date	Revision	Changes
03-Nov-2021	1	Initial release.
15-Feb-2022	2	Updated Figure 2.
01-Dec-2022	3	Added new TSSOP14, SO14 and SOT23-5 packages in Section 5 Package information. Updated Section 1 Pin connections, Table 4. Absolute maximum ratings, phase margin typical value in Table 6, Table 7, Table 8 and Section 6 Ordering information.

Contents

List of tables

List of figures