

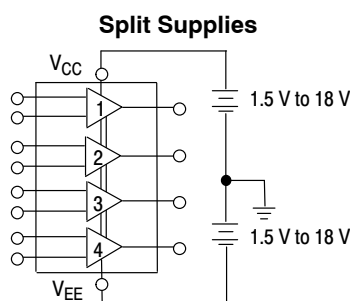
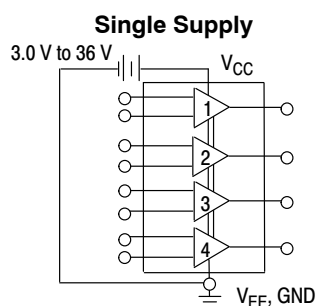
# MC3403, MC3303

## Single Supply Quad Operational Amplifiers

The MC3403 is a low cost, quad operational amplifier with true differential inputs. The device has electrical characteristics similar to the popular MC1741C. However, the MC3403 has several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 V or as high as 36 V with quiescent currents about one third of those associated with the MC1741C (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

### Features

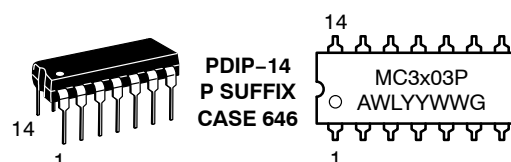
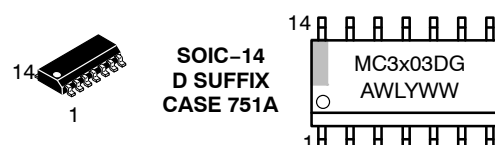
- Short Circuit Protected Outputs
- Class AB Output Stage for Minimal Crossover Distortion
- True Differential Input Stage
- Single Supply Operation: 3.0 V to 36 V
- Split Supply Operation:  $\pm 1.5$  V to  $\pm 18$  V
- Low Input Bias Currents: 500 nA Max
- Four Amplifiers Per Package
- Internally Compensated
- Similar Performance to Popular MC1741C
- Industry Standard Pin-outs
- ESD Diodes Added for Increased Ruggedness
- Pb-Free Packages are Available



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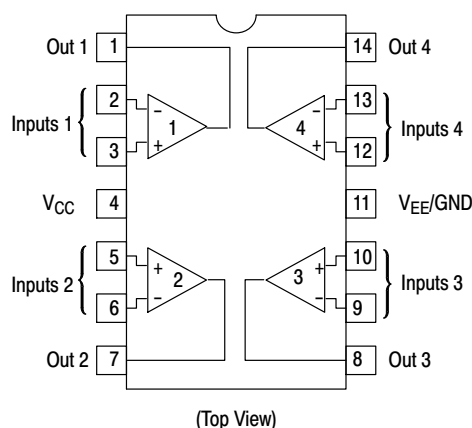
<http://onsemi.com>

### MARKING DIAGRAMS



x = 3 or 4  
A = Assembly Location  
WL = Wafer Lot  
YY, Y = Year  
WW = Work Week  
G = Pb-Free Package

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# MC3403, MC3303

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC3303D	SOIC-14	55 Units / Rail
MC3303DG	SOIC-14 (Pb-Free)	
MC3303DR2	SOIC-14	2500 Tape & Reel
MC3303DR2G	SOIC-14 (Pb-Free)	
MC3303P	PDIP-14	25 Units / Rail
MC3303PG	PDIP-14 (Pb-Free)	
MC3403D	SOIC-14	55 Units / Rail
MC3403DG	SOIC-14 (Pb-Free)	
MC3403DR2	SOIC-14	2500 Tape & Reel
MC3403DR2G	SOIC-14 (Pb-Free)	
MC3403P	PDIP-14	25 Units / Rail
MC3403PG	PDIP-14 (Pb-Free)	

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltages Single Supply Split Supplies	$V_{CC}$ $V_{CC}, V_{EE}$	36 $\pm 18$	Vdc
Input Differential Voltage Range (Note 1)	$V_{IDR}$	$\pm 36$	Vdc
Input Common Mode Voltage Range (Notes 1 and 2)	$V_{ICR}$	$\pm 18$	Vdc
Storage Temperature Range	$T_{stg}$	-55 to +125	°C
Operating Ambient Temperature Range MC3303 MC3403	$T_A$	-40 to +85 0 to +70	°C
Junction Temperature	$T_J$	150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Split power supplies.

2. For supply voltages less than  $\pm 18$  V, the absolute maximum input voltage is equal to the supply voltage.

# MC3403, MC3303

## ELECTRICAL CHARACTERISTICS

( $V_{CC} = +15\text{ V}$ ,  $V_{EE} = -15\text{ V}$  for MC3403;  $V_{CC} = +14\text{ V}$ ,  $V_{EE} = \text{GND}$  for MC3303  $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

Characteristic	Symbol	MC3403			MC3303			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage $T_A = T_{\text{high}}$ to $T_{\text{low}}$ (Note 3)	$V_{IO}$	–	2.0	10	–	2.0	8.0	mV
		–	–	12	–	–	10	
Input Offset Current $T_A = T_{\text{high}}$ to $T_{\text{low}}$	$I_{IO}$	–	30	50	–	30	75	nA
		–	–	200	–	–	250	
Large Signal Open Loop Voltage Gain $V_O = \pm 10\text{ V}$ , $R_L = 2.0\text{ k}\Omega$ $T_A = T_{\text{high}}$ to $T_{\text{low}}$	$A_{VOL}$	20	200	–	20	200	–	V/mV
		15	–	–	15	–	–	
Input Bias Current $T_A = T_{\text{high}}$ to $T_{\text{low}}$	$I_{IB}$	–	–200	–500	–	–200	–500	nA
		–	–	–800	–	–	–1000	
Output Impedance $f = 20\text{ Hz}$	$z_o$	–	75	–	–	75	–	$\Omega$
Input Impedance $f = 20\text{ Hz}$	$z_i$	0.3	1.0	–	0.3	1.0	–	M $\Omega$
Output Voltage Range $R_L = 10\text{ k}\Omega$ $R_L = 2.0\text{ k}\Omega$ $R_L = 2.0\text{ k}\Omega$ , $T_A = T_{\text{high}}$ to $T_{\text{low}}$	$V_O$	$\pm 12$	$\pm 13.5$	–	12	12.5	–	V
		$\pm 10$	$\pm 13$	–	10	12	–	
		$\pm 10$	–	–	10	–	–	
Input Common Mode Voltage Range	$V_{ICR}$	+13 V – $V_{EE}$	+13 V – $V_{EE}$	–	+12 V – $V_{EE}$	+12.5 V – $V_{EE}$	–	V
Common Mode Rejection $R_S \leq 10\text{ k}\Omega$	CMR	70	90	–	70	90	–	dB
Power Supply Current ( $V_O = 0$ ) $R_L = \infty$	$I_{CC}$ , $I_{EE}$	–	2.8	7.0	–	2.8	7.0	mA
Individual Output Short-Circuit Current (Note 4)	$I_{SC}$	$\pm 10$	$\pm 20$	$\pm 45$	$\pm 10$	$\pm 30$	$\pm 45$	mA
Positive Power Supply Rejection Ratio	PSRR+	–	30	150	–	30	150	$\mu\text{V/V}$
Negative Power Supply Rejection Ratio	PSRR–	–	30	150	–	30	150	$\mu\text{V/V}$
Average Temperature Coefficient of Input Offset Current $T_A = T_{\text{high}}$ to $T_{\text{low}}$	$\Delta I_{IO}/\Delta T$	–	50	–	–	50	–	$\text{pA}/^\circ\text{C}$
Average Temperature Coefficient of Input Offset Voltage $T_A = T_{\text{high}}$ to $T_{\text{low}}$	$\Delta V_{IO}/\Delta T$	–	10	–	–	10	–	$\mu\text{V}/^\circ\text{C}$
Power Bandwidth $A_V = 1$ , $R_L = 10\text{ k}\Omega$ , $V_O = 20\text{ V(p-p)}$ , THD = 5%	BWp	–	9.0	–	–	9.0	–	kHz
Small-Signal Bandwidth $A_V = 1$ , $R_L = 10\text{ k}\Omega$ , $V_O = 50\text{ mV}$	BW	–	1.0	–	–	1.0	–	MHz
Slew Rate $A_V = 1$ , $V_i = -10\text{ V}$ to $+10\text{ V}$	SR	–	0.6	–	–	0.6	–	V/ $\mu\text{s}$
Rise Time $A_V = 1$ , $R_L = 10\text{ k}\Omega$ , $V_O = 50\text{ mV}$	$t_{TLH}$	–	0.35	–	–	0.35	–	$\mu\text{s}$
Fall Time $A_V = 1$ , $R_L = 10\text{ k}\Omega$ , $V_O = 50\text{ mV}$	$t_{TLH}$	–	0.35	–	–	0.35	–	$\mu\text{s}$
Overshoot $A_V = 1$ , $R_L = 10\text{ k}\Omega$ , $V_O = 50\text{ mV}$	os	–	20	–	–	20	–	%
Phase Margin $A_V = 1$ , $R_L = 2.0\text{ k}\Omega$ , $V_O = 200\text{ pF}$	$\phi_m$	–	60	–	–	60	–	$^\circ$
Crossover Distortion ( $V_{in} = 30\text{ mVpp}$ , $V_{out} = 2.0\text{ Vpp}$ , $f = 10\text{ kHz}$ )	–	–	1.0	–	–	1.0	–	%

3. MC3303:  $T_{\text{low}} = -40^\circ\text{C}$ ,  $T_{\text{high}} = +85^\circ\text{C}$ , MC3403:  $T_{\text{low}} = 0^\circ\text{C}$ ,  $T_{\text{high}} = +70^\circ\text{C}$

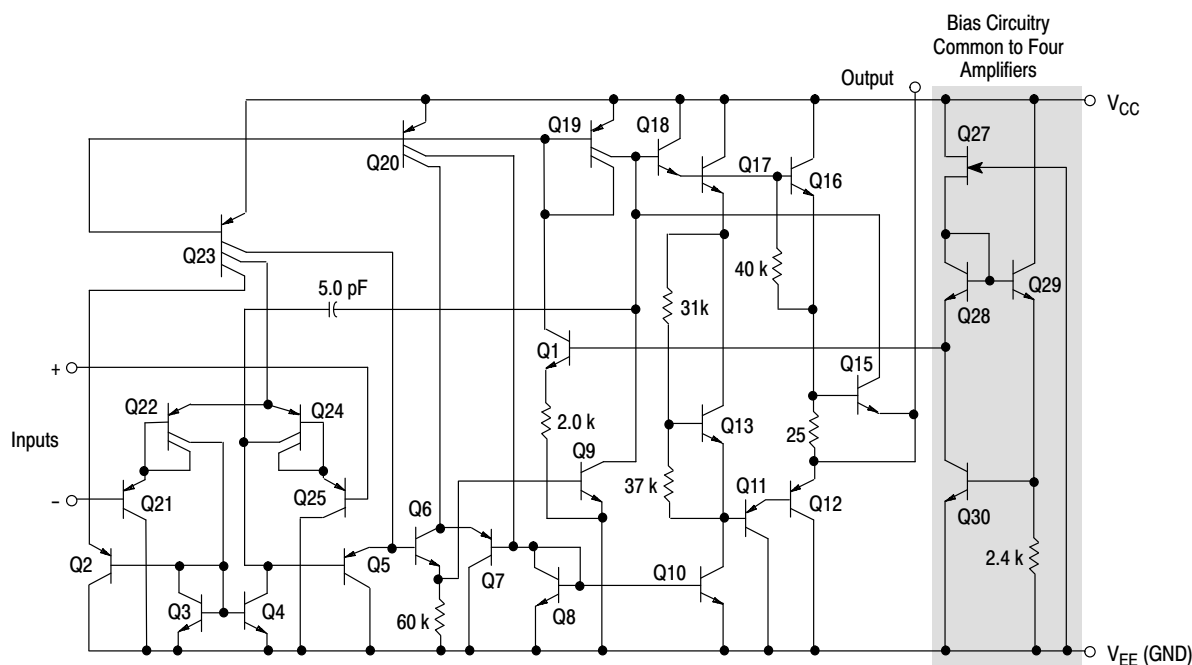
4. Not to exceed maximum package power dissipation.

# MC3403, MC3303

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5.0\text{ V}$ ,  $V_{EE} = \text{GND}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

Characteristic	Symbol	MC3403			MC3303			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$V_{IO}$	–	2.0	10	–	–	10	mV
Input Offset Current	$I_{IO}$	–	30	50	–	–	75	nA
Input Bias Current	$I_{IB}$	–	–200	–500	–	–	–500	nA
Large Signal Open Loop Voltage Gain $R_L = 2.0\text{ k}\Omega$	$A_{VOL}$	10	200	–	10	200	–	V/mV
Power Supply Rejection Ratio	PSRR	–	–	150	–	–	150	$\mu\text{V/V}$
Output Voltage Range (Note 5) $R_L = 10\text{ k}\Omega$ , $V_{CC} = 5.0\text{ V}$ $R_L = 10\text{ k}\Omega$ , $5.0 \leq V_{CC} \leq 30\text{ V}$	$V_{OR}$	3.3 $V_{CC}-2.0$	3.5 $V_{CC}-1.7$	– –	3.3 $V_{CC}-2.0$	3.5 $V_{CC}-1.7$	– –	$V_{pp}$
Power Supply Current	$I_{CC}$	–	2.5	7.0	–	2.5	7.0	mA
Channel Separation $f = 1.0\text{ kHz to } 20\text{ kHz}$ (Input Referenced)	CS	–	–120	–	–	–120	–	dB

5. Output will swing to ground with a 10 k $\Omega$  pull down resistor.



**Figure 1. Representative Schematic Diagram**  
(1/4 of Circuit Shown)

## CIRCUIT DESCRIPTION

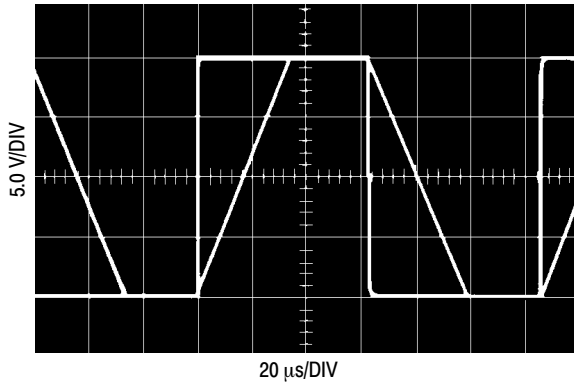


Figure 2. Inverter Pulse Response

The MC3403/3303 is made using four internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input device Q24 and Q22 with input buffer transistors Q25 and Q21 and the differential to single ended converter Q3 and Q4. The first

stage performs not only the first stage gain function but also performs the level shifting and Transconductance reduction functions. By reducing the Transconductance, a smaller compensation capacitor (only 5.0 pF) can be employed, thus saving chip area. The Transconductance reduction is accomplished by splitting the collectors of Q24 and Q22. Another feature of this input stage is that the input common mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

The output stage is unique because it allows the output to swing to ground in single supply operation and yet does not exhibit any crossover distortion in split supply operation. This is possible because Class AB operation is utilized.

Each amplifier is biased from an internal voltage regulator which has a low temperature coefficient, thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

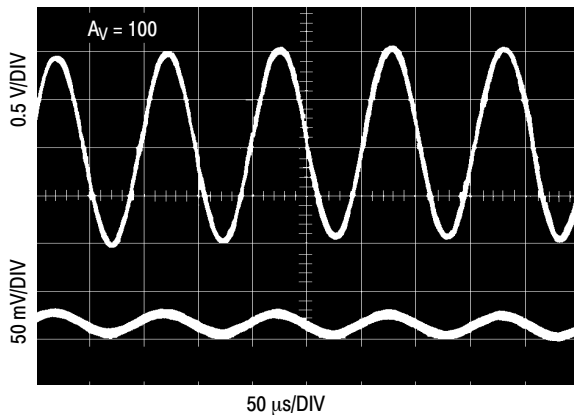


Figure 3. Sine Wave Response

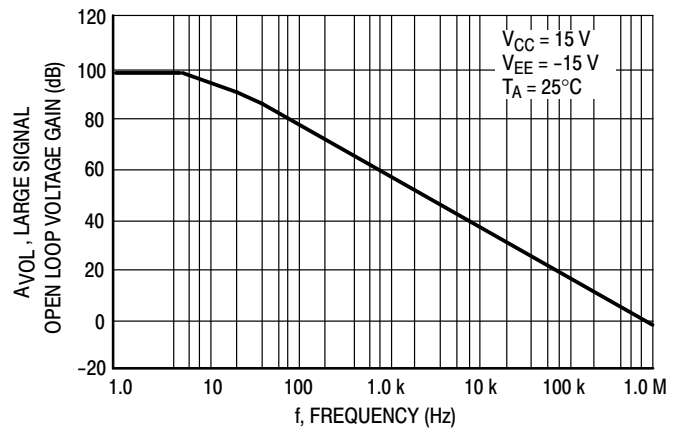


Figure 4. Open Loop Frequency Response

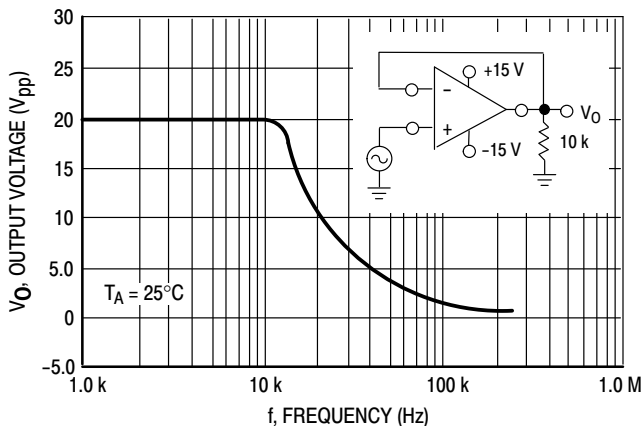


Figure 5. Power Bandwidth

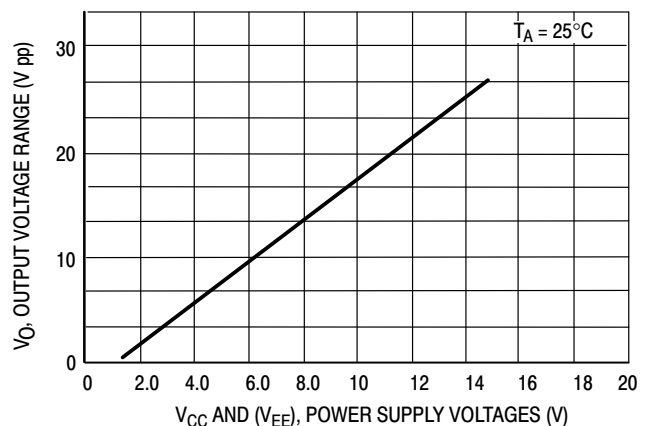
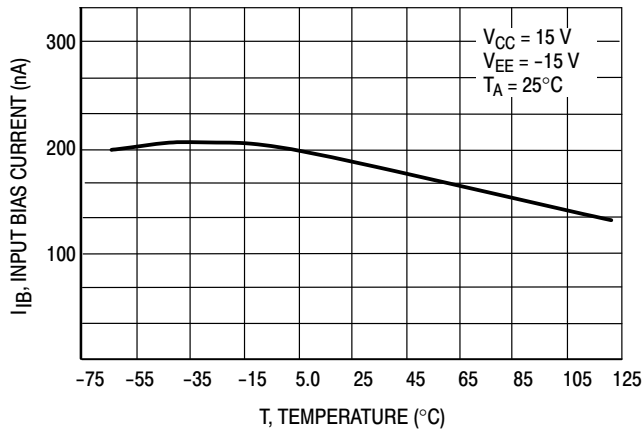
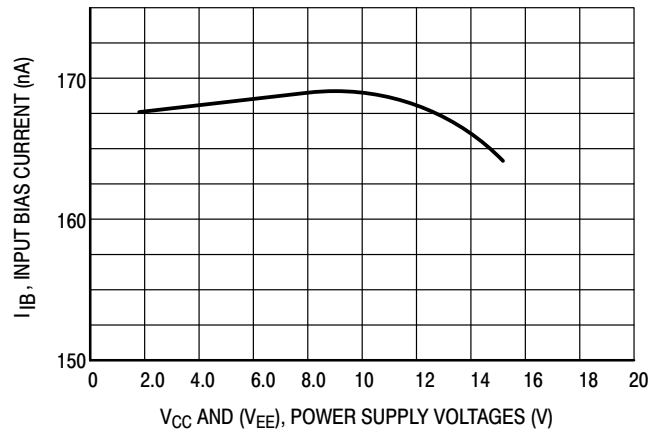


Figure 6. Output Swing versus Supply Voltage

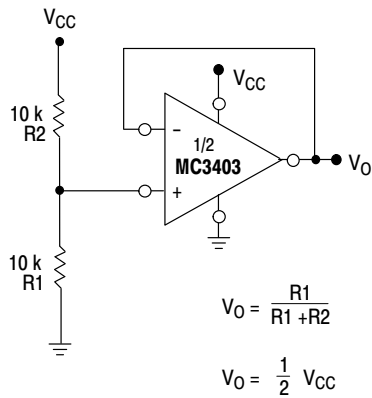
## MC3403, MC3303



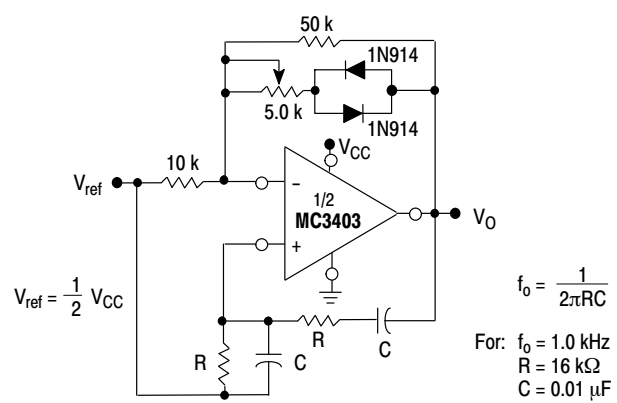
**Figure 7. Input Bias Current versus Temperature**



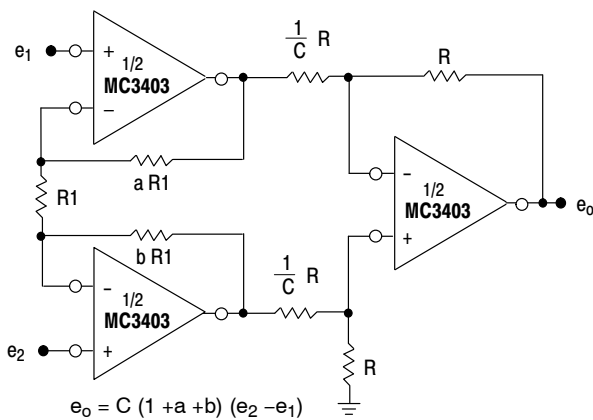
**Figure 8. Input Bias Current versus Supply Voltage**



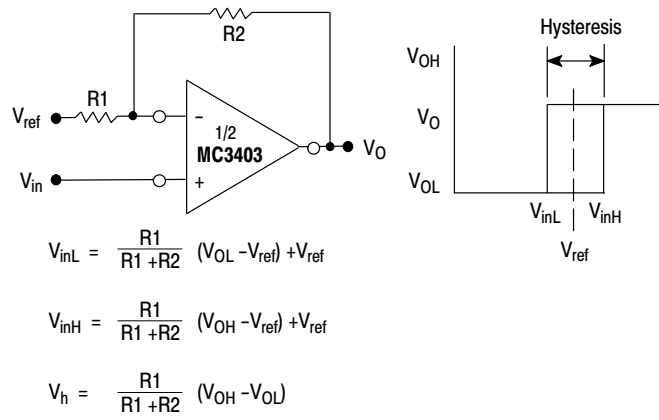
**Figure 9. Voltage Reference**



**Figure 10. Wien Bridge Oscillator**



**Figure 11. High Impedance Differential Amplifier**



**Figure 12. Comparator with Hysteresis**

## MC3403, MC3303

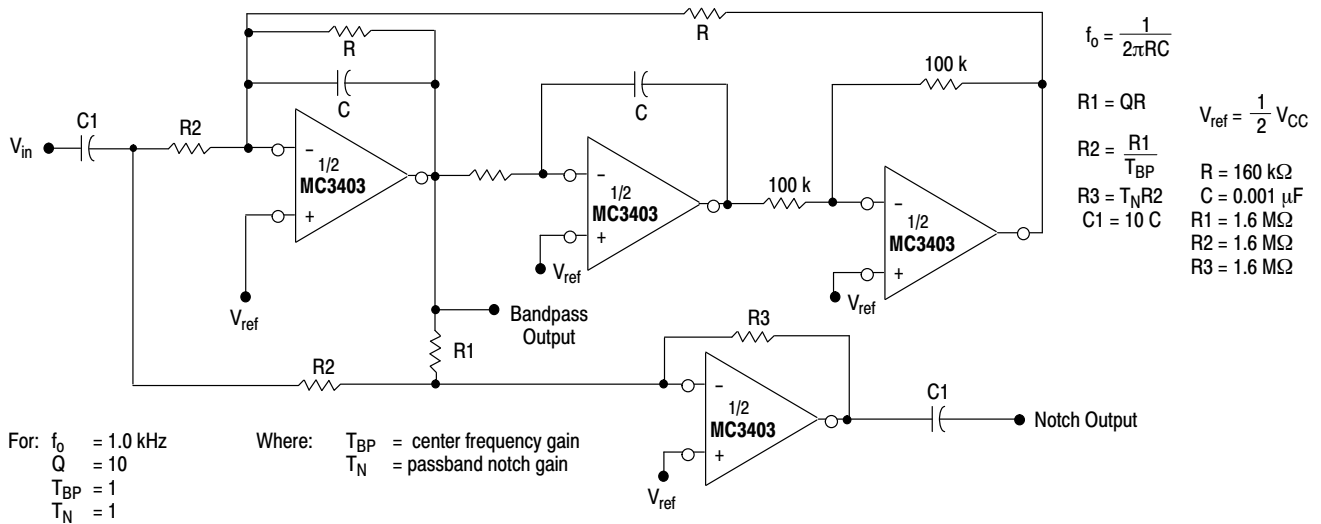


Figure 13. Bi-Quad Filter

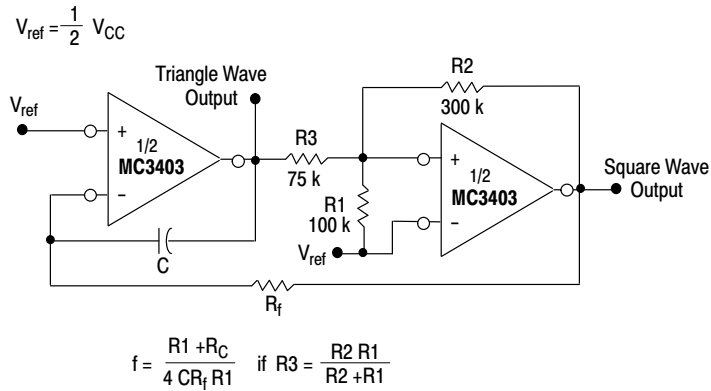
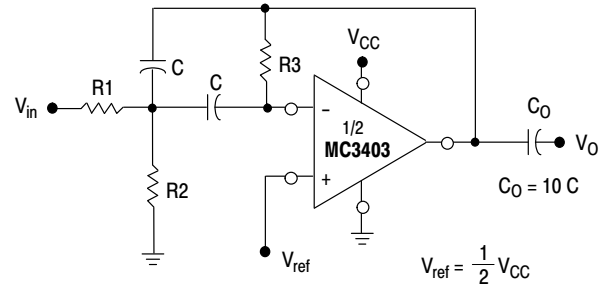


Figure 14. Function Generator



Given:  $f_0$  = center frequency  
 $A(f_0)$  = gain at center frequency

Choose value  $f_0$ ,  $C$

$$\text{Then: } R3 = \frac{Q}{\pi f_0 C} \quad R1 = \frac{R3}{2 A(f_0)} \quad R2 = \frac{R1 R5}{4 Q^2 R1 - R5}$$

For less than 10% error from operational amplifier where  $f_0$  and BW are expressed in Hz.

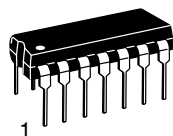
If source impedance varies, filter may be preceded by voltage follower buffer to stabilize filter parameters.

Figure 15. Multiple Feedback Bandpass Filter

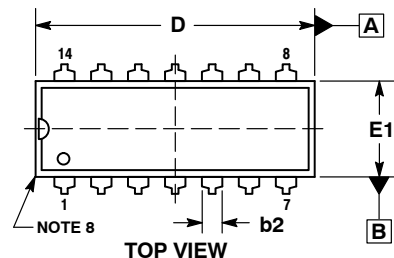
# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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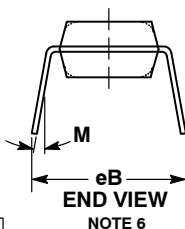
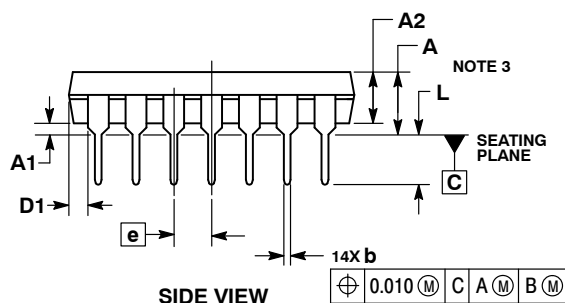
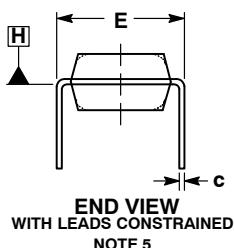


SCALE 1:1



PDIP-14  
CASE 646-06  
ISSUE S

DATE 22 APR 2015



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.210	---	5.33
A1	0.015	---	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.735	0.775	18.67	19.69
D1	0.005	---	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	---	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	---	10°	---	10°

### GENERIC MARKING DIAGRAM\*



STYLES ON PAGE 2

XXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.  
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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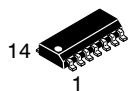
DATE 22 APR 2015

STYLE 1: PIN 1. COLLECTOR 2. BASE 3. EMITTER 4. NO CONNECTION 5. EMITTER 6. BASE 7. COLLECTOR 8. COLLECTOR 9. BASE 10. EMITTER 11. NO CONNECTION 12. EMITTER 13. BASE 14. COLLECTOR	STYLE 2: CANCELLED	STYLE 3: CANCELLED	STYLE 4: PIN 1. DRAIN 2. SOURCE 3. GATE 4. NO CONNECTION 5. GATE 6. SOURCE 7. DRAIN 8. DRAIN 9. SOURCE 10. GATE 11. NO CONNECTION 12. GATE 13. SOURCE 14. DRAIN
STYLE 5: PIN 1. GATE 2. DRAIN 3. SOURCE 4. NO CONNECTION 5. SOURCE 6. DRAIN 7. GATE 8. GATE 9. DRAIN 10. SOURCE 11. NO CONNECTION 12. SOURCE 13. DRAIN 14. GATE	STYLE 6: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. NO CONNECTION 5. ANODE/CATHODE 6. NO CONNECTION 7. ANODE/CATHODE 8. ANODE/CATHODE 9. ANODE/CATHODE 10. NO CONNECTION 11. ANODE/CATHODE 12. ANODE/CATHODE 13. NO CONNECTION 14. COMMON ANODE	STYLE 7: PIN 1. NO CONNECTION 2. ANODE 3. ANODE 4. NO CONNECTION 5. ANODE 6. NO CONNECTION 7. ANODE 8. ANODE 9. ANODE 10. NO CONNECTION 11. ANODE 12. ANODE 13. NO CONNECTION 14. COMMON CATHODE	STYLE 8: PIN 1. NO CONNECTION 2. CATHODE 3. CATHODE 4. NO CONNECTION 5. CATHODE 6. NO CONNECTION 7. CATHODE 8. CATHODE 9. CATHODE 10. NO CONNECTION 11. CATHODE 12. CATHODE 13. NO CONNECTION 14. COMMON ANODE
STYLE 9: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. NO CONNECTION 5. ANODE/CATHODE 6. ANODE/CATHODE 7. COMMON ANODE 8. COMMON ANODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. NO CONNECTION 12. ANODE/CATHODE 13. ANODE/CATHODE 14. COMMON CATHODE	STYLE 10: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. ANODE/CATHODE 5. ANODE/CATHODE 6. NO CONNECTION 7. COMMON ANODE 8. COMMON CATHODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. ANODE/CATHODE 12. ANODE/CATHODE 13. NO CONNECTION 14. COMMON ANODE	STYLE 11: PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. ANODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE	STYLE 12: PIN 1. COMMON CATHODE 2. COMMON ANODE 3. ANODE/CATHODE 4. ANODE/CATHODE 5. ANODE/CATHODE 6. COMMON ANODE 7. COMMON CATHODE 8. ANODE/CATHODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. ANODE/CATHODE 12. ANODE/CATHODE 13. ANODE/CATHODE 14. ANODE/CATHODE

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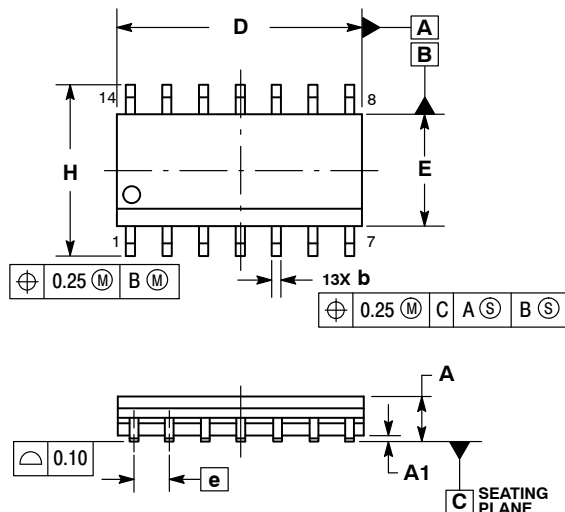
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-14 NB  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016

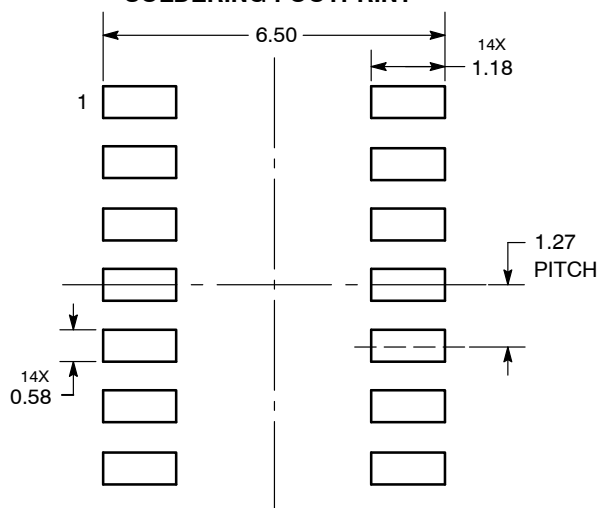


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

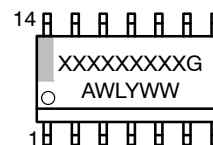
## SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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**SOIC-14**  
**CASE 751A-03**  
**ISSUE L**

DATE 03 FEB 2016

STYLE 1:  
PIN 1. COMMON CATHODE  
2. ANODE/CATHODE  
3. ANODE/CATHODE  
4. NO CONNECTION  
5. ANODE/CATHODE  
6. NO CONNECTION  
7. ANODE/CATHODE  
8. ANODE/CATHODE  
9. ANODE/CATHODE  
10. NO CONNECTION  
11. ANODE/CATHODE  
12. ANODE/CATHODE  
13. NO CONNECTION  
14. COMMON ANODE

STYLE 2:  
CANCELLED

STYLE 3:  
PIN 1. NO CONNECTION  
2. ANODE  
3. ANODE  
4. NO CONNECTION  
5. ANODE  
6. NO CONNECTION  
7. ANODE  
8. ANODE  
9. ANODE  
10. NO CONNECTION  
11. ANODE  
12. ANODE  
13. NO CONNECTION  
14. COMMON CATHODE

STYLE 4:  
PIN 1. NO CONNECTION  
2. CATHODE  
3. CATHODE  
4. NO CONNECTION  
5. CATHODE  
6. NO CONNECTION  
7. CATHODE  
8. CATHODE  
9. CATHODE  
10. NO CONNECTION  
11. CATHODE  
12. CATHODE  
13. NO CONNECTION  
14. COMMON ANODE

STYLE 5:  
PIN 1. COMMON CATHODE  
2. ANODE/CATHODE  
3. ANODE/CATHODE  
4. ANODE/CATHODE  
5. ANODE/CATHODE  
6. NO CONNECTION  
7. COMMON ANODE  
8. COMMON CATHODE  
9. ANODE/CATHODE  
10. ANODE/CATHODE  
11. ANODE/CATHODE  
12. ANODE/CATHODE  
13. NO CONNECTION  
14. COMMON ANODE

STYLE 6:  
PIN 1. CATHODE  
2. CATHODE  
3. CATHODE  
4. CATHODE  
5. CATHODE  
6. CATHODE  
7. CATHODE  
8. ANODE  
9. ANODE  
10. ANODE  
11. ANODE  
12. ANODE  
13. ANODE  
14. ANODE

STYLE 7:  
PIN 1. ANODE/CATHODE  
2. COMMON ANODE  
3. COMMON CATHODE  
4. ANODE/CATHODE  
5. ANODE/CATHODE  
6. ANODE/CATHODE  
7. ANODE/CATHODE  
8. ANODE/CATHODE  
9. ANODE/CATHODE  
10. ANODE/CATHODE  
11. COMMON CATHODE  
12. COMMON ANODE  
13. ANODE/CATHODE  
14. ANODE/CATHODE

STYLE 8:  
PIN 1. COMMON CATHODE  
2. ANODE/CATHODE  
3. ANODE/CATHODE  
4. NO CONNECTION  
5. ANODE/CATHODE  
6. ANODE/CATHODE  
7. COMMON ANODE  
8. COMMON ANODE  
9. ANODE/CATHODE  
10. ANODE/CATHODE  
11. NO CONNECTION  
12. ANODE/CATHODE  
13. ANODE/CATHODE  
14. COMMON CATHODE

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