

REAC1251J

Low Input Offset Voltage $V_{IO} \leq 1\text{mV} (@ -40^{\circ}\text{C} \text{ to } +125^{\circ}\text{C})$ R03DS0165EJ0100
 Single Power Supply Dual Operational Amplifiers Rev.1.00
 2021.7.12

DESCRIPTION

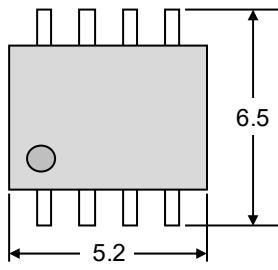
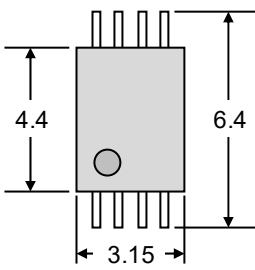
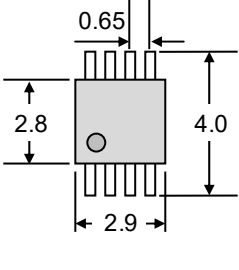
The REAC1251J is a single power and dual operational amplifiers which has features low input offset voltage $V_{IO} \leq \pm 1\text{mV}$ and low input offset voltage temperature drift in $T_a = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$. The features include low-voltage operation, a common-mode input voltage that range from V^- (GND) level, an output from a V^- (GND) level that is determined by the output stage of class C push-pull circuit and a $50\text{ }\mu\text{A}$ (TYP.) constant current, and a low current consumption.

In addition to that, this amplifier can also operate in both positive and negative power supply and can be used extensively in various amplifier circuits.

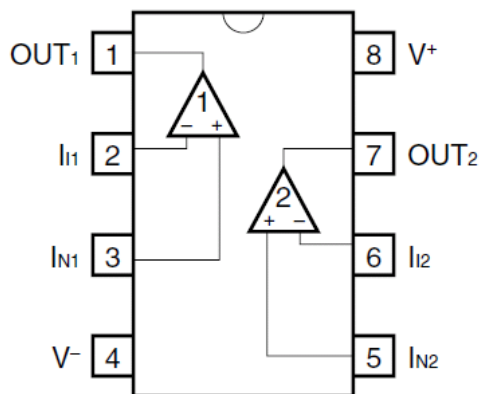
Features

- Low input offset voltage $\pm 1\text{mV}$ (Max.) @ $T_a : -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
- Low input offset voltage temperature drift $\pm 1\mu\text{V}/^{\circ}\text{C}$ (Typ.)
- Qualified and characterized according to AEC-Q100
- The package line-up is MSOP

ORDERING INFORMATION

Package	Standard SOP	TSSOP	MSOP
Subject Part Number	REAC1251JSM	REAC1251JSP	REAC1251JSN
Product Type	High Quality Level		
Quality Level	High Quality Level		
Outline Comparison	Unit : mm 	Unit : mm 	Unit : mm 
(Mounting Area Ratio)	(100 %)	(60 %)	(34 %)

PIN CONFIGURATION (Marking Side)



ABSOLUTE MAXIMUM RATINGS

<T_A= -40°C to +125 °C>

Parameter	Symbol	REAC1251JSM	REAC1251JSP	REAC1251JSN	Unit
Power Supply Voltage ^{Note.1}	V ⁺ - V ⁻	-0.1 to +32			V
Differential Input Voltage	V _{ID}	±10			V
Input Voltage ^{Note.2}	V _I	V ⁻ -0.1 to V ⁺ +32			V
Output applied Voltage ^{Note.3}	V _O	V ⁻ -0.1 to V ⁺ +0.1			V
Total Power Dissipation ^{Note.4}	P _T	440			mW
Output Short Circuit Duration ^{Note.5}	t _s	Indefinite			s
Operating Ambient Temperature	T _A	-40 to +125			°C
Storage Temperature	T _{stg}	-55 to +150			°C

Note

- Note that reverse connections of the power supply may damage ICs.
- The input voltage is allowed to input without damage or destruction independent of the magnitude of V⁺. Either input signal is not allowed to go negative by more than 0.1 V if the conditions are within absolute maximum ratings. This specification which includes the transition state such as electric power ON/OFF must be kept. In addition, the input voltage that operates normally as an operational amplifier is within the Common Mode Input Voltage range of an electrical characteristic.
- A range where input voltage can be applied to an output pin externally with no deterioration or damage to the feature (characteristic). The input voltage can be applied regardless of the electric supply voltage. This specification which includes the transition state such as electric power ON/OFF must be kept.
- This is the value of when the glass epoxy substrate (size: 100 mm x 100 mm, thickness: 1 mm, 15% of the substrate area where only one side is copper foiled is filling wired) is mounted.
Note that restrictions will be made to the following conditions for each product, and the derating ratio depending on the operating ambient temperature.

REAC1251JSM Derate at -4.4 mW/°C when T_A > 50°C.Junction □ ambient thermal resistance R_{th(J-A)}=227°C/WREAC1251JSP Derate at -5.5 mW/°C when T_A > 69°C.Junction □ ambient thermal resistance R_{th(J-A)}=183°C/WREAC1251JSN Derate at -4.8 mW/°C when T_A > 58°C.Junction □ ambient thermal resistance R_{th(J-A)}=208°C/W

- Short circuits from the output to V⁺ can cause destruction. Pay careful attention to the total power dissipation not to exceed the absolute maximum ratings, Note 4.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power Supply Voltage (Split)	$V^{\pm}$	± 1.5		± 15	V
Power Supply Voltage ($V^- = \text{GND}$)	V^+	+3		+30	V

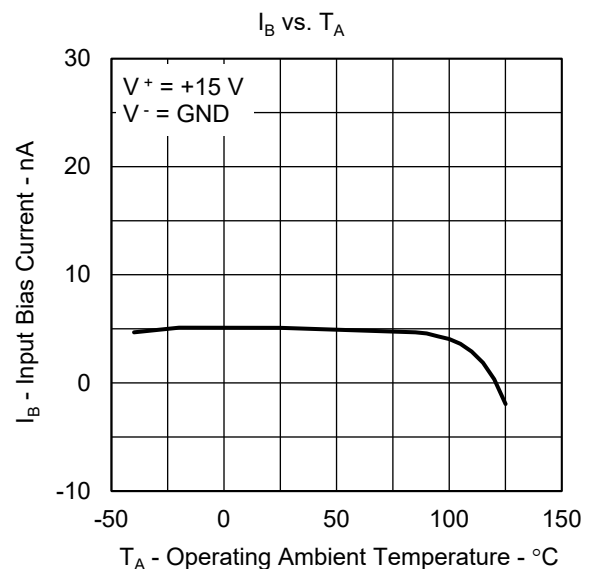
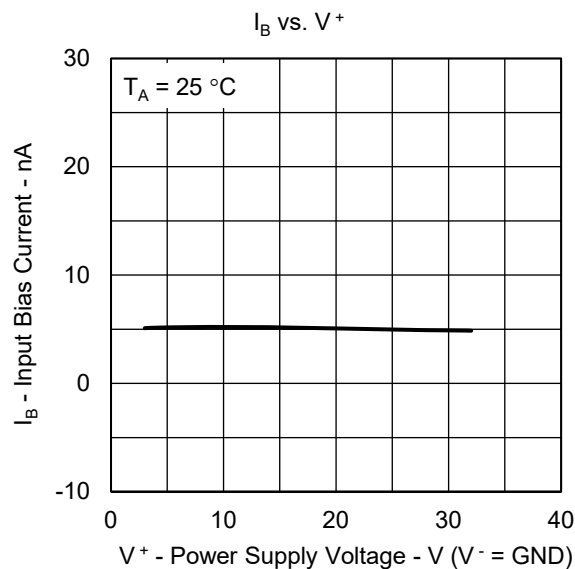
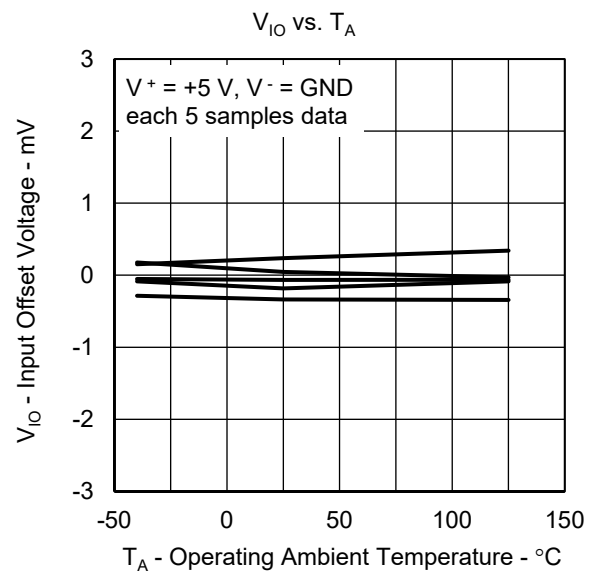
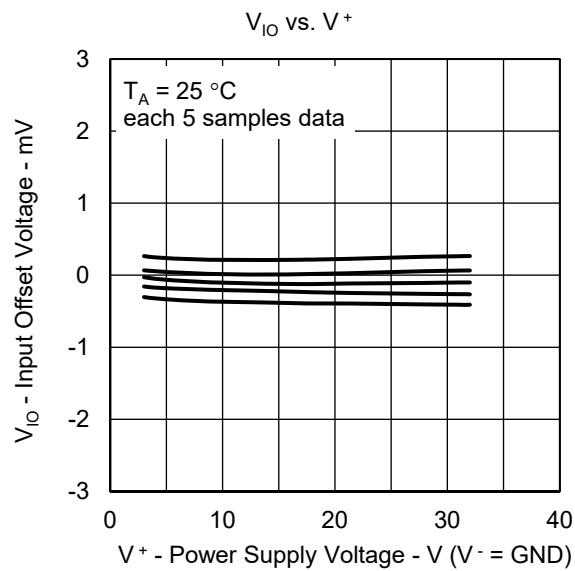
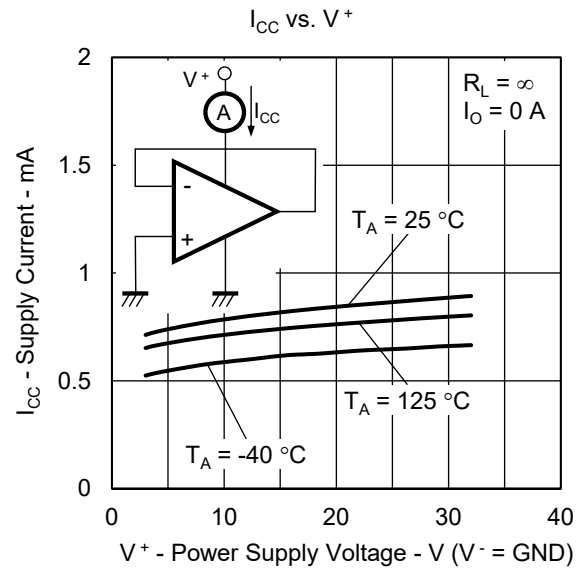
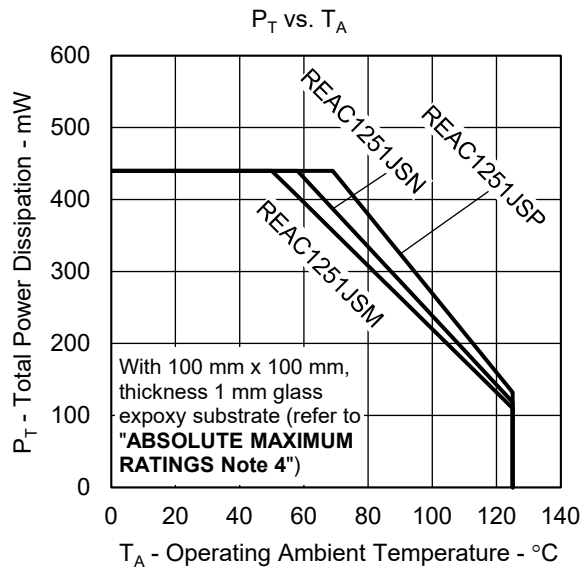
ELECTRICAL CHARACTERISTICS

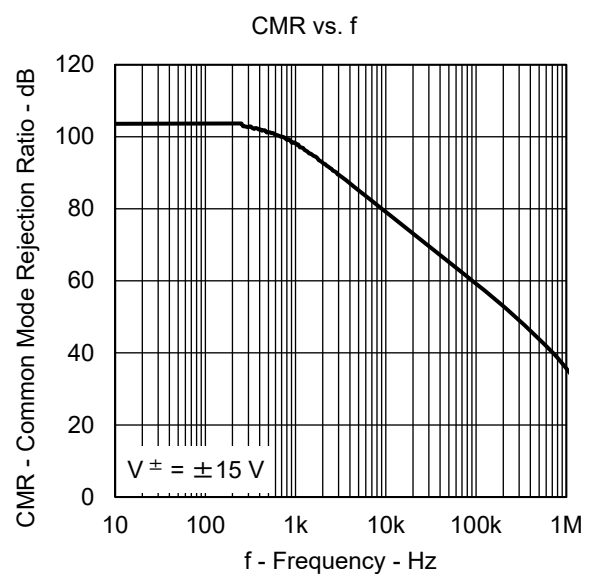
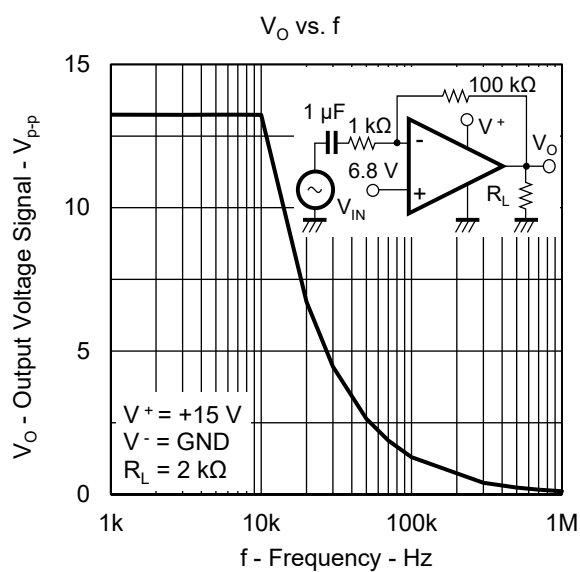
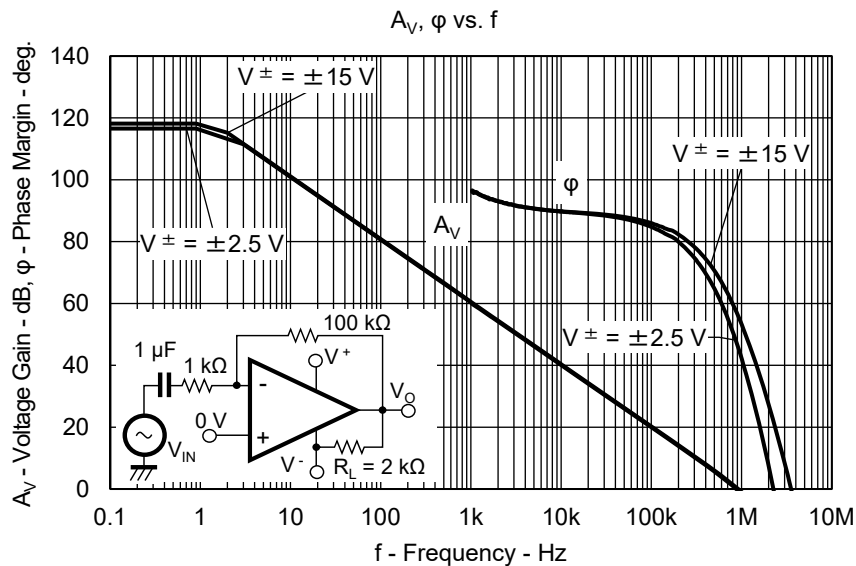
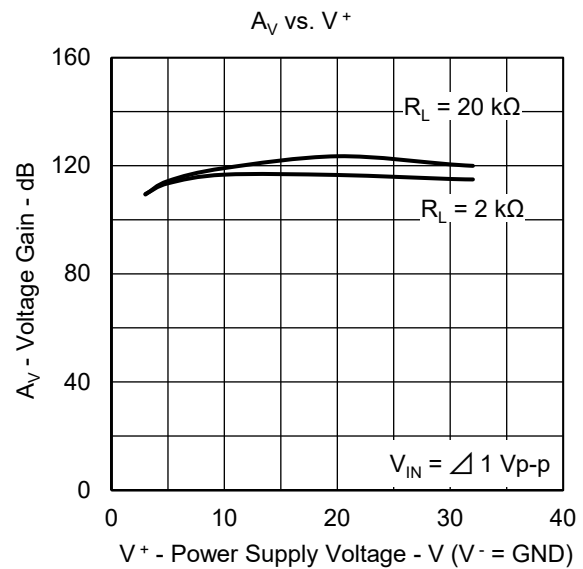
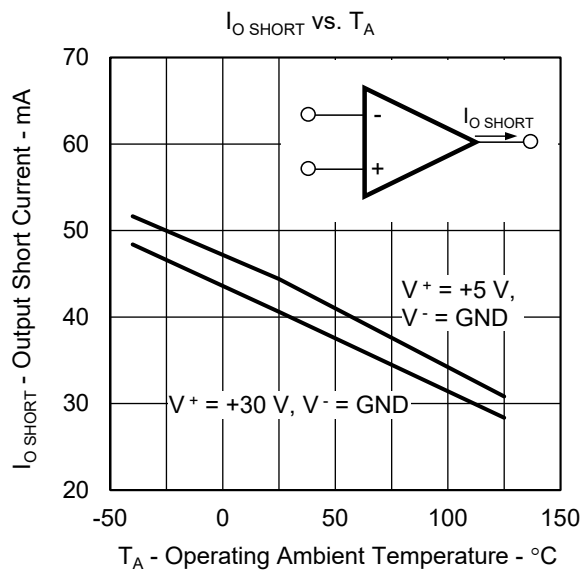
< $V^+ = +5\text{V}$, $V^- = \text{GND}$, $T_A = 25^\circ\text{C}$ >

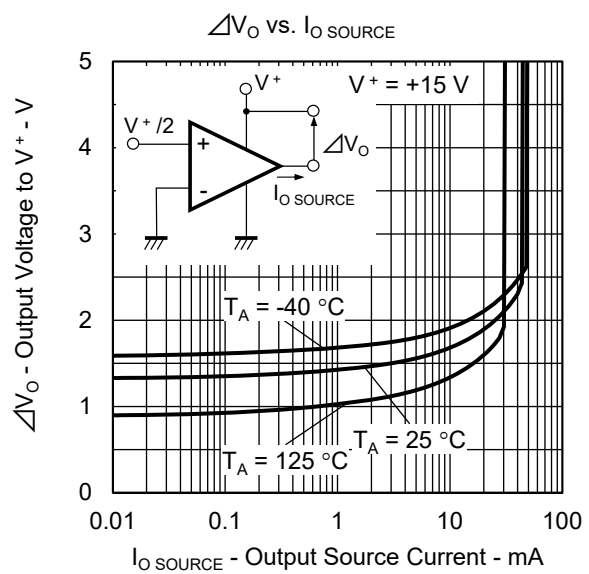
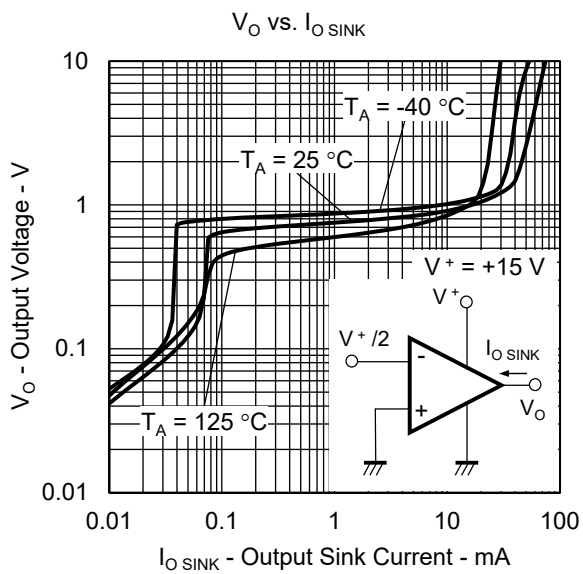
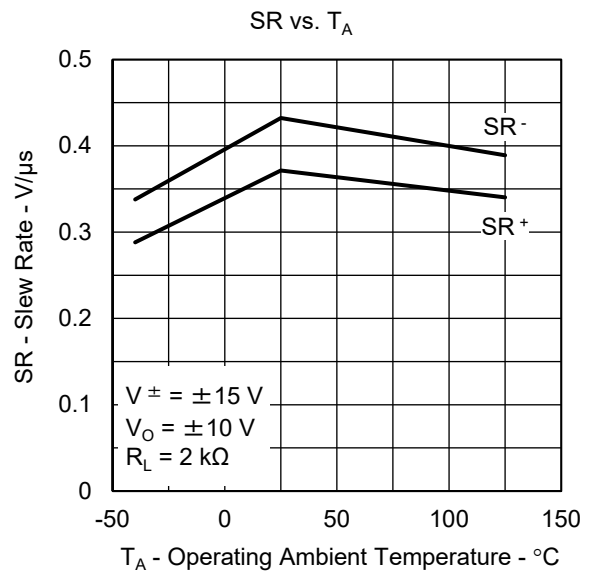
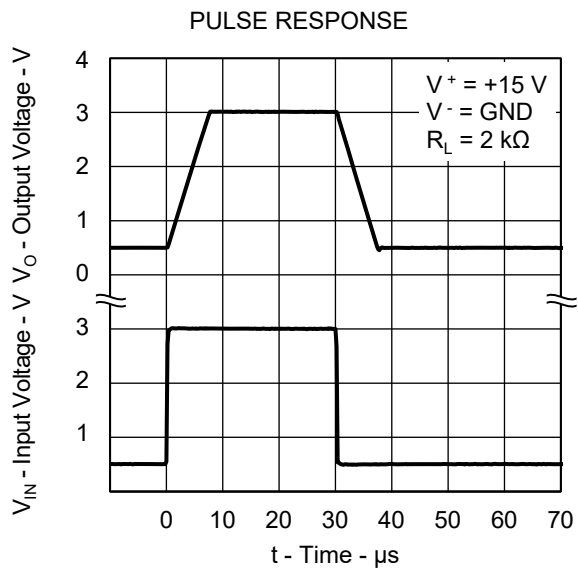
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Conditions
Input Offset Voltage	V_{IO}		± 0.5	± 1	mV	$V_{IN} = 1/2V_{CC}$ $R_S \leq 50\Omega$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$
Input Offset Current	I_{IO}		± 5	± 50	nA	
Input Bias Current ^{Note 6}	I_B		14	60	nA	
Large Signal Voltage Gain	A_V	25,000	100,000			$R_L \geq 2\text{k}\Omega$ (Connect to GND)
Supply Current ^{Note 7}	I_{CC}		0.7	1.4	mA	$R_L = \infty$, $I_O = 0\text{A}$
Common Mode Rejection Ratio	CMR	65	85		dB	
Supply Voltage Rejection Ratio	SVR	65	100		dB	
Common Mode Input Voltage Range	V_{ICM}	0		$V^+ - 1.5$	V	
Output Voltage Swing	V_O	0		$V^+ - 1.6$	V	$R_L = 2\text{k}\Omega$ (Connect to GND)
Output Current (Source)	$I_{O \text{ SOURCE}}$	20	40		mA	$V_{IN}^+ = +1\text{V}$, $V_{IN}^- = 0\text{V}$
Output Current (Sink)	$I_{O \text{ SINK1}}$	10	20		mA	$V_{IN}^- = +1\text{V}$, $V_{IN}^+ = 0\text{V}$
	$I_{O \text{ SINK2}}$	12	50		μA	$V_{IN}^- = +1\text{V}$, $V_{IN}^+ = 0\text{V}$, $V_O = 200\text{mV}$
Channel Separation			120		dB	$f = 1\text{kHz}$ to 20kHz

Note 6. The input bias current flows in the direction where the IC flows out because the first stage is configured with a PNP transistor.

7. This is a current that flows in the internal circuit. This current will flow irrespective of the channel used.

TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, TYP.) (Reference value)



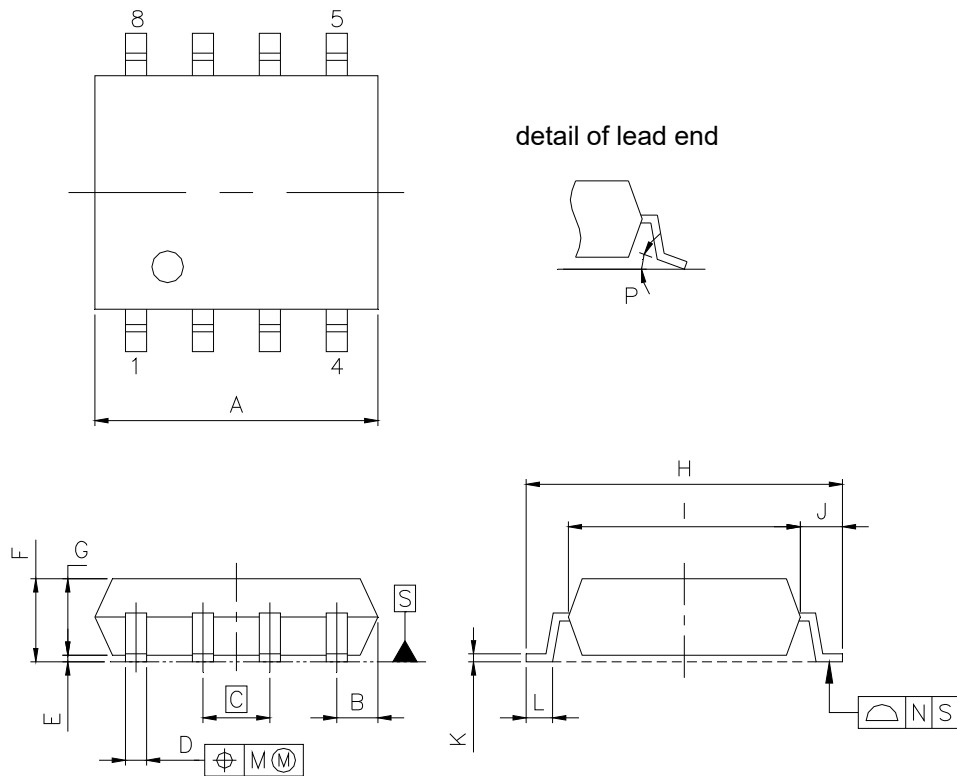


PACKAGE DRAWINGS

8-PIN PLASTIC SOP

JEITA Package code	RENESAS code	Previous code	MASS (TYP.) [g]
P-SOP8-0225-1.27	PRSP0008DL-A	S8GM-50-225B	0.08

Unit : mm

**NOTE**

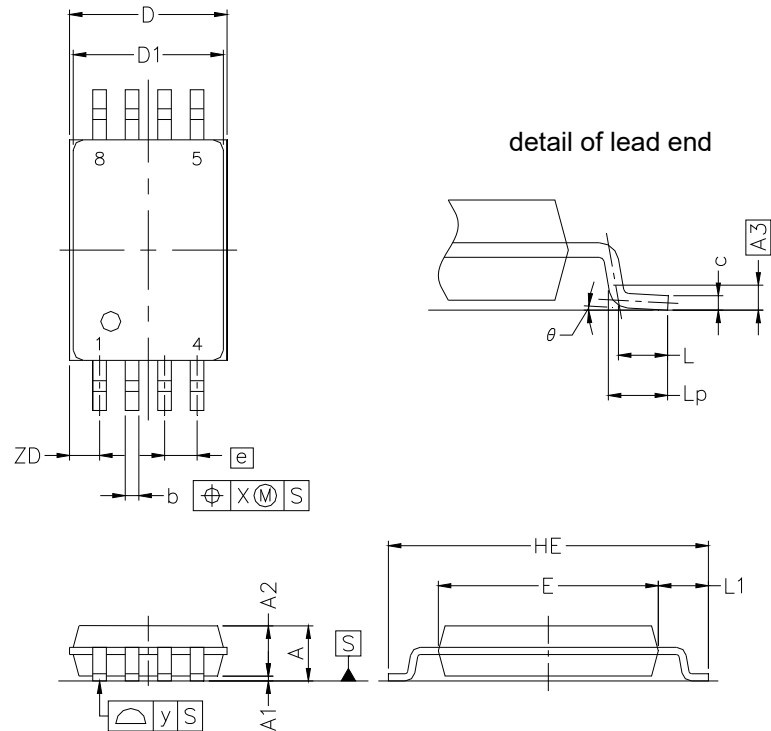
Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	5.2 $^{+0.17}_{-0.20}$
B	0.78 MAX
C	1.27 (T.P.)
D	0.42 $^{+0.08}_{-0.07}$
E	0.1 ± 0.1
F	1.59 ± 0.21
G	1.49
H	6.5 ± 0.3
I	4.4 ± 0.15
J	1.1 ± 0.2
K	0.17 $^{+0.08}_{-0.07}$
L	0.6 ± 0.2
M	0.12
N	0.10
P	3° $^{+7°}_{-3°}$

8-PIN PLASTIC TSSOP

JEITA Package code	RENESAS code	Previous code	MASS(TYP.) [g]
P-TSSOP8-0225-0.65	PTSP0008JD-A	P8GR-65-9LG	—

Unit : mm

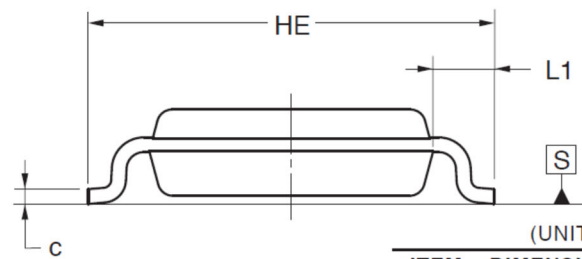
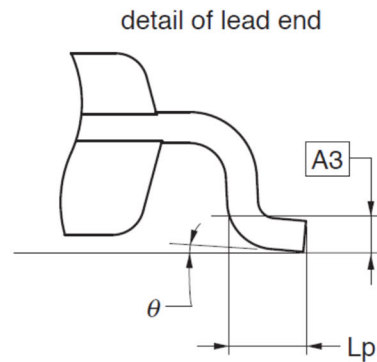
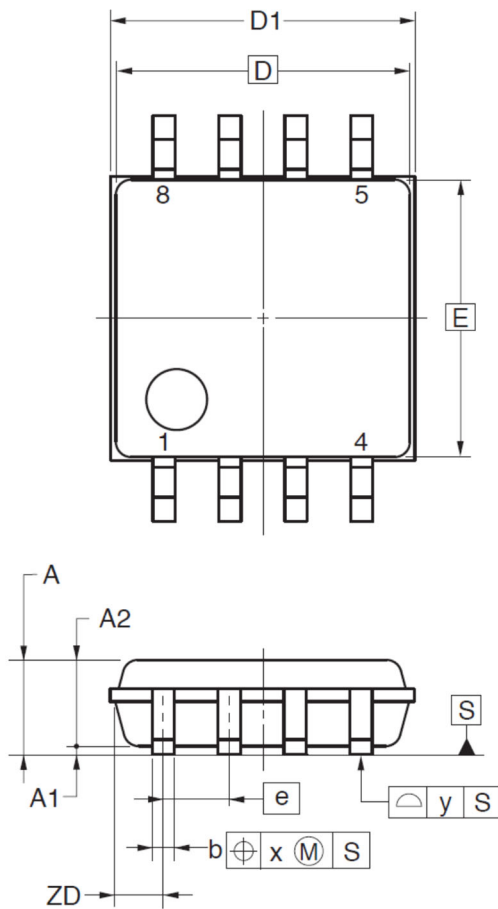
**NOTE**

Each lead centerline is located within 0.10 mm of its true position at maximum material condition.

ITEM	MILLIMETERS
D	3.15 ±0.15
D1	3.00 ±0.10
E	4.40 ±0.10
HE	6.40 ±0.20
A	1.20 MAX.
A1	0.10 ±0.05
A2	1.00 ±0.05
A3	0.25
b	0.24 ^{+0.06} _{-0.05}
c	0.145 ±0.055
L	0.5
Lp	0.60 ±0.15
L1	1.00 ±0.20
θ	3° ^{+5°} _{-3°}
e	0.65
x	0.10
y	0.10
ZD	0.60

8-PIN PLASTIC MSOP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-TSSOP8-2.8x2.9-0.65	PTSP0008JF-A	P8MP-65-KAA-1	0.02



(UNIT:mm)

ITEM	DIMENSIONS
D	2.90
D1	3.00 ± 0.20
E	2.80
HE	4.00 ± 0.20
e	0.65
b	0.22 ± 0.05
A	1.03 MAX.
A1	0.08 ± 0.05
A2	0.85 ± 0.05
A3	0.25
L1	0.60 ± 0.20
c	0.145 ^{+0.05} _{-0.03}
Lp	0.37 ± 0.10
x	0.10
y	0.10
θ	3° ^{+5°} _{-3°}
ZD	0.525

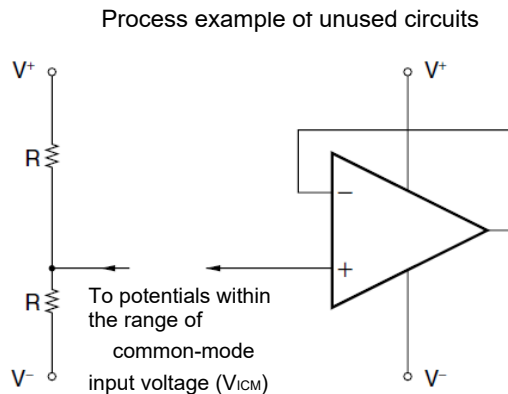
NOTE

Each lead centerline is located within 0.10 mm of its true position at maximum material condition.

PRECAUTIONS FOR USE

○The process of unused circuits

If there is an unused circuit, the following connection is recommended.



Remark A midpoint potential of V^+ and V^- is applied to this example.

○Ratings of input/output pin voltage

When the voltage of input/output pin exceeds the absolute maximum rating, it may cause degradation of characteristics or damages, by a conduction of a parasitic diode within an IC. In addition, when the input pin may be lower than V^- , or the output pin may exceed the power supply voltage, it is recommended to make a clamp circuit by a diode whose forward voltage is low (e.g.: Schottky diode) for protection.

○Range of common-mode input voltage

When the supply voltage does not meet the condition of electrical characteristics, the range of common-mode input voltage is as follows.

V_{ICM} (TYP.): V^- to $V^+ - 1.5$ (V) ($T_A = 25^\circ\text{C}$).

During designing, do include some tolerance by considering temperature characteristics and etc.

○The maximum output voltage

The range of the TYP. value of the maximum output voltage when the supply voltage does not meet the condition of electrical characteristics is as follows:

V_{OM+} (TYP.): $V^+ - 1.6$ [V] ($T_A = 25^\circ\text{C}$),

V_{OM-} (TYP.): ($I_{O\text{ SINK}} \leq 50 \mu\text{A}$): Approx. V^- (V) ($T_A = 25^\circ\text{C}$)

During designing, consider variations in characteristics and temperature characteristics for use with allowance. In addition, also note that the output voltage range ($V_{OM+} - V_{OM-}$) becomes narrow when an output current increases.

○Operation of output

This IC consist an output level of a class C push-pull. Therefore, when a load resistance is connected to the midpoint potential of V^+ , V^- , a crossover distortion occurs at the transition state of output current flow direction (source, sink).

○Handling of ICs

When stress is added to ICs due to warpage or bending of a board, the characteristic fluctuates due to piezoelectric effect. Therefore, pay attention to warpage or bending of a board.

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- 虽然瑞萨电子一直致力于提高瑞萨电子产品的质量和可靠性，但是，半导体产品有其自身的具体特性，如一定的故障发生率以及在某些使用条件下会发生故障等。除非是瑞萨电子产品数据表或其他瑞萨电子文档中指定为高可靠性产品或用于恶劣环境的导线，否则瑞萨电子产品未进行防辐射设计，以避免因瑞萨电子产品失效或发生故障而造成身体伤害、火灾导致伤害或损害和/或其他对公众构成危险事故。例如进行软硬件安全设计（包括但不限于冗余设计、防火控制以及故障预防等）、适当的老化处理或其他适当的措施等。由于对微机电软件单独进行评估非常困难且不实际，所以请用户自行负责最终产品或系统进行安全评估。
- 关于环境保护方面的详细内容，例如每种瑞萨电子产品的环境兼容性等，请与瑞萨电子的营业部门联系。用户负责仔细并充分查阅对管制物质的使用或含量进行管理的所有适用法律法规（包括但不限于《欧盟RoHS指令》），并在使用瑞萨电子产品时遵守所有适用法律法规。对于因用户未遵守相应法律法规而导致的损害或损失，瑞萨电子概不承担任何责任。
- 不可将瑞萨电子产品和技术用于或者嵌入日本国内或海外相应的法律法规所禁止生产、使用及销售的任何产品或系统中。也不可将瑞萨电子产品和技术用于(1)与大规模杀伤性武器（例如核武器、化学武器、生物武器或运送此类武器的导弹，包括无人机(UAV)）的开发、设计、制造、使用、存储等相关的任何目的；(2)与常规武器的开发、设计、制造或使用相关的任何目的；(3)扰乱国际和平与安全的任何其他目的，并且不可向任何第三方销售、出口、租赁、转让、或让与瑞萨电子产品或技术，无论直接或间接知悉或者有理由知悉该第三方或任何其他方将从从事上述活动。用户必须遵守对方或交易行司法管辖权的任意国家、地区政府所公布和管理的任何适用出口管制法律法规。
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(Rev.4.0-1 November 2017)



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