ISL28134

5V Ultra Low Noise, Auto-Zero Rail-to-Rail Precision Op Amp

FN6957
Rev.6.03
Oct 27, 2022

The ISL28134 is a single, auto-zeroing operational amplifier optimized for single and dual supply operation from 2.25V to 6.0V and ±1.125V and ±3.0V. The ISL28134 uses auto-zeroing circuitry to provide very low input offset voltage, drift and a reduction of the 1/f noise corner below 0.1Hz. The ISL28134 achieves ultra low offset voltage, offset temperature drift, wide gain bandwidth and rail-to-rail input/output swing while minimizing power consumption.

The ISL28134 is ideal for amplifying the sensor signals of analog front-ends that include pressure, temperature, medical, strain gauge and inertial sensors down to the µV levels.

The ISL28134 can be used over standard amplifiers with high stability across the industrial temperature range of -40°C to +85°C and the full industrial temperature range of -40°C to +125°C. The ISL28134 is available in an industry standard pinout SOIC and SOT-23 packages.

Applications

- Medical instrumentation
- Sensor gain amps
- Precision low drift, low frequency ADC drivers
- Precision voltage reference buffers
- Thermopile, thermocouple, and other temperature sensors front-end amplifiers
- Inertial sensors
- Process control systems
- Weight scales and strain gauge sensors

Features

- Rail-to-rail inputs and outputs
  - CMRR at V_{CM} = 0.1V beyond V_S . . . . . 135dB, typ
  - V_{OH} and V_{OL} . . . . . .10mV from V_S, typ
- No 1/f noise corner down to 0.1Hz
  - Input noise voltage . . . . . .10nV/√Hz at 1kHz
  - 0.1Hz to 10Hz noise voltage. . . . . 250nV_{P-P}
- Low offset voltage . . . . . 2.5µV, Max
- Superb offset drift . . . . . 15nV/°C, Max
- Single supply . . . . . 2.25V to 6.0V
- Dual supply . . . . . ±1.125V to ±3.0V
- Low I_{CC} . . . . . 675µA, typ
- Wide bandwidth 3.5MHz
- Operating temperature range
  - Industrial . . . . . .-40°C to +85°C
  - Full industrial . . . . . .-40°C to +125°C
- Packaging
  - Single: SOIC, SOT-23

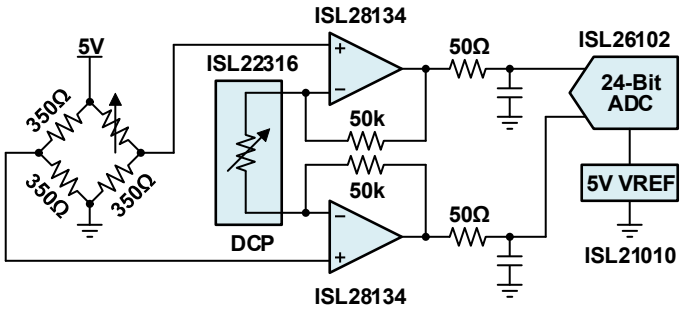


FIGURE 1. PRECISION WEIGH SCALE / STRAIN GAUGE

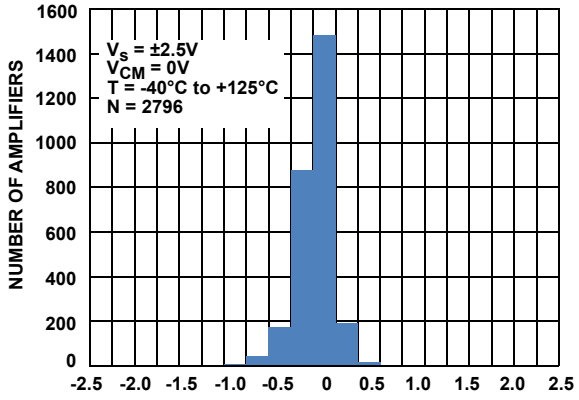
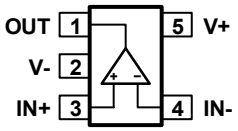


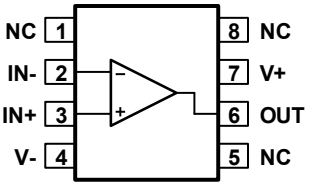
FIGURE 2. V_{OS} HISTOGRAM V_S = 5V

Pin Configurations

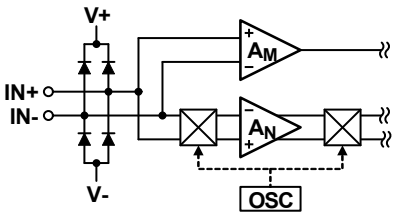
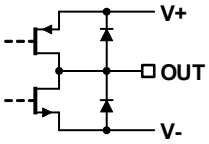
5 LD SOT-23
TOP VIEW



8 LD SOIC
TOP VIEW



Pin Descriptions

ISL28134 (8 Ld SOIC)	ISL28134 (5 Ld SOT-23)	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
2	4	IN-	Inverting input	(See Circuit 1)
3	3	IN+	Non-inverting input	 Circuit 1
4	2	V-	Negative supply	
6	1	OUT	Output	 Circuit 2
7	5	V+	Positive supply	
1, 5, 8	-	NC	No Connect	Pin is floating. No connection made to IC.

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	PACKAGE DESCRIPTION (RoHS Compliant)	PKG. DWG. #	CARRIER TYPE (Note 1)	TEMP RANGE
ISL28134IBZ	28134 IBZ	8 Ld SOIC	M8.15E	Tube	-40°C to +85°C
ISL28134IBZ-T13				Reel, 2.5k	
ISL28134IBZ-T7				Reel, 1k	
ISL28134IBZ-T7A				Reel, 250	
ISL28134FHZ-T7	BEEA (Note 4)	5 Ld SOT-23	P5.064A	Reel, 3k	-40°C to +125°C
ISL28134FHZ-T7A				Reel, 250	
ISL28134ISENSEV1Z	Evaluation Board				
ISL28134SOICEVAL1Z	Evaluation Board				

NOTES:

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL28134 device page. For more information about MSL, see TB363.
4. The part marking is located on the bottom of the part.

Absolute Maximum Ratings

Supply Voltage V+ to V- 6.5V
Voltage VIN to GND. . . . . (V- - 0.3V) to (V+ + 0.3V) V
Input Differential Voltage 6.5V
Input Current 20mA
Voltage VOUT to GND (10s) . . . . . (V+) or (V-)
dv/dt Supply Slew Rate 100V/µs
ESD Rating
Human Body Model (Tested per JED22-A114F) 4kV
Machine Model (Tested per JED22-A115B) 300V
Charged Device Model (Tested per JED22-C110D) 2kV
Latch-up (Passed Per JESD78B) . . . . . +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
5 Ld SOT-23 (Notes 5, 6)	225	116
8 Ld SOIC (Notes 5, 6)	125	77.2

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Operating Conditions

Ambient Operating Temperature Range
Industrial Grade Package . . . . . -40°C to +85°C
Full Industrial Grade Package. . . . . -40°C to +125°C
Operating Voltage Range . . . . . 2.25V (±1.125V) to 6V (±3V)

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See TB379 for details.
6. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

V_S = 5V, V_{CM} = 2.5V, T_A = +25°C, unless otherwise specified. **Boldface limits apply across the specified operating temperature range.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
DC SPECIFICATIONS						
V_{OS}	Input Offset Voltage		-2.5	-0.2	2.5	µV
		T_A = -40°C to +85°C	**-3.4**	-	**3.4**	µV
		T_A = -40°C to +125°C	**-4**	-	**4**	µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient	T_A = -40°C to +125°C	**-15**	-0.5	**15**	nV/°C
I_B	Input Bias Current		-300	±120	300	pA
		T_A = -40°C to +85°C	**-300**	-	**300**	pA
		T_A = -40°C to +125°C	**-550**	-	**550**	pA
TCI_B	Input Bias Current Temperature Coefficient	T_A = -40°C to +85°C	**-**	±1.4	**-**	pA/°C
		T_A = -40°C to +125°C	**-**	±2	**-**	pA/°C
I_{OS}	Input Offset Current		-600	±240	600	pA
		T_A = -40°C to +85°C	**-600**	-	**600**	pA
		T_A = -40°C to +125°C	**-750**	-	**750**	pA
TCI_{OS}	Input Offset Current Temperature Coefficient	T_A = -40°C to +85°C	**-**	±2.8	**-**	pA/°C
		T_A = -40°C to +125°C	**-**	±4	**-**	pA/°C
Common Mode Input Voltage Range		V+ = 5.0V, V- = 0V Guaranteed by CMRR	**-0.1**	-	**5.1**	V
CMRR	Common Mode Rejection Ratio	V_{CM} = -0.1V to 5.1V	120	135	-	dB
		V_{CM} = -0.1V to 5.1V	**115**	-	-	dB
PSRR	Power Supply Rejection Ratio	V_S = 2.25V to 6.0V	120	135	-	dB
		V_S = 2.25V to 6.0V	**120**	-	-	dB
V_S	Supply Voltage (V+ to V-)	Guaranteed by PSRR	**2.25**	-	**6.0**	V

Electrical Specifications V_S = 5V, V_{CM} = 2.5V, T_A = +25°C, unless otherwise specified. **Boldface limits apply across the specified operating temperature range. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
I_S	Supply Current Per Amplifier	R_L = OPEN	-	675	900	µA
		R_L = OPEN T_A = -40°C to +85°C	**-**	-	**1075**	µA
		R_L = OPEN T_A = -40°C to +125°C	**-**	-	**1150**	µA
I_{SC}	Short Circuit Output Source Current	R_L = Short to V-	-	65	-	mA
	Short Circuit Output Sink Current	R_L = Short to V+	-	-65	-	mA
V_{OH}	Output Voltage Swing, HIGH From V_{OUT} to V_+	R_L = 10kΩ to V_{CM}	15	10	-	mV
		R_L = 10kΩ to V_{CM}	**15**	-	-	mV
V_{OL}	Output Voltage Swing, LOW From V_- to V_{OUT}	R_L = 10kΩ to V_{CM}	-	10	15	mV
		R_L = 10kΩ to V_{CM}	-	-	**15**	mV
A_{OL}	Open Loop Gain	R_L = 1MΩ	-	174	-	dB
AC SPECIFICATIONS						
C_{IN}	Input Capacitance	Differential	-	5.2	-	pF
		Common Mode	-	5.6	-	pF
e_N	Input Noise Voltage	f = 0.1Hz to 10Hz	-	250	400	nV_{P-P}
		f = 10Hz	-	8	-	nV/√Hz
		f = 1kHz	-	10	-	nV/√Hz
I_N	Input Noise Current	f = 1kHz	-	200	-	fA/√Hz
GBWP	Gain Bandwidth Product		-	3.5	-	MHz
EMIRR	EMI Rejection Ratio	A_V = +1, V_{IN} = 200mV_{p-p}, V_{CM} = 0V, V+ = 2.5V, V- = -2.5V	-	75	-	dB
TRANSIENT RESPONSE						
SR	Positive Slew Rate	V+ = 5V, V- = 0V, V_{OUT} = 1V to 3V, R_L = 100kΩ, C_L = 3.7pF	-	1.5	-	V/µs
	Negative Slew Rate		-	1.0	-	V/µs
t_r, t_f, Small Signal	Rise Time, t_r 10% to 90%	V+ = 5V, V- = 0V, V_{OUT} = 0.1V_{P-P}, R_F = 0Ω, R_L = 100kΩ, C_L = 3.7pF	-	0.07	-	µs
	Fall Time, t_f 10% to 90%		-	0.17	-	µs
t_r, t_f Large Signal	Rise Time, t_r 10% to 90%	V+ = 5V, V- = 0V, V_{OUT} = 2V_{P-P}, R_F = 0Ω, R_L = 100kΩ, C_L = 3.7pF	-	1.3	-	µs
	Fall Time, t_f 10% to 90%		-	2.0	-	µs
t_s	Settling Time to 0.1%, 2V_{P-P} Step	A_V = -1, R_F = 1kΩ, C_L = 3.7pF	-	100	-	µs
$t_{recover}$	Output Overload Recovery Time, Recovery to 90% of Output Saturation	A_V = +2, R_F = 10kΩ, R_L = 100k, C_L = 3.7pF	-	3.1	-	µs

Electrical Specifications

V_S = 2.5V, V_{CM} = 1.25V, T_A = +25°C, unless otherwise specified. **Boldface limits apply over the specified operating temperature range.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
DC SPECIFICATIONS						
V_{OS}	Input Offset Voltage		-2.5	-0.2	2.5	µV
		T_A = -40°C to +85°C	**-3.4**	-	**3.4**	µV
		T_A = -40°C to +125°C	**-4**	-	**4**	µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient	T_A = -40°C to +125°C	**-15**	-0.5	**15**	nV/°C
I_B	Input Bias Current		-300	±120	300	pA
		T_A = -40°C to +85°C	**-300**	-	**300**	pA
		T_A = -40°C to +125°C	**-550**	-	**550**	pA
TCI_B	Input Bias Current Temperature Coefficient	T_A = -40°C to +85°C	**-**	±1.4	**-**	pA/°C
		T_A = -40°C to +125°C	**-**	±2	**-**	pA/°C
I_{OS}	Input Offset Current		-600	±240	600	pA
		T_A = -40°C to +85°C	**-600**	-	**600**	pA
		T_A = -40°C to +125°C	**-750**	-	**750**	pA
TCI_{OS}	Input Offset Current Temperature Coefficient	T_A = -40°C to +85°C	**-**	±2.8	**-**	pA/°C
		T_A = -40°C to +125°C	**-**	±4	**-**	pA/°C
Common Mode Input Voltage Range		V+ = 2.5V, V- = 0V Guaranteed by CMRR	**-0.1**	-	**2.6**	V
CMRR	Common Mode Rejection Ratio	V_{CM} = -0.1V to 2.6V	120	135	-	dB
		V_{CM} = -0.1V to 2.6V	**115**	-	-	dB
I_S	Supply Current per Amplifier	R_L = OPEN	-	715	940	µA
		R_L = OPEN T_A = -40°C to +85°C	**-**	-	**1115**	µA
		R_L = OPEN T_A = -40°C to +125°C	**-**	-	**1190**	µA
I_{SC}	Short Circuit Output Source Current	R_L = Short to Ground	-	65	-	mA
	Short Circuit Output Sink Current	R_L = Short to V+	-	-65	-	mA
V_{OH}	Output Voltage Swing, HIGH From V_{OUT} to V_+	R_L = 10kΩ to V_{CM}	15	10	-	mV
		R_L = 10kΩ to V_{CM}	**15**	-	-	mV
V_{OL}	Output Voltage Swing, LOW From V_- to V_{OUT}	R_L = 10kΩ to V_{CM}	-	10	15	mV
		R_L = 10kΩ to V_{CM}	-	-	**15**	mV
AC SPECIFICATIONS						
C_{IN}	Input Capacitance	Differential	-	5.2	-	pF
		Common Mode	-	5.6	-	pF
e_N	Input Noise Voltage	f = 0.1Hz to 10Hz	-	250	400	nV_{P-P}
		f = 10Hz	-	8	-	nV/√Hz
		f = 1kHz	-	10	-	nV/√Hz
I_N	Input Noise Current	f = 1kHz	-	200	-	fA/√Hz
GBWP	Gain Bandwidth Product		-	3.5	-	MHz

Electrical Specifications

V_S = 2.5V, V_{CM} = 1.25V, T_A = +25°C, unless otherwise specified. **Boldface limits apply over the specified operating temperature range. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
TRANSIENT RESPONSE						
SR	Positive Slew Rate	V+ = 2.5V, V- = 0V, V_{OUT} = 0.25V to 2.25V, R_L = 100kΩ, C_L = 3.7pF	-	1.5	-	V/µs
	Negative Slew Rate		-	1.0	-	V/µs
t_r, t_f, Small Signal	Rise Time, t_r 10% to 90%	V+ = 2.5V, V- = 0V, V_{OUT} = 0.1V_{P-P}, R_F = 0Ω, R_L = 100kΩ, C_L = 3.7pF	-	0.07	-	µs
	Fall Time, t_f 10% to 90%		-	0.17	-	µs
t_r, t_f Large Signal	Rise Time, t_r 10% to 90%	V+ = 2.5V, V- = 0V, V_{OUT} = 2V_{P-P}, R_F = 0Ω, R_L = 100kΩ, C_L = 3.7pF	-	1.3	-	µs
	Fall Time, t_f 10% to 90%		-	2.0	-	µs
t_s	Settling Time to 0.1%, 2V_{P-P} Step	A_V = -1, R_F = 1kΩ, C_L = 3.7pF	-	100	-	µs
$t_{recover}$	Output Overload Recovery Time, Recovery to 90% of Output Saturation	A_V = +2, R_F = 10kΩ, R_L = 100k, C_L = 3.7pF	-	1.5	-	µs

NOTE:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves

T_A = +25°C, V_{CM} = 0V Unless otherwise specified.

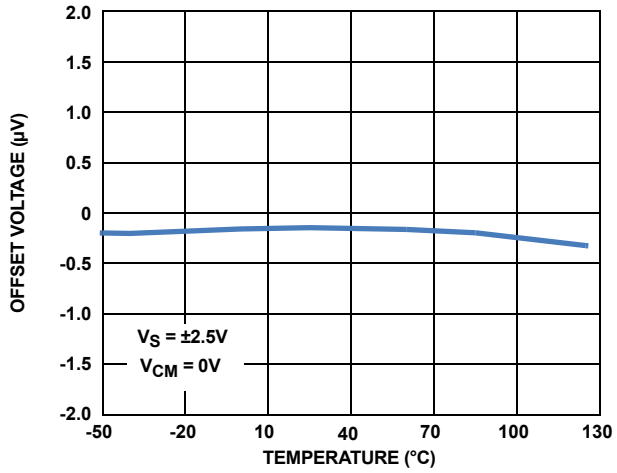


FIGURE 3. V_{OS} vs TEMPERATURE, V_S = ±2.5V

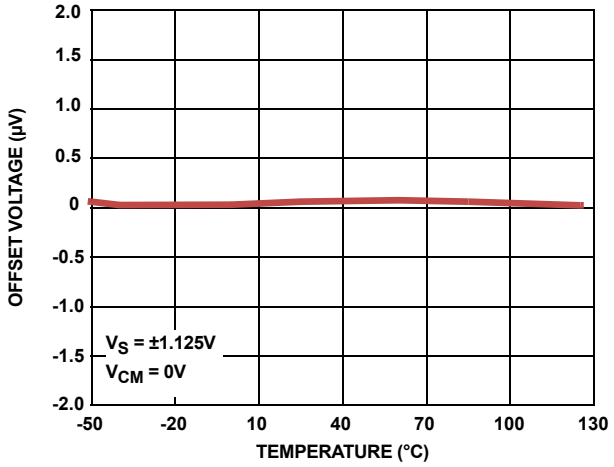


FIGURE 4. V_{OS} vs TEMPERATURE, V_S = ±1.125V

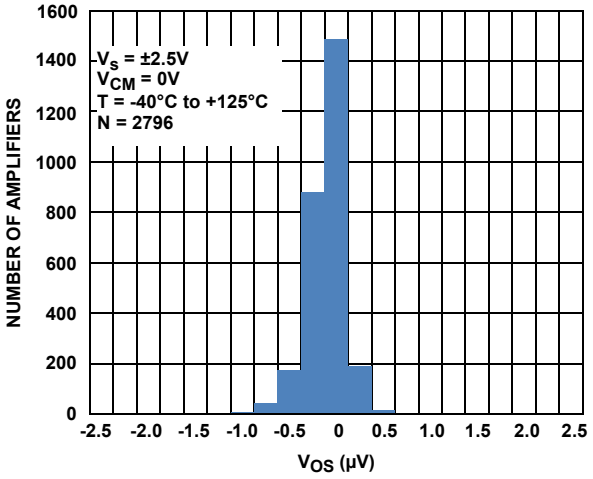


FIGURE 5. V_{OS} HISTOGRAM V_S = 5V

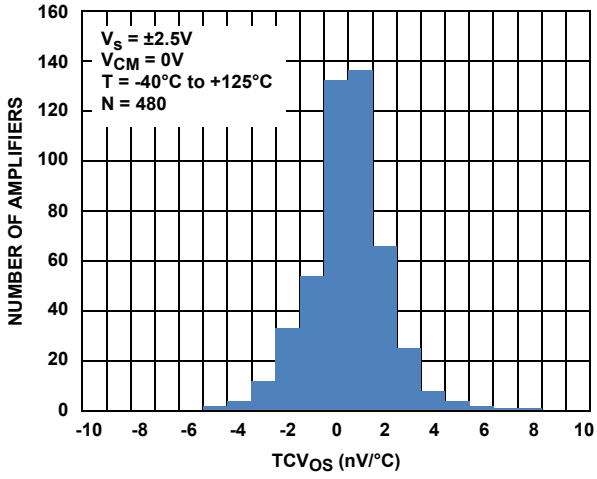


FIGURE 6. TCV_{OS} HISTOGRAM V_S = 5V

Typical Performance Curves T_A = +25°C, V_{CM} = 0V Unless otherwise specified. **(Continued)**

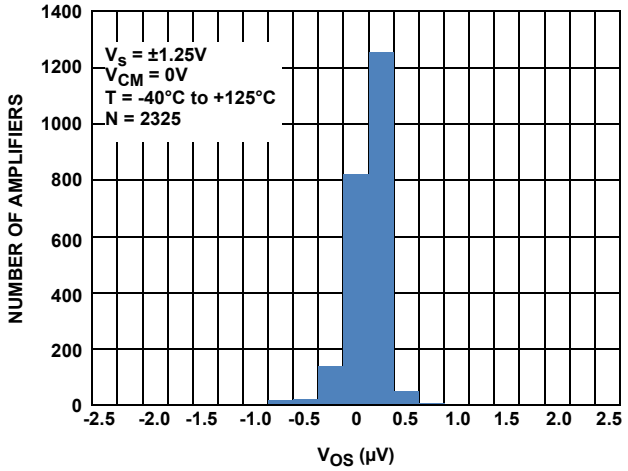


FIGURE 7. V_{OS} HISTOGRAM V_S = 2.5V

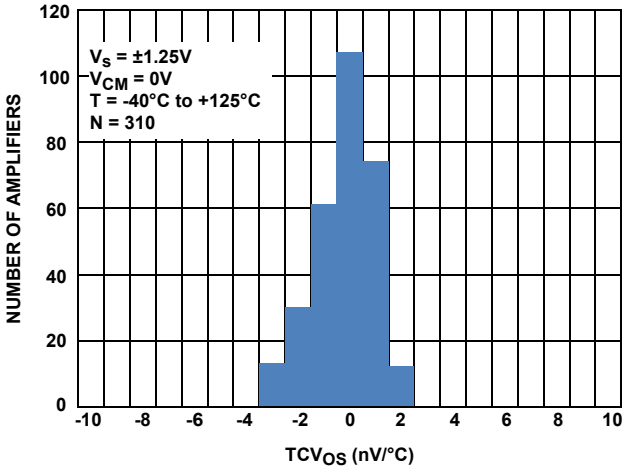


FIGURE 8. TCV_{OS} HISTOGRAM V_S = 2.5V

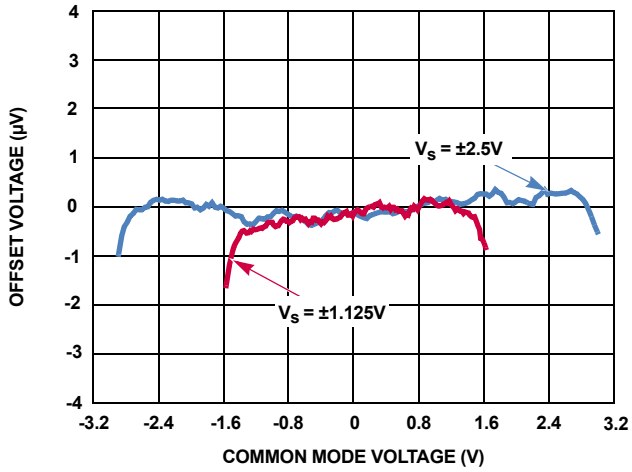


FIGURE 9. V_{OS} vs V_{CM}

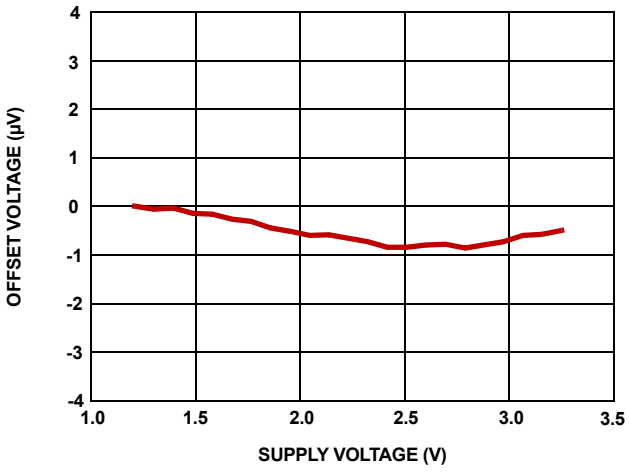


FIGURE 10. V_{OS} vs SUPPLY VOLTAGE

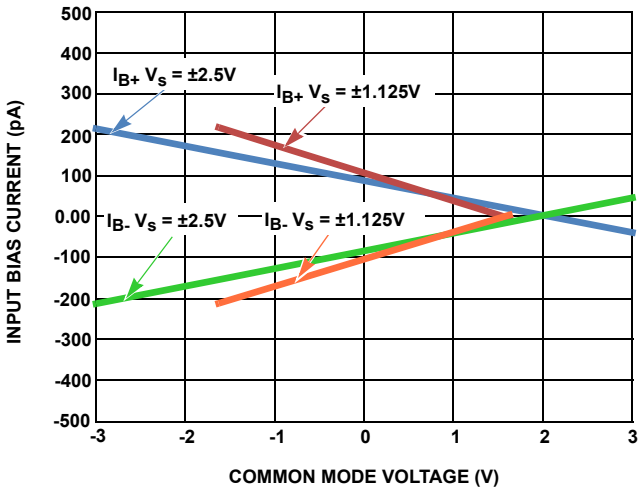


FIGURE 11. I_B vs V_{CM}

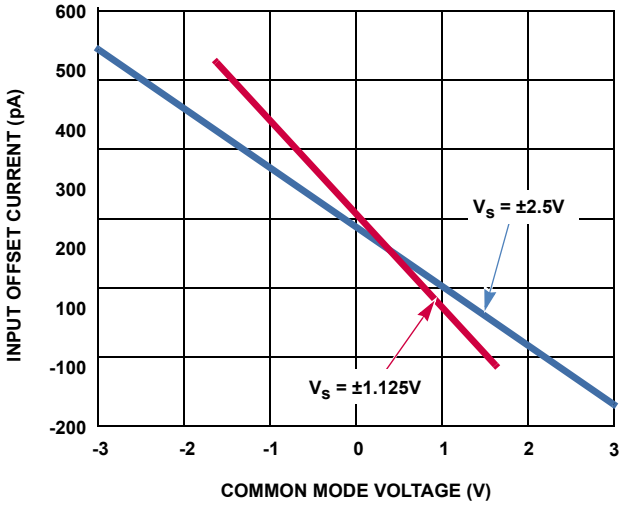


FIGURE 12. I_{OS} vs V_{CM}

Typical Performance Curves T_A = +25°C, V_{CM} = 0V Unless otherwise specified. **(Continued)**

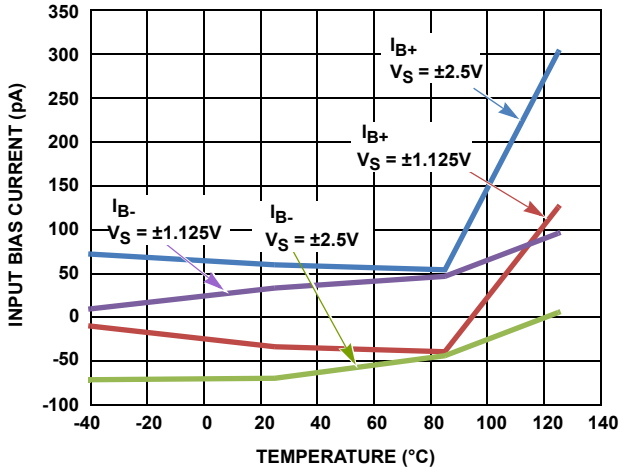


FIGURE 13. I_B vs TEMPERATURE

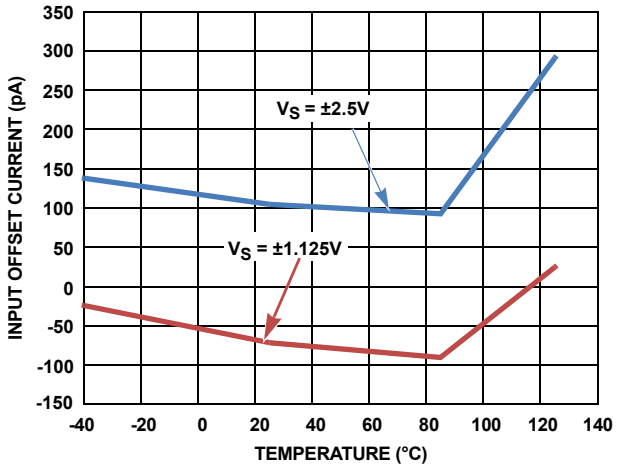


FIGURE 14. I_{OS} vs TEMPERATURE

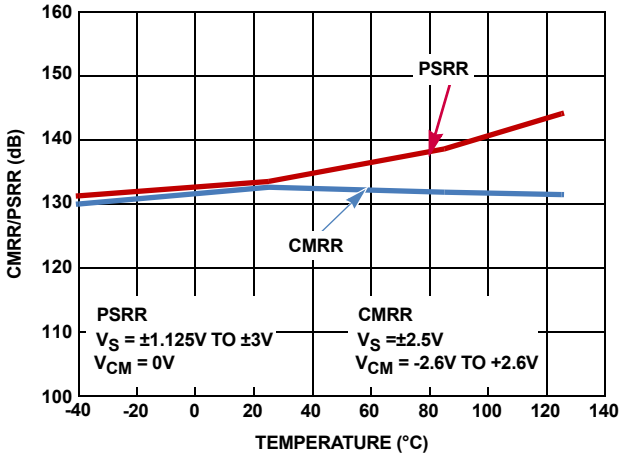


FIGURE 15. CMRR and PSRR vs TEMPERATURE

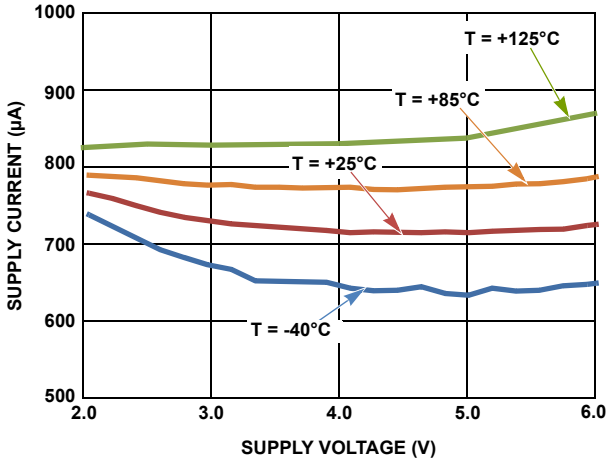


FIGURE 16. SUPPLY CURRENT vs SUPPLY VOLTAGE

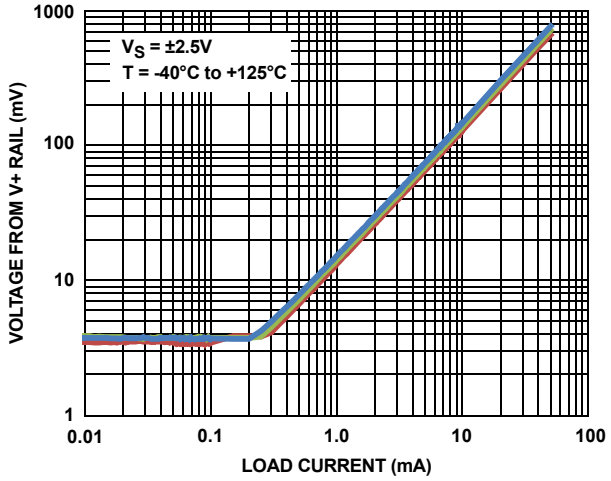


FIGURE 17. OUTPUT HIGH OVERHEAD VOLTAGE vs LOAD CURRENT

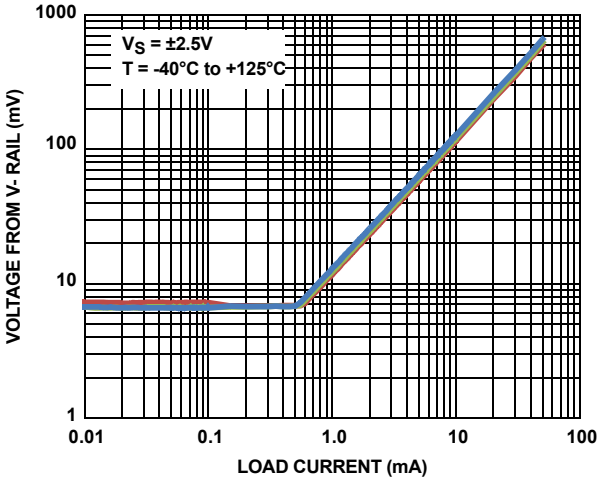


FIGURE 18. OUTPUT LOW OVERHEAD VOLTAGE vs LOAD CURRENT

Typical Performance Curves T_A = +25°C, V_{CM} = 0V Unless otherwise specified. **(Continued)**

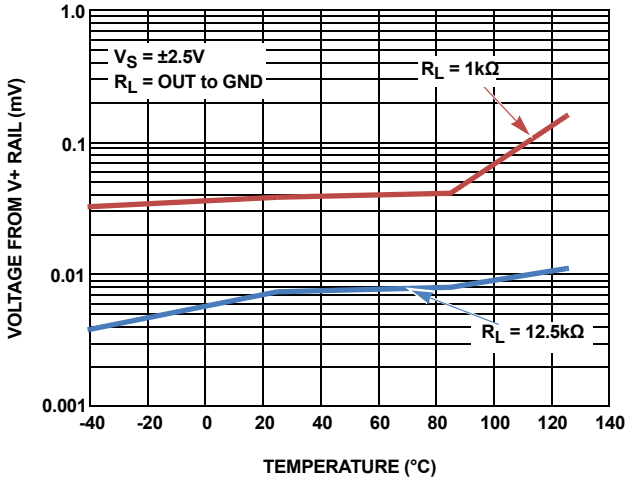


FIGURE 19. V_{OH} vs TEMPERATURE

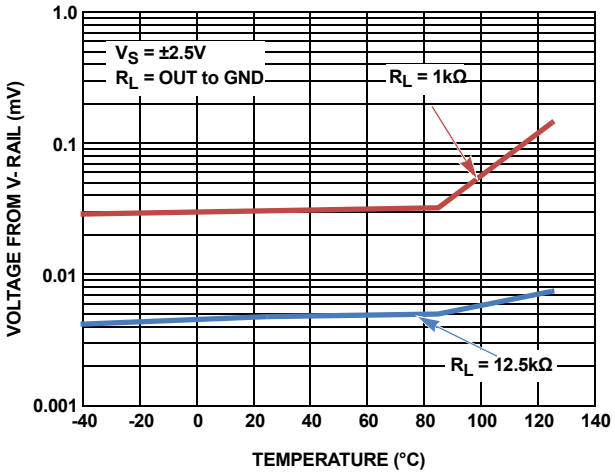


FIGURE 20. V_{OL} vs TEMPERATURE

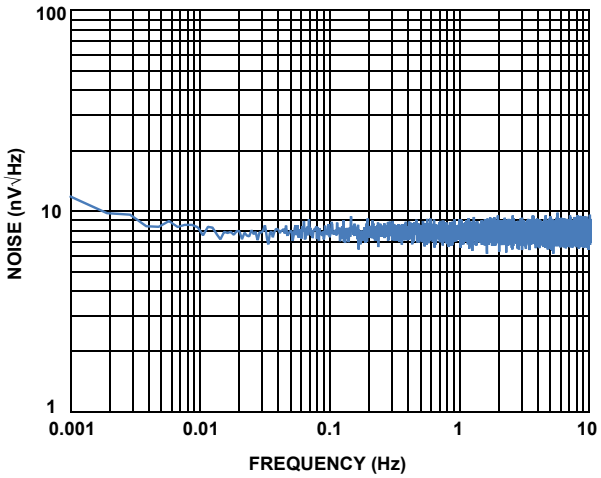


FIGURE 21. INPUT NOISE VOLTAGE DENSITY vs FREQUENCY

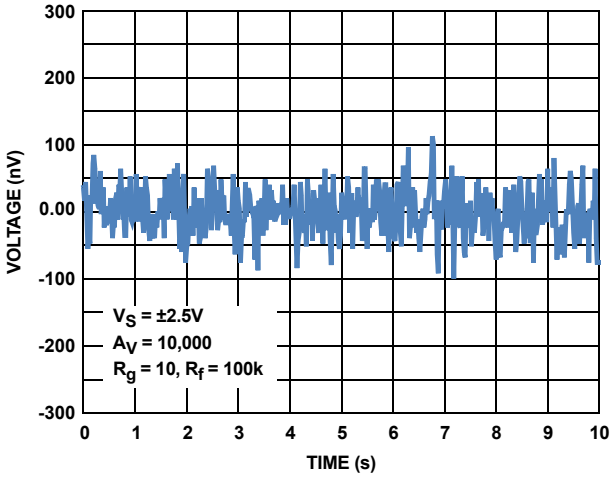


FIGURE 22. INPUT NOISE VOLTAGE 0.1Hz TO 10Hz

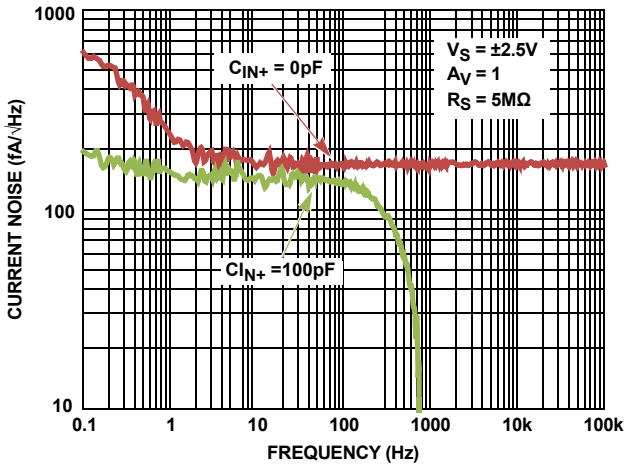


FIGURE 23. INPUT NOISE CURRENT DENSITY vs FREQUENCY

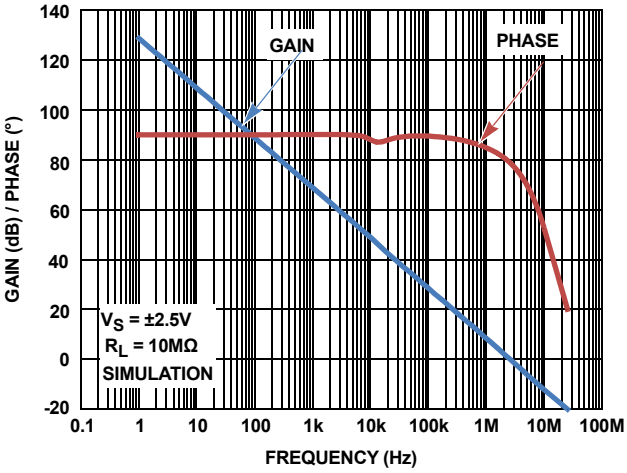


FIGURE 24. OPEN LOOP GAIN AND PHASE, R_L = 10M

Typical Performance Curves T_A = +25°C, V_{CM} = 0V Unless otherwise specified. **(Continued)**

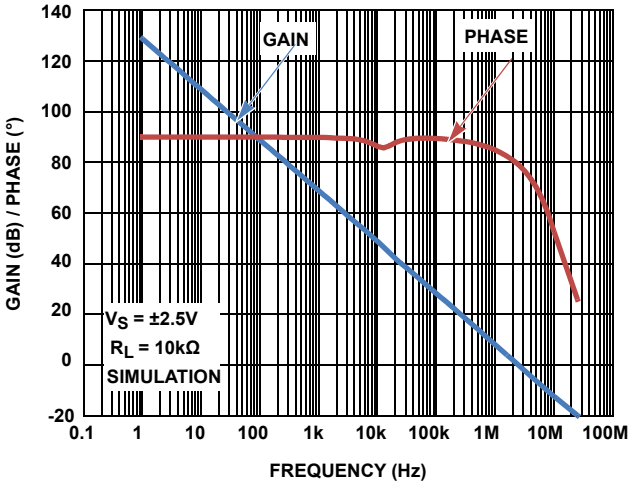


FIGURE 25. OPEN LOOP GAIN AND PHASE, R_L = 10k

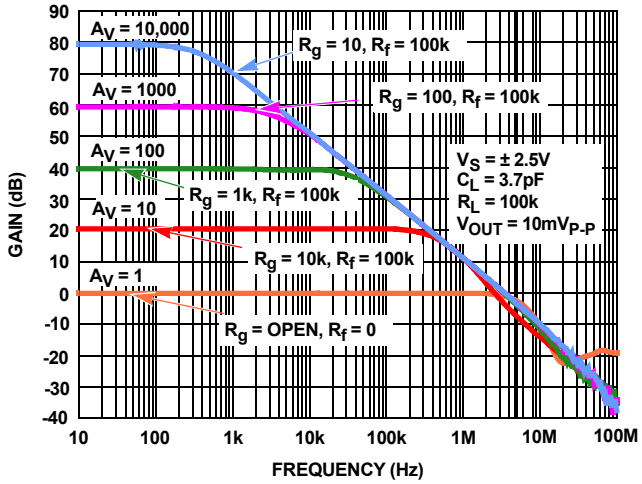


FIGURE 26. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

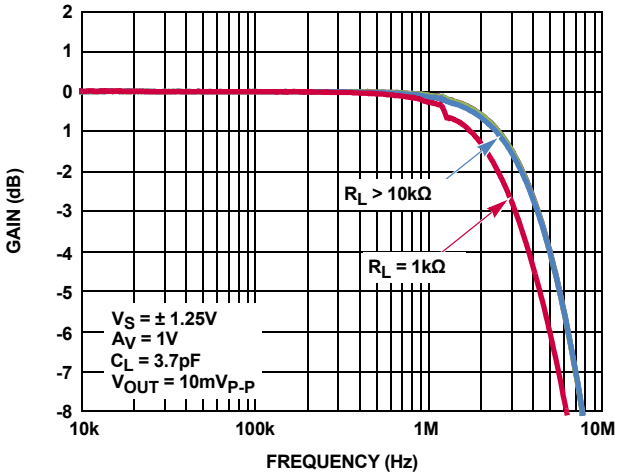


FIGURE 27. GAIN vs FREQUENCY vs R_L, V_S = 2.5V

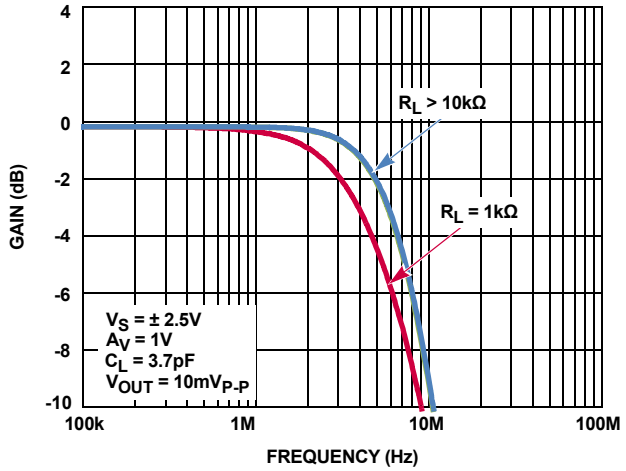


FIGURE 28. GAIN vs FREQUENCY vs R_L, V_S = 5.0V

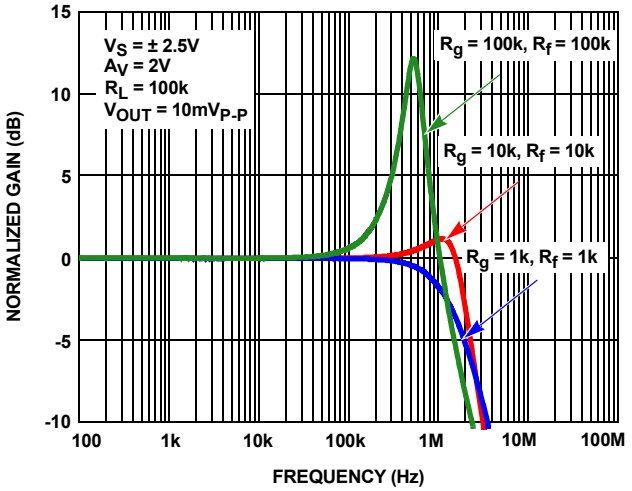


FIGURE 29. GAIN vs FREQUENCY vs FEEDBACK RESISTOR VALUES R_f/R_g

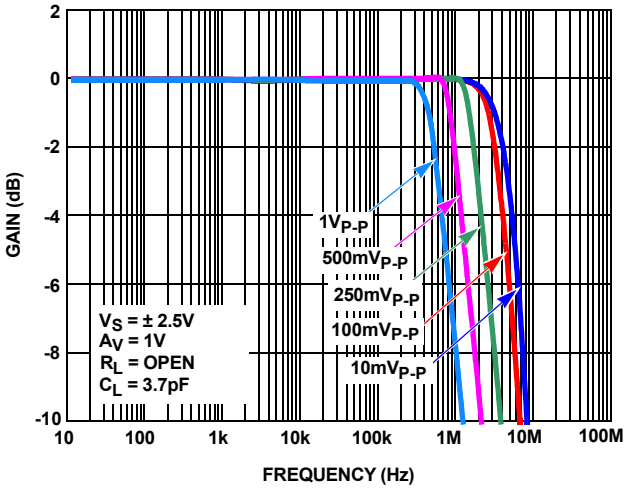


FIGURE 30. GAIN vs FREQUENCY vs V_{OUT}

Typical Performance Curves T_A = +25°C, V_{CM} = 0V Unless otherwise specified. **(Continued)**

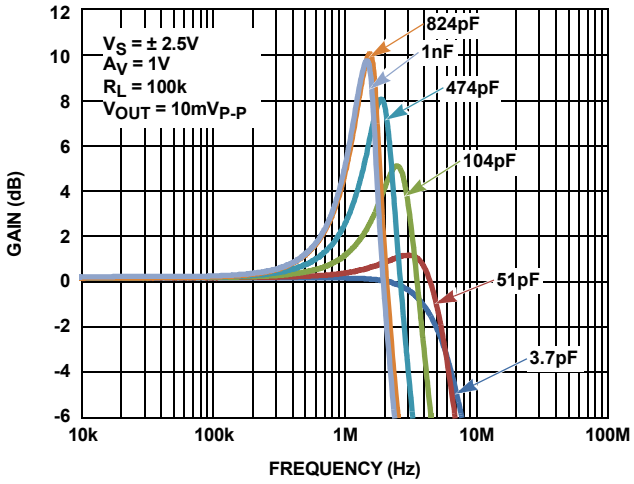


FIGURE 31. GAIN vs FREQUENCY vs C_L

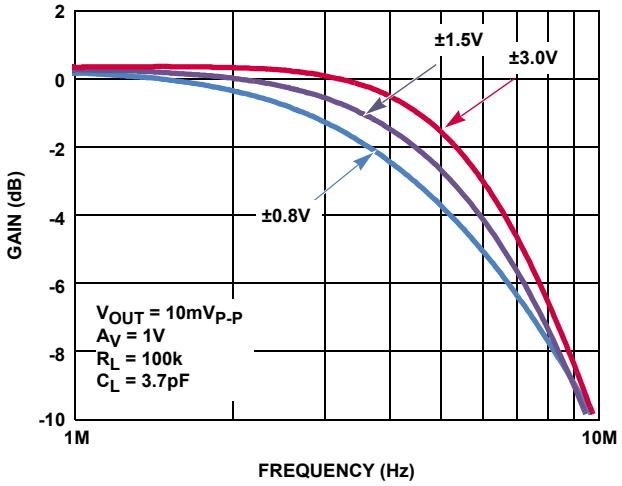


FIGURE 32. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

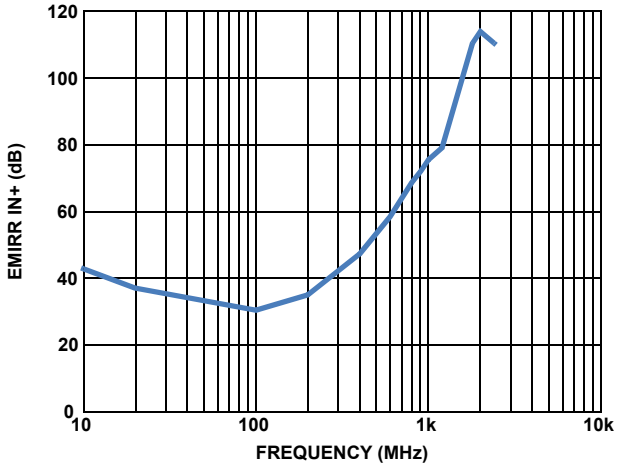


FIGURE 33. EMIRR AT IN+ PIN vs FREQUENCY

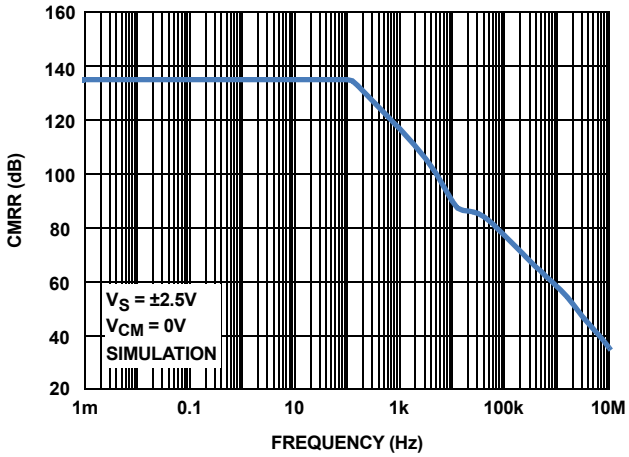


FIGURE 34. CMRR vs FREQUENCY, V_S = 5V

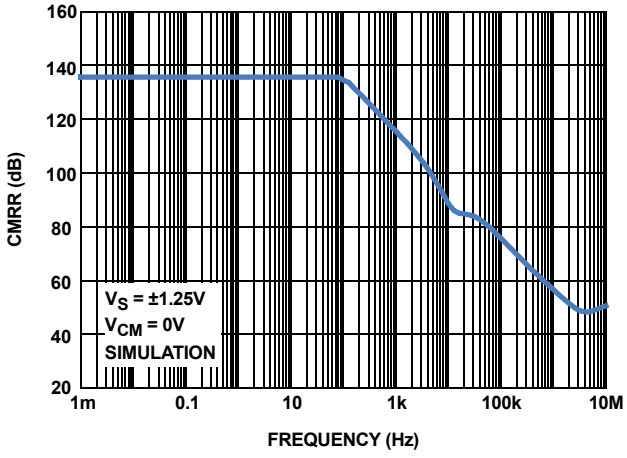


FIGURE 35. CMRR vs FREQUENCY, V_S = 2.5V

Typical Performance Curves $T_A = +25°C$, $V_{CM} = 0V$ Unless otherwise specified. **(Continued)**

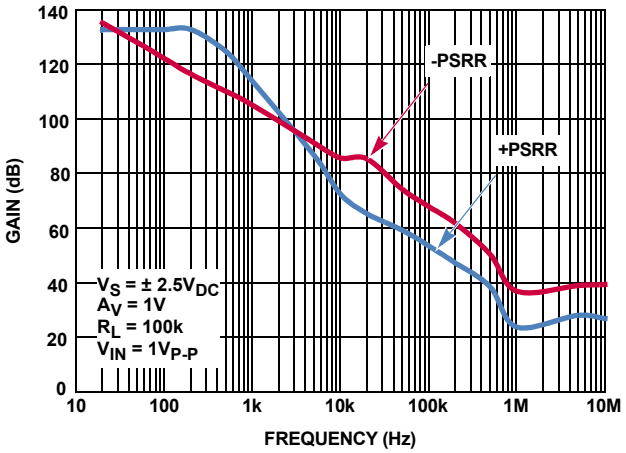


FIGURE 36. PSRR vs FREQUENCY, V_S = 5V

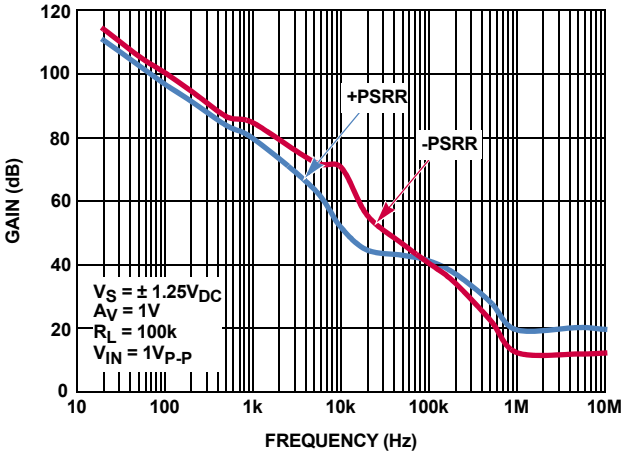


FIGURE 37. PSRR vs FREQUENCY, V_S = 2.5V

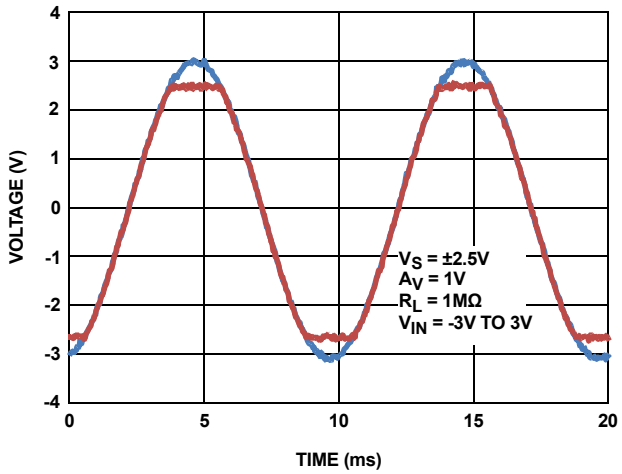


FIGURE 38. NO PHASE INVERSION

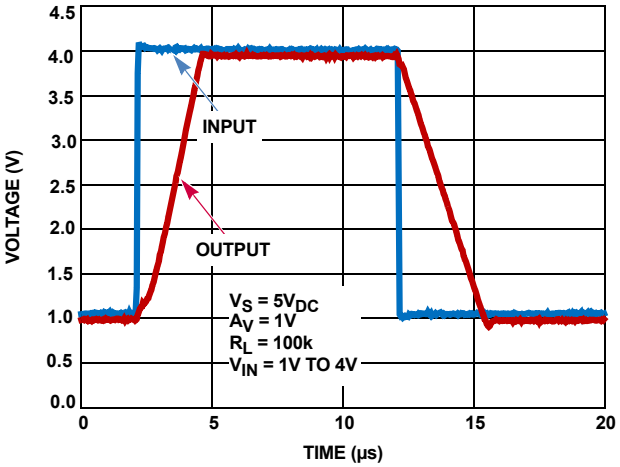


FIGURE 39. LARGE SIGNAL STEP RESPONSE (3V)

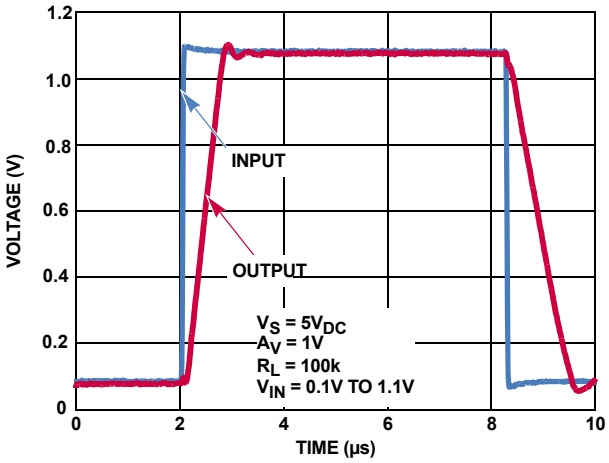


FIGURE 40. LARGE SIGNAL STEP RESPONSE (1V)

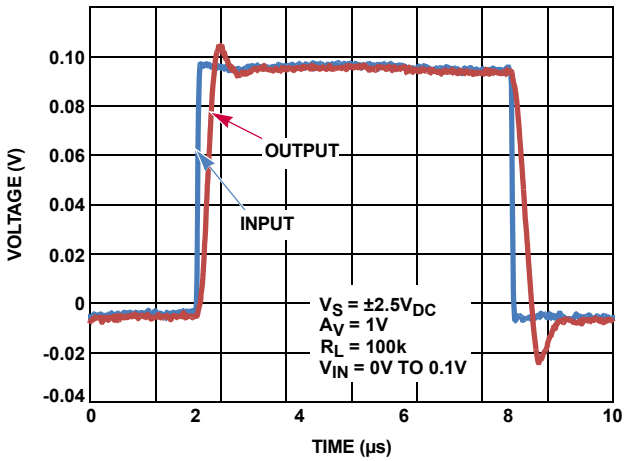


FIGURE 41. SMALL SIGNAL STEP RESPONSE (100mV)

Typical Performance Curves T_A = +25°C, V_{CM} = 0V Unless otherwise specified. **(Continued)**

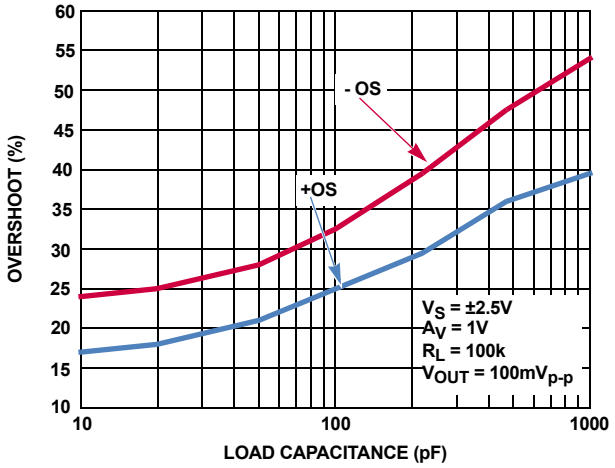


FIGURE 42. SMALL SIGNAL OVERSHOOT vs LOAD CAPACITANCE, VS = ±2.5V

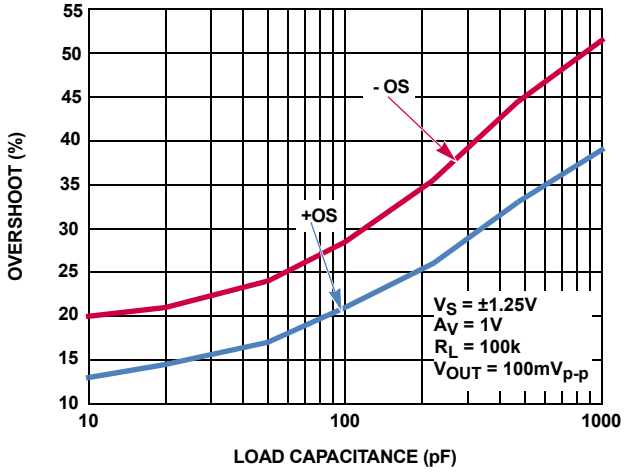


FIGURE 43. SMALL SIGNAL OVERSHOOT vs LOAD CAPACITANCE, V_S = ±1.25V

Applications Information

Functional Description

The ISL28134 is a single 5V rail-to-rail input/output amplifier that operates on a single or dual supply. The ISL28134 uses a proprietary auto-zeroing technique that combines a 3.5MHz main amplifier with a very high open loop gain (174dB) offset-nulling amplifier to achieve very low offset voltage and drift (0.2µV, 0.5nV/°C) while having a low supply current (675µA). The very low 1/f noise corner <0.1Hz and low input noise voltage (8nV/√Hz at 100Hz) of the amplifier makes it ideal for low frequency precision applications requiring very high gain and low noise.

This multi-path amplifier architecture contains a time continuous main amplifier whose input DC offset is corrected by a parallel-connected, high gain offset-nulling DC correction amplifier operating at 100kHz. From DC to ~10kHz, both amplifiers are active with the DC offset correction active with most of the low frequency gain provided by the nulling amplifier. A 10kHz crossover filter cuts off the low frequency nulling amplifier path leaving the main amplifier active out to the -3dB frequency (3.5MHz GBWP).

The key benefits of this architecture for precision applications are rail-to-rail inputs/outputs, high open loop gain, low DC offset and temperature drift, low 1/f noise corner and low input noise voltage. The noise is virtually flat across the frequency range from a few MHz out to 100kHz, except for the narrow noise peak at the amplifier crossover frequency (10kHz).

Power Supply Considerations

The ISL28134 features a wide supply voltage operating range. The ISL28134 operates on single (+2.25V to +6.0V) or dual (±1.125 to ±3.0V) supplies. Power supply voltages greater than the +6.5V absolute maximum (specified in the "Absolute Maximum Ratings" on page 4) can permanently damage the device. Performance of the device is optimized for supply voltages greater than 2.5V. This makes the ISL28134 ideal for portable 3V battery applications that require the precision performance. It is highly recommended that a 0.01µF or larger high frequency decoupling capacitor is placed across the power supply pins of the IC to maintain high performance of the amplifier.

Rail-to-rail Input and Output (RRIO)

Unlike some amplifiers whose inputs may not be taken to the power supply rails or whose outputs may not drive to the supply rails, the ISL28134 features rail-to-rail inputs and outputs. This allows the amplifier inputs to have a wide common mode range (100mV beyond supply rails) while maintaining high CMRR (135dB) and maximizes the signal to noise ratio of the amplifier by having the V_{OH} and V_{OL} levels be at the V+ and V- rails, respectively.

Low Input Voltage Noise Performance

In precision applications, the input noise of the front end amplifier is a critical parameter. Combined with a high DC gain to amplify the small input signal, the input noise voltage will result in an output error in the amplifier. A $1µV_{P-P}$ input noise voltage with an amplifier gain of 10,000V/V will result in an output offset in the range of 10mV, which can be an unacceptable error source. With only $250nV_{P-P}$ at the input, along with a flat noise response down to 0.1Hz, the ISL28134 can amplify small input signals with minimal output error.

The ISL28134 has the lowest input noise voltage compared to other competitor's Auto-Zero amplifiers with similar supply currents (see Table 1). The overall input referred voltage noise of an amplifier can be expressed as a sum of the input noise voltage, input noise current of the amplifier and the Johnson noise of the gain-setting resistors used. The product of the input noise current and external feedback resistors along with the Johnson noise, increases the total output voltage noise as the value of the resistance goes up. For optimizing noise performance, choose lower value feedback resistors to minimize the effect of input noise current. Although the ISL28134 features a very low 200fA/√Hz input noise current, at source impedances >100kΩ, the input referred noise voltage will be dominated by the input current noise. Keep source input impedances under 10kΩ for optimum performance.

TABLE 1.

PART	VOLTAGE NOISE AT 100Hz	0.1Hz TO 10Hz PEAK-TO-PEAK VOLTAGE NOISE
Competitor A	22nV/√Hz	600nV$_{P-P}$
Competitor B	16nV/√Hz	260nV$_{P-P}$
Competitor C	90nV/√Hz	1500nV$_{P-P}$
ISL28134	8nV/√Hz	250nV$_{P-P}$

High Source Impedance Applications

The input stage of auto-zero amplifiers do not behave like conventional amplifier input stages. The ISL28134 uses switches that continually sample the nulling amplifier input at 100kHz to reduce the input offset to 1µV. The dynamic behavior of these switches induces a charge injection current to the input terminals of the amplifier. The charge injection current has a DC path to ground through the resistances seen at the input terminals of the amplifier. Higher input impedance cause an apparent shift in the input bias current of the amplifier. Input impedances larger than 10kΩ begin to have significant increases in the bias currents. To minimize the effect of impedance on input bias currents, an input resistance of <10kΩ is recommended.

Because the nulling amplifier has charge injection currents at each terminal, the input impedance should be balanced across each input (see Figure 44). The input impedance of the amplifier should be matched between the IN+ and IN- terminals to minimize total input offset current. Input offset currents show up as an additional output offset voltage, as shown in Equation 1:

$$V_{OSTOT} = V_{OS} - R_F * I_{OS} \quad \text{(EQ. 1)}$$

If the offset voltage of the amplifier is negative, the input offset currents will add to the total output offset. For a 10,000V/V gain amplifier using 1MΩ feedback resistor, a 500pA total input offset current will have an additional output offset voltage of 0.5mV. By keeping the input impedance low and balanced across the amplifier inputs, the input offset current is kept below 100pA, resulting in an offset voltage 0.1mV or less.

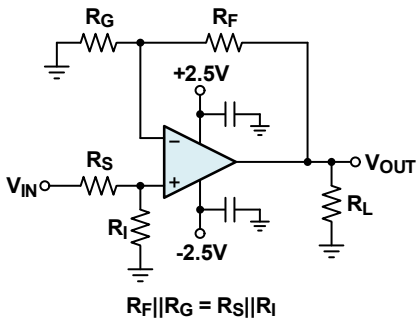


FIGURE 44. CIRCUIT IMPLEMENTATION FOR REDUCING INPUT BIAS CURRENTS

IN+ and IN- Protection

The ISL28134 is capable of driving the input terminals up to and beyond the supply rails by about 0.5V. Back biased ESD diodes from the input pins to the V+ and V- rails will conduct current when the input signals go more than 0.5V beyond the rail (see Figure 45). The ESD protection diodes must be current limited to 20mA or less to prevent damage of the IC. This current can be reduced by placing a resistor in series with the IN+ and IN- inputs in the event the input signals go beyond the rail.

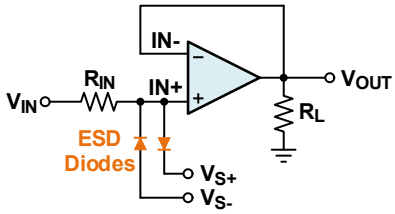


FIGURE 45. INPUT CURRENT LIMITING

EMI Rejection

Electromagnetic Interference (EMI) can be a problem in high frequency applications for precision amplifiers. The op amp pins are susceptible to EMI signals which can rectify high frequency inputs beyond the amplifier bandwidth and present itself as a shift in DC offset voltage. Long trace leads to op amp pins may act as an antenna for radiated RF signals, which result in a total conductive EMI noise into the op amp inputs.

The most susceptible pin is the non-inverting IN+ input therefore, EMI rejection (EMIR) on this pin is important for RF type applications. The ability of the amplifier output to reject EMI is called EMI Rejection Ratio (EMIRR) and is computed as:

$$EMIRR\ (dB) = 20 \log (V_{IN\_PEAK}/\Delta V_{OS})$$

The test circuit for measuring the DC offset of the amplifier with an RF signal input to the IN+ pin is shown in Figure 46. The EMIRR performance of the ISL28134 at the IN+ pin across a frequency of 10MHz to 2.4GHz is plotted on Figure 33. The ISL28134 shows a typical EMIRR of 75dB at 1GHz. For better EMI immunity, a small RFI filter can be placed at the input to attenuate out of band signals and reduce DC offset shift from high frequency RF signals into the IN+ pin. For example, a 15Ω and 100pF RC filter will roll off signals above 100MHz for better EMIRR performance.

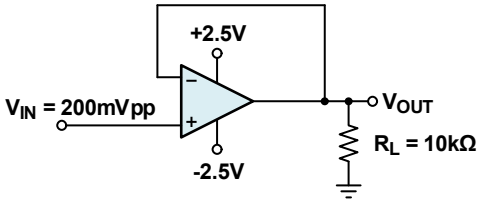


FIGURE 46. CIRCUIT TESTING EMIRR

Output Phase Reversal

The Output phase reversal is the unexpected inversion of the amplifier output signal when the inputs exceed the common mode input range. Since the ISL28134 is a rail-to-rail input amplifier, the ISL28134 is specifically designed to prevent output phase reversal within its common mode input range. In fact, the ISL28134 will not phase invert even when the input signals go 0.5V beyond the supply rails (see Figure 38). If input signals are expected to go beyond the rails, it is highly recommended to minimize the forward biased ESD diode current to prevent phase inversion by placing a resistor in series with the input.

High Gain, Precision DC-Coupled Amplifier

Precision applications that need to amplify signals in the range of a few µV require gain in the order of thousands of V/V to get a good signal to the Analog to Digital Converter (ADC). This can be achieved by using a very high gain amplifier with the appropriate open loop gain and bandwidth.

In addition to the high gain and bandwidth, it is important that the amplifier have low V_{OS} and temperature drift along with a low input noise voltage. For example, an amplifier with 100µV offset voltage and 0.5µV/°C offset drift configured in a closed loop gain of 10,000V/V would produce an output error of 1V and a 5mV/°C temperature dependent error. Unless offset trimming and temperature compensation techniques are used, this error makes it difficult to resolve the input voltages needed in the precision application.

The ISL28134 features a low V_{OS} of ±4µV max and a very stable 10nV/°C max temperature drift, which produces an output error of only ±40mV and a temperature error of 0.1mV/°C. With an ultra low input noise of 210nV_{P-P} (0.1Hz to 10Hz) and no 1/f corner frequency, the ISL28134 is capable of amplifying signals in the µV range with high accuracy. For even further DC precision, some feedback filtering C_F (see Figure 47) to reduce the noise can be implemented as a total signal stage amplifier. As a method of best practice, the ISL28134 should be impedance matched at the two input terminals. A balancing capacitor of the same value at the on-inverting terminal will result in the amplifier input impedances tracking across frequency

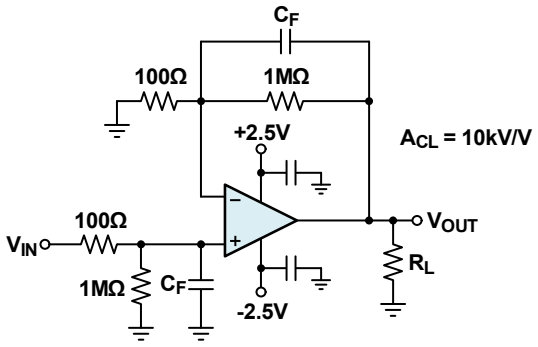


FIGURE 47. HIGH GAIN, PRECISION DC-COUPLED AMPLIFIER

ISL28134 SPICE Model

Figure 48 shows the SPICE model schematic and Figure 49 shows the net list for the SPICE model. The model is a simplified version of the actual device and simulates important AC and DC parameters. The AC parameters incorporated into the model are: 1/f and flat band noise voltage, slew rate, CMRR, and gain and phase. The DC parameters are I_{OS}, V_{OS}, total supply current, output voltage swing and output current limit (65mA). The model uses typical parameters given in the "Electrical Specifications" table beginning on page 4. The AVOL is adjusted for 174dB with the dominant pole at 6.5mHz. The CMRR is set at 135dB, f = 200Hz. The input stage models the actual device to present an accurate AC representation. The model is configured for an ambient temperature of +25°C.

Figures 50 through 63 show the characterization vs simulation results for the noise voltage, open loop gain phase, closed loop gain vs frequency, CMRR, large signal 3V step response, large signal 1V step response, and output voltage swing V_{OH}/V_{OL} ±2.5V supplies (no phase inversion).

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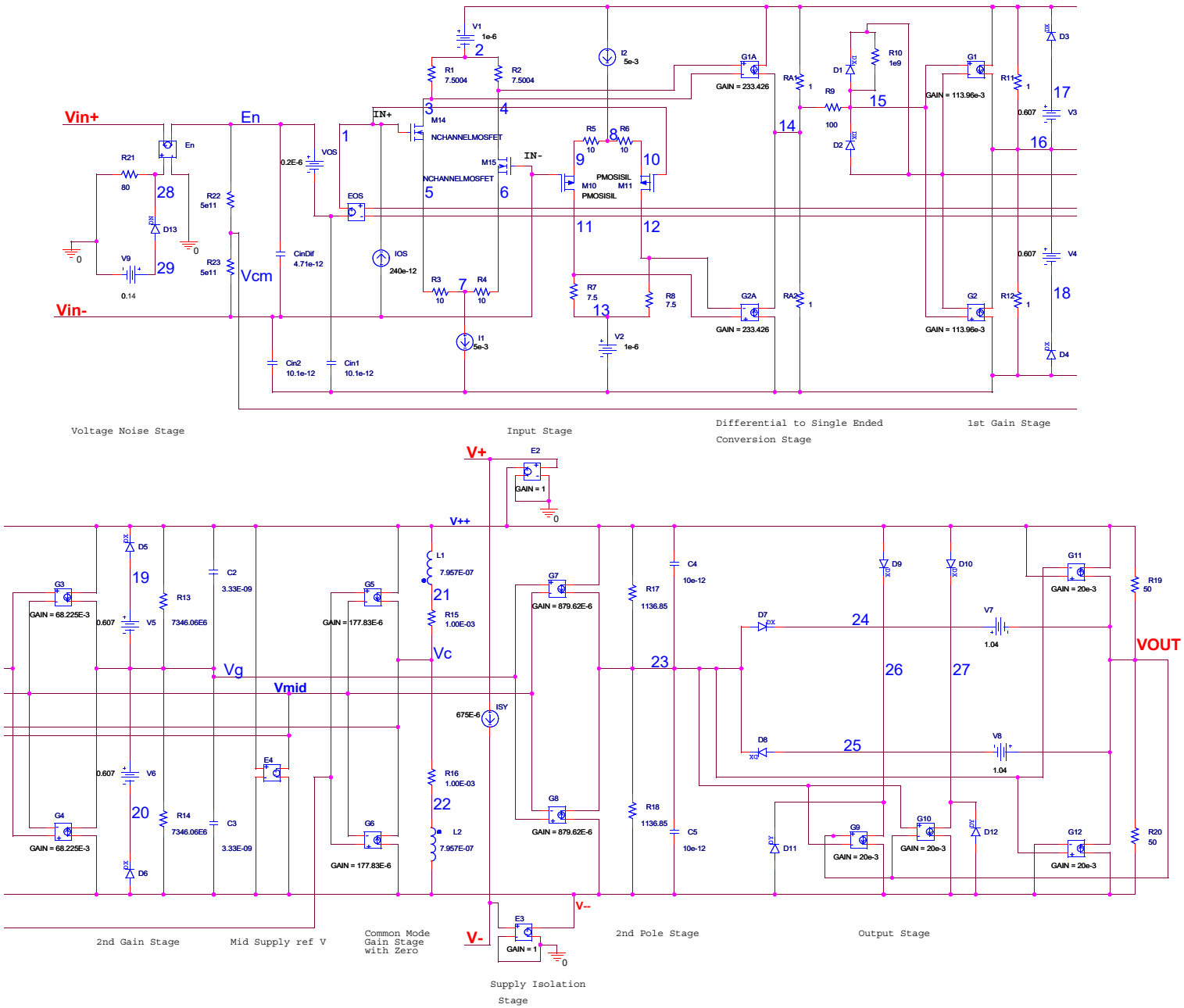


FIGURE 48. SPICE SCHEMATIC

```
*ISL28134 Macromodel
*
*Revision History:
* Revision A, LaFontaine June 17th 2011
* Model for Noise, quiescent supply currents,
*CMRR135dB f = 200Hz, AVOL 174dB f =
*6.5mHz, SR = 1.5V/us, GBWP 3.5MHz.
*Copyright 2011 by Intersil Corporation
*Refer to data sheet “LICENSE STATEMENT”
*Use of this model indicates your acceptance
*with the terms and provisions in the License
*Statement.
*
*Intended use:
*This Pspice Macromodel is intended to give
*typical DC and AC performance
*characteristics under a wide range of
*external circuit configurations using
*compatible simulation platforms – such as
*iSim PE.
*
*Device performance features supported by
*this model:
*Typical, room temp., nominal power supply
*voltages used to produce the following
*characteristics:
*Open and closed loop I/O impedances,
*Open loop gain and phase,
*Closed loop bandwidth and frequency
*response,
*Loading effects on closed loop frequency
*response,
*Input noise terms including 1/f effects,
*Slew rate, Input and Output Headroom limits
*to I/O voltage swing, Supply current at
*nominal specified supply voltages,
*Output current limiting (65mA)
*
*Device performance features NOT
*supported by this model:
*Harmonic distortion effects,
*Disable operation (if any),
*Thermal effects and/or over temperature
*parameter variation,
*Performance variation vs. supply voltage,
*Part to part performance variation due to
*normal process parameter spread,
*Any performance difference arising from
*different packaging,
*Load current reflected into the power supply
*current.
* source ISL28134
*
* Connections:     +input
*                        |    -input
*                        |    | +Vsupply
*                        |    |     | -Vsupply
*                        |    |     |   |  output
*                        |    |     |   |     |
.subckt ISL28134 Vin+ Vin- V+ V- VOUT
*
*Voltage Noise
E_En        VIN+ EN 28 0 1
D_D13       29 28 DN
V_V9        29 0 0.14
R_R21       28 0 80
*
*Input Stage
M_M10       11 VIN- 9 9 PMOSISIL
M_M11       12 1 10 10 PMOSISIL
M_M14       3 1 5 5 NCHANNELMOSFET
M_M15       4 VIN- 6 6 NCHANNELMOSFET
I_I1        7 V-- DC 5e-3
I_I2        V++ 8 DC 5e-3
I_IOS       VIN- 1 DC 240e-12
G_G1A       V++ 14 4 3 233.4267
G_G2A       V-- 14 11 12 233.4267
V_V1        V++ 2 1e-6
V_V2        13 V-- 1e-6
V_VOS       EN 30 0.2E-6
R_R1        3 2  7.5004
R_R2        4 2  7.5004
R_R3        5 7  10
R_R4        7 6  10
R_R5        9 8  10
R_R6        8 10  10
R_R7        13 11  7.5
R_R8        13 12  7.5
R_RA1       14 V++  1
R_RA2       V-- 14  1
C_CinDif    VIN- EN  4.71e-12
C_Cin1      V-- 30  10.1e-12
C_Cin2      V-- VIN-  10.1e-12
*
*1st Gain Stage
G_G1        V++ 16 15 VMID 113.96e-3
G_G2        V-- 16 15 VMID 113.96e-3
V_V3        17 16 0.607
V_V4        16 18 0.607
D_D1        15 VMID DX
D_D2        VMID 15 DX
D_D3        17 V++ DX
D_D4        V-- 18 DX
R_R9        15 14  100
R_R10       15 VMID  1e9
R_R11       16 V++  1
R_R12       V-- 16  1
*
*2nd Gain Stage
G_G3        V++ VG 16 VMID 68.225E-3
G_G4        V-- VG 16 VMID 68.225E-3
V_V5        19  VG 0.607
V_V6        VG 20 0.607
D_D5        19 V++ DX
D_D6        V-- 20 DX
R_R13       VG V++  7346.06E6
R_R14       V-- VG 7346.06E6
C_C2        VG V++  3.33E-09
C_C3        V-- VG 3.33E-09
*
*Mid supply Ref
E_E4        VMID V-- V++ V-- 0.5
*
*Supply Isolation Stage
E_E2        V++ 0 V+ 0 1
E_E3        V-- 0 V- 0 1
I_ISY       V+ V- DC 675E-6
*
*Common Mode Gain Stage
G_G5        V++ VC VCM VMID 177.83E-6
G_G6        V-- VC VCM VMID 177.83E-6
E_EOS       1 30 VC VMID 1
R_R15       VC 21  1.00E-03
R_R16       22 VC  1.00E-03
R_R22       EN VCM  5e11
R_R23       VCM VIN-  5e11
L_L1        21 V++  7.957E-07
L_L2        22 V--  7.957E-07
*
*2nd Pole Stage
G_G7        V++ 23 VG VMID 879.62E-6
G_G8        V-- 23 VG VMID 879.62E-6
R_R17       23 V++  1136.85
R_R18       V-- 23  1136.85
C_C4        23 V++  10e-12
C_C5        V-- 23  10e-12
*
*Output Stage
G_G9        26 V-- VOUT 23 20e-3
G_G10       27 V-- 23 VOUT 20e-3
G_G11       VOUT V++ V++ 23 20e-3
G_G12       V-- VOUT 23 V-- 20e-3
V_V7        24 VOUT 1.04
V_V8        VOUT 25 1.04
D_D7        23 24 DX
D_D8        25 23 DX
D_D9        V++ 26 DX
D_D10       V++ 27 DX
D_D11       V-- 26 DY
D_D12       V-- 27 DY
R_R19       VOUT V++  50
R_R20       V-- VOUT  50
*
.model pmosisil pmos (kp=16e-3 vto=-0.6
+kf=0 af=1)
.model NCHANNELMOSFET nmos (kp=3e-3
+vto=0.6 kf=0 af=1)
.model DN D(KF=6.69e-9 af=1)
.MODEL DX D(IS=1E-12 Rs=0.1 kf=0 af=1)
.MODEL DY D(IS=1E-15 BV=50 Rs=1 kf=0
+af=1)
.ends ISL28134
```

FIGURE 49. SPICE NET LIST

Characterization vs Simulation Results

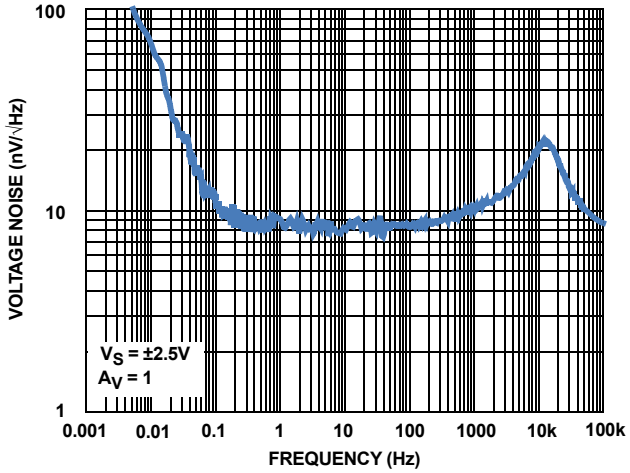


FIGURE 50. CHARACTERIZED INPUT NOISE VOLTAGE

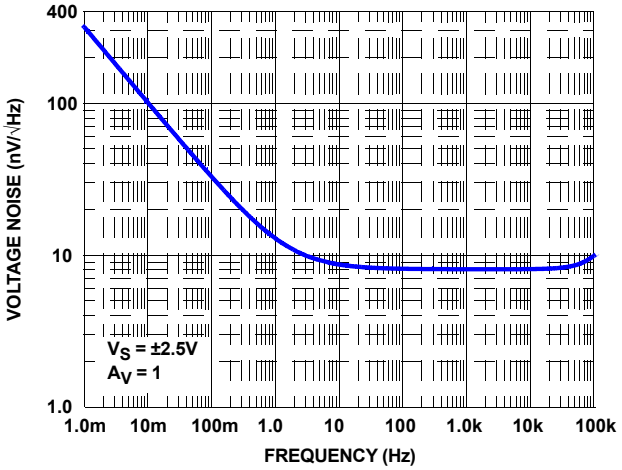


FIGURE 51. SIMULATED INPUT NOISE VOLTAGE

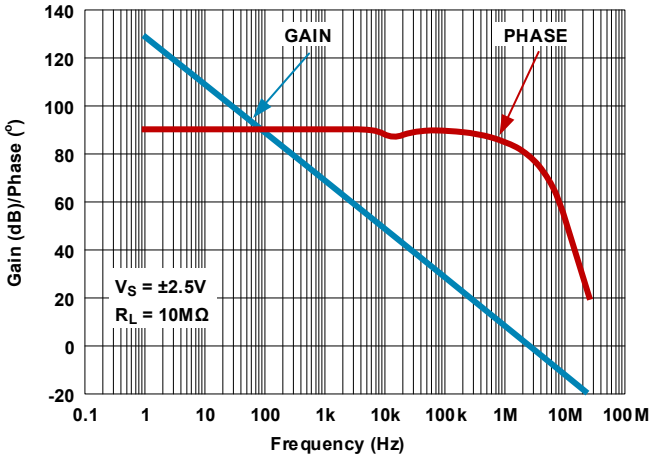


FIGURE 52. CHARACTERIZED OPEN-LOOP GAIN, PHASE vs FREQUENCY

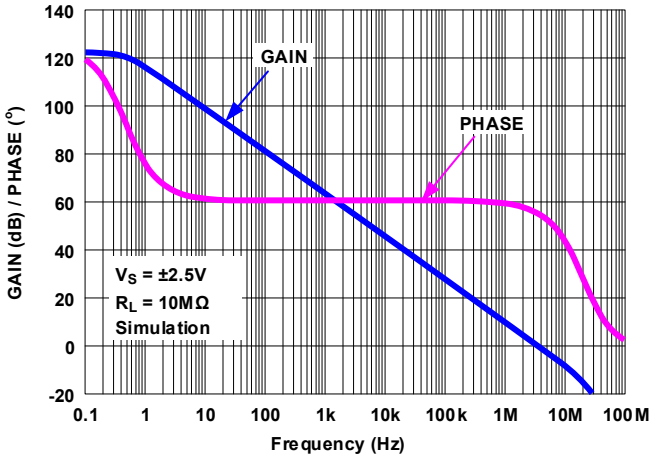


FIGURE 53. SIMULATED OPEN-LOOP GAIN, PHASE vs FREQUENCY

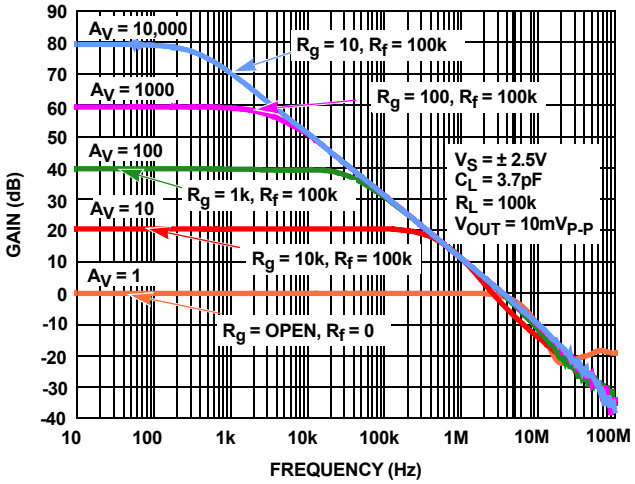


FIGURE 54. CHARACTERIZED CLOSED-LOOP GAIN vs FREQUENCY

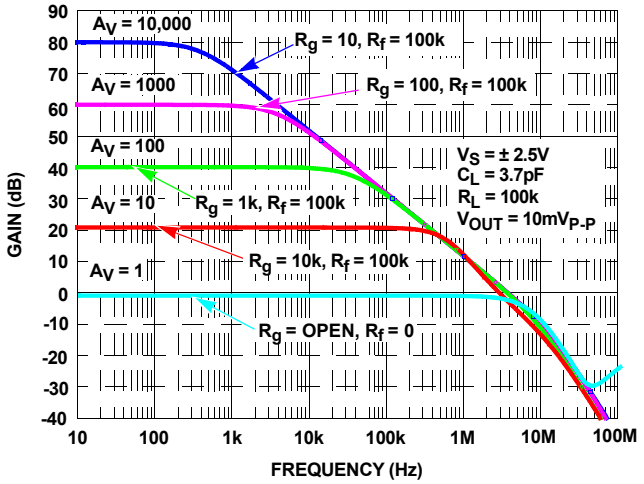


FIGURE 55. SIMULATED CLOSED-LOOP GAIN vs FREQUENCY

Characterization vs Simulation Results (Continued)

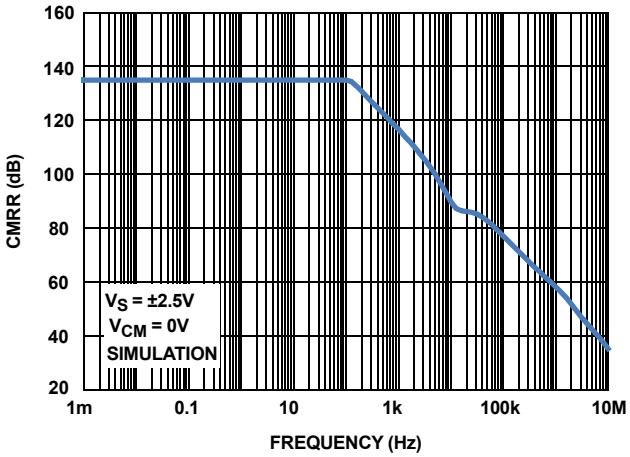


FIGURE 56. CHARACTERIZED CMRR vs FREQUENCY

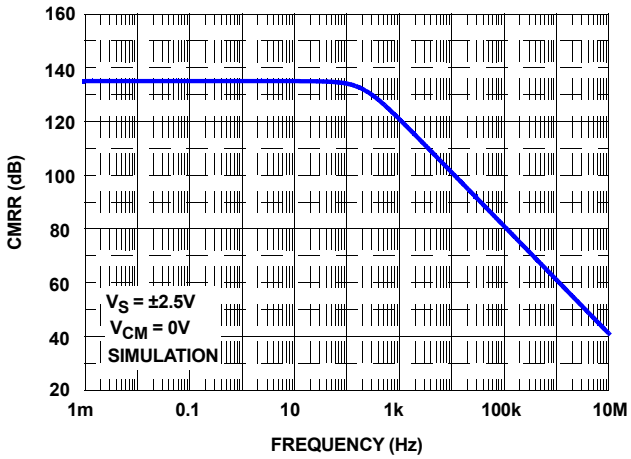


FIGURE 57. SIMULATED CMRR vs FREQUENCY

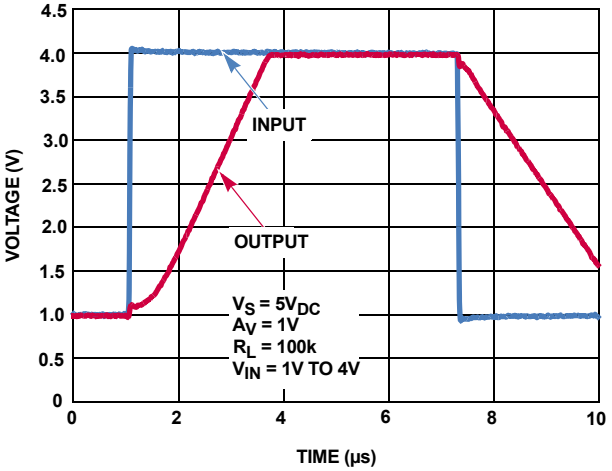


FIGURE 58. CHARACTERIZED LARGE SIGNAL STEP RESPONSE (3V)

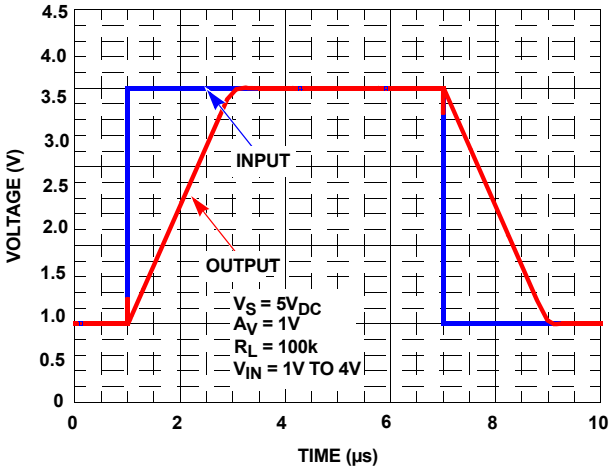


FIGURE 59. SIMULATED LARGE SIGNAL STEP RESPONSE (3V)

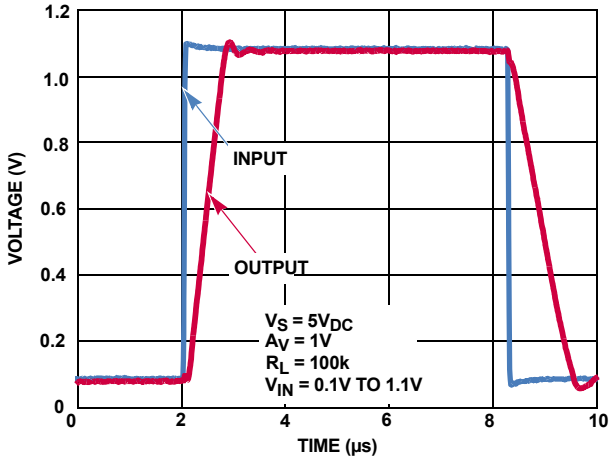


FIGURE 60. CHARACTERIZED SMALL-SIGNAL TRANSIENT RESPONSE

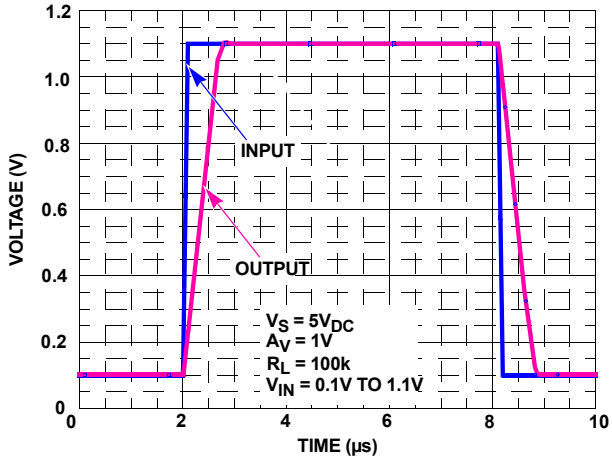


FIGURE 61. SIMULATED SMALL-SIGNAL TRANSIENT RESPONSE

Characterization vs Simulation Results (Continued)

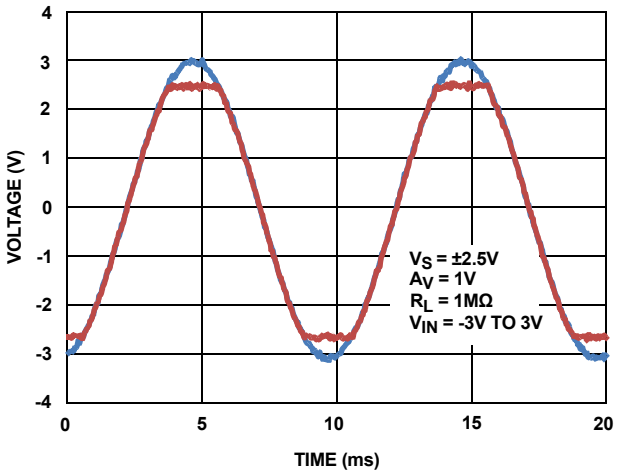


FIGURE 62. CHARACTERIZED NO PHASE INVERSION

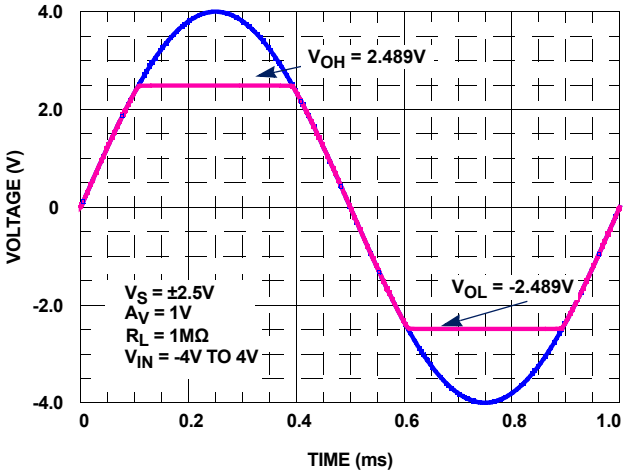


FIGURE 63. SIMULATED NO PHASE INVERSION, V_{OH} AND V_{OL}

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
Oct 27, 2022	6.03	Updated Figures 52 and 53.
Feb 22, 2022	6.02	Removed Related Literature section. Updated the Ordering Information table formatting. Corrected error in EC tables for V_{OS} (-40C to 125C) in the MAX column changed from -4uV to +4uV and moved V_{OS} and TCV_{OS} specs from the bottom of the first EC table (V_S = 5V) to the top of the 2nd EC table (V_S = 2.5V).
Mar 12, 2020	6.01	Updated Title Updated links throughout. Updated Related Literature. Updated Figures 1, 44, 45, 46, and 47. Updated Pin Configuration diagrams and circuits in Pin Description table. Updated Functional Description and High Source Impedance Applications sections. Removed About Intersil section. Updated disclaimer.
Oct 14, 2014	6.00	Figure 44 updated from: $R_s//R_g = R_S//R_g$ to: $R_F//R_I = R_S//R_g$. Removed part numbers ISL28134FRUZ-T7 and ISL28134FBZ from ordering information table. Removed 6 LD UTDFN throughout the document. Removed pod L6.1.6x1.6.
Jul 3, 2013	5.00	Updated the figure 1 on page 1, and changed title from “PRECISION 10-BIT WEIGH SCALE/STRAIN GAUGE” to “PRECISION WEIGH SCALE / STRAIN GAUGE”. Updated Figure 21: “Input noise voltage density vs frequency” on page 10. Added typical EMIRR spec to Electrical Spec table under section “AC SPECIFICATIONS” on page 5. Added applications paragraph to “EMI Rejection” on page 15. Added 2 Figures, 33 and 46, describing the test circuit and typical performance graph for “EMI Rejection” on page 15.
Aug 3, 2012	4.00	Made correction to Figure 1 on page 1 by changing resistor label from “1MΩ” to “20kΩ”.

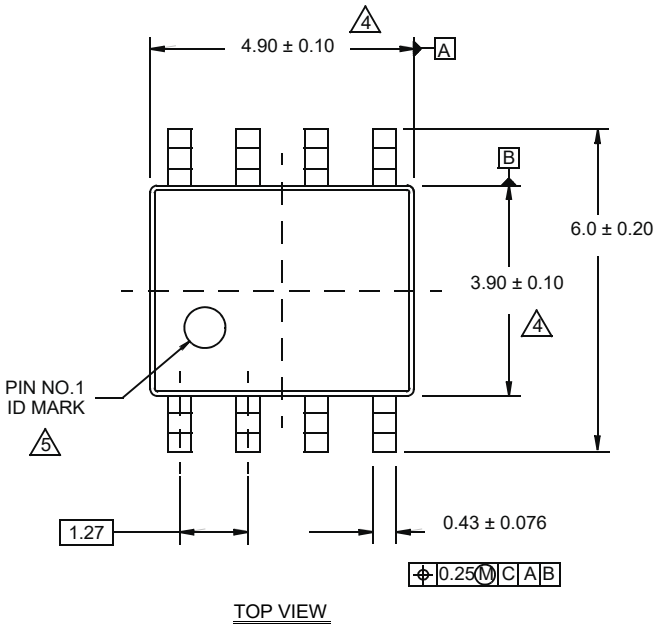
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision. **(Continued)**

DATE	REVISION	CHANGE
Dec 12, 2011	3.00	Updated front page introduction to reflect +125°C grade and SOT-23 package release. Updated Figure 1 with newer relevant Apps Circuit Updated Figure 2 with extended temp range -40°C to 125°C Updated "Ordering Information" on page 3 by removing "Coming Soon" from ISL28134FHZ SOT-23 packages. Updated "Operating Conditions" on page 4 to include Full Industrial Grade Package. Updated "Electrical Specifications" Tables for both Vs = 5V and Vs = 2.5V (page 4 to page 7) as follows: Modified common conditions at top of tables from "Boldface limits apply over the operating temperature range, -40°C to +85°C." to "Boldface limits apply over the specified operating temperature range." Added MIN/MAX Vos spec from -40°C to 125°C: ±4µV Updated Conditions cell for TCVos from +85°C to +125°C. No limit change. Added MIN/MAX Ibias spec from -40°C to 125°C: ±550pA Added Typ TCIbias spec from -40°C to 125°C: ±2pA/C Added MIN/MAX Ios spec from -40°C to 125°C: ±750pA Added Typ TCIos spec from TA = -40°C to +125°C: ±4pA/C Updated Conditions cell for Common Mode Input Voltage Range Spec (removed T_A = -40°C to +85°C). No limit change. Updated Conditions cell for CMRR for over temp (bolded) specs (removed T_A = -40°C to +85°C). No limit change. Updated Conditions cell for PSRR for over temp (bolded) specs (removed T_A = -40°C to +85°C). No limit change. Updated Conditions cell for Vs (removed T_A = -40°C to +85°C). No limit change. Added MAX Is spec from -40°C to 125°C: 1150µA Updated Conditions cell for VOH for over temp (bolded) specs (removed T_A = -40°C to +85°C). No limit change. Updated Conditions cell for VOL for over temp (bolded) specs (removed T_A = -40°C to +85°C). No limit change. Updated the following Figures to reflect the temp range from the range of (-40°C to 85°C) to (-40°C to 125°C) Figures 3-8, page 7 to page 8 Figures 11-20, page 8 to page 10 Minor edit to SPICE netlist Figure 49, page 18. Added "+" signs on 3 rows as follows: "model pmosisil pmos (kp=16e-3 vto=-0.6 +kf=0 af=1) .model NCHANNELMOSFET nmos (kp=3e-3 +vto=0.6 kf=0 af=1) .model DN D(KF=6.69e-9 af=1) .MODEL DX D(IS=1E-12 Rs=0.1 kf=0 af=1) .MODEL DY D(IS=1E-15 BV=50 Rs=1 kf=0 +af=1) .ends ISL28134"
Jul 6, 2011	2.00	Added Evaluation board to "Ordering Information" on page 3. Updated "INPUT NOISE VOLTAGE DENSITY vs FREQUENCY" on page 10 (Changed MIN frequency from 100mHz to 1mHz) Updated "LARGE SIGNAL STEP RESPONSE (3V)" on page 13 by changing the Time from 0 to 10 to 0 to 20 Added "ISL28134 SPICE Model" section, which includes Schematic, Macromodel and Characterization vs Simulation Results.
Jun 8, 2011	1.00	Initial release to web.

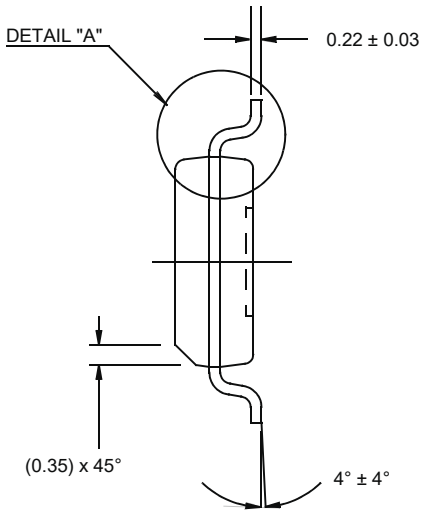
Package Outline Drawings

For the most recent package outline drawing, see M8.15E.

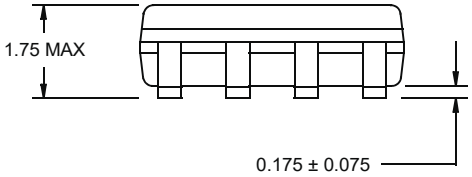
M8.15E
8 Lead Narrow Body Small Outline Plastic Package
Rev 0, 08/09



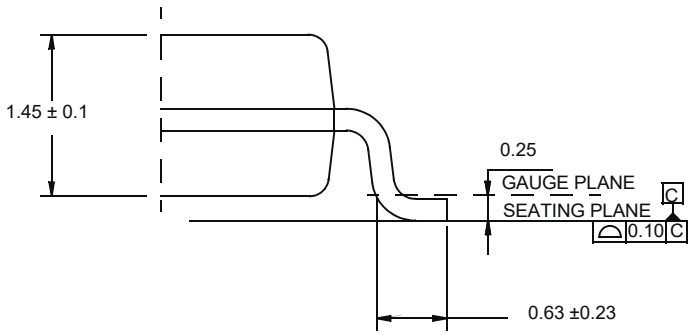
TOP VIEW



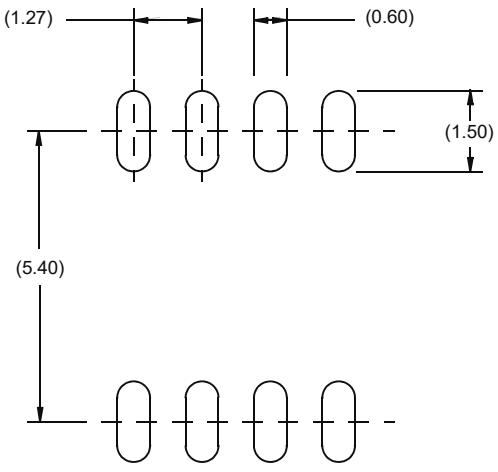
SIDE VIEW "B"



SIDE VIEW "A"



DETAIL "A"



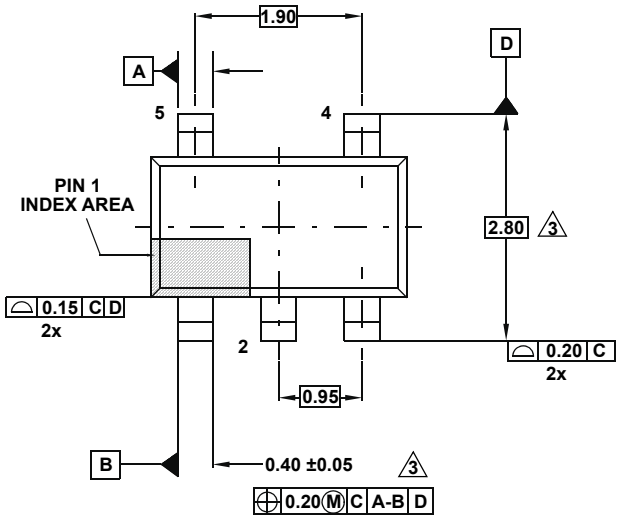
TYPICAL RECOMMENDED LAND PATTERN

NOTES:

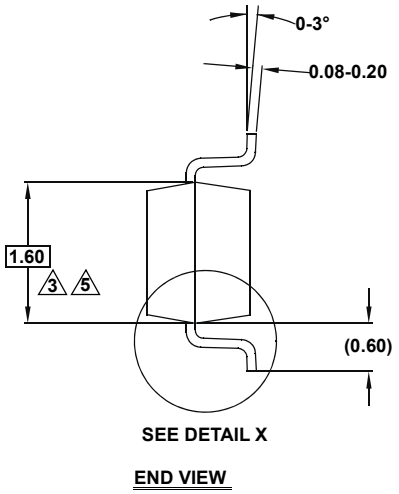
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

For the most recent package outline drawing, see P5.064A.

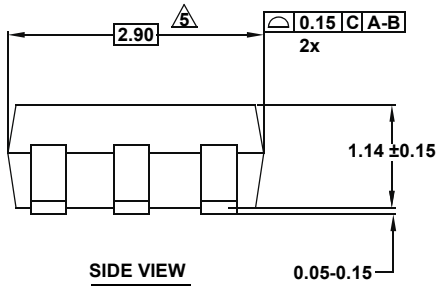
P5.064A
5 Lead Small Outline Transistor Plastic Package
Rev 0, 2/10



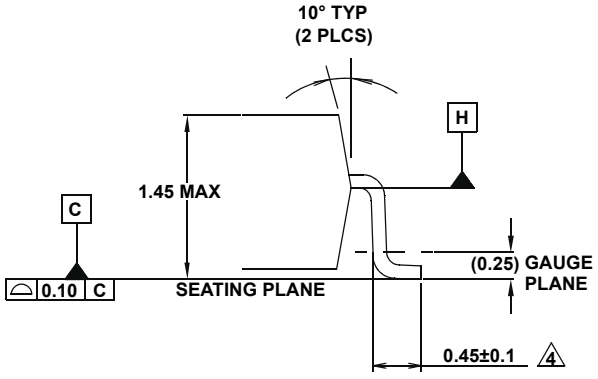
TOP VIEW



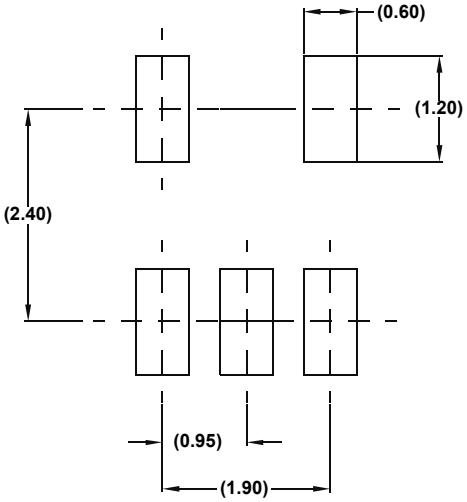
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to guage plane.
5. This dimension is measured at Datum “H”.
6. Package conforms to JEDEC MO-178AA.

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