

# AR0238: 1/2.7-Inch 2.1 Mp/Full HD Digital Image Sensor

## AR0238

### General Description

onsemi's AR0238 is a 1/2.7-inch CMOS digital image sensor with an active-pixel array of 1928Hx1088V. It captures images in either linear or high dynamic range modes, with a rolling-shutter readout. It includes sophisticated camera functions such as in-pixel binning, windowing and both video and single frame modes. It is designed for both low light and high dynamic range scene performance. It is programmable through a simple two-wire serial interface. The AR0238 produces extraordinarily clear, sharp digital pictures, and its ability to capture both continuous video and single frames makes it the perfect choice for a wide range of applications, including surveillance and HD video.

**Table 1. KEY PARAMETERS**

| Parameter                   |          | Typical Value                                                                                                      |
|-----------------------------|----------|--------------------------------------------------------------------------------------------------------------------|
| Optical format              |          | 1/2.7–inch (6.6 mm)                                                                                                |
| Active pixels               |          | 1928(H) x 1088(V) (16:9 mode)                                                                                      |
| Pixel size                  |          | 3.0 μm x 3.0 μm                                                                                                    |
| Color filter array          |          | RGB Bayer, RGB–IR                                                                                                  |
| Shutter type                |          | Electronic rolling shutter and GRR                                                                                 |
| Input clock range           |          | 6 – 48 MHz                                                                                                         |
| Output clock maximum        |          | 148.5 Mp/s (4–lane HiSPi)<br>74.25 Mp/s (Parallel)                                                                 |
| Output                      | Serial   | HiSPi 10–, or 12–bit                                                                                               |
|                             | Parallel | 10–, or 12–bit                                                                                                     |
| Frame rate                  | 1080p    | 60 fps Linear HiSPi<br>30 fps Linear Parallel<br>30 fps Line Interleaved HiSPi<br>15 fps Line Interleaved Parallel |
| Responsivity                |          | 4.0 V/lux–sec                                                                                                      |
| SNR <sub>MAX</sub>          |          | 41 dB                                                                                                              |
| Max Dynamic range           |          | Up to 96 dB                                                                                                        |
| Supply voltage              | I/O      | 1.8 or 2.8 V                                                                                                       |
|                             | Digital  | 1.8 V                                                                                                              |
|                             | Analog   | 2.8 V                                                                                                              |
|                             | HiSPi    | 0.3 V – 0.6 V (SLVS), 1.7 V – 1.9 V (HiVcm)                                                                        |
| Power consumption (typical) |          | < 300 mW Line interleaved 1080p30<br><190 mW 1080p30 Linear Mode                                                   |
| Operating temperature       |          | –30°C to + 85°C Ambient                                                                                            |
| Package options             |          | 11.43x11.43 mm 48–pin mPLCC<br>Recon Die                                                                           |

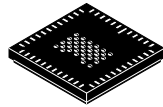
### Features

- Superior Low-light Performance
- Latest 3.0  $\mu\text{m}$  Pixel with onsemi DR-Pix™ Technology with Dual Conversion Gain
- Full HD Support at up to 1080P 60 fps for Superior Video Performance
- Linear or High Dynamic Range Capture
- Supports Line Interleaved T1/T2 readout to Enable HDR Processing in ISP Chip
- Support for External Mechanical Shutter
- On-chip Phase-locked Loop (PLL) Oscillator
- Integrated Position-based Color and Lens Shading Correction
- Slave Mode for Precise Frame-rate Control
- Stereo/3D Camera Support
- Statistics Engine
- Data Interfaces: Four-lane Serial High-speed Pixel Interface (HiSPi) Differential Signaling (SLVS and HiVCM), or Parallel
- Auto Black Level Calibration
- High-speed Configurable Context Switching
- Temperature Sensor

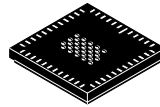
### Applications

- Video Recording and Streaming
- 1080p60 (monitoring) Video Applications
- High Dynamic Range Imaging

# AR0238



PLCC48 11.43x11.43 (HiSPi)  
CASE 776AQ



PLCC48 11.43x11.43 (Parallel)  
CASE 776AS

**Table 2. ORDERING INFORMATION**

| Part Number             | Product Description                       | Orderable Product Attribute Description |
|-------------------------|-------------------------------------------|-----------------------------------------|
| AR0238CSSC12SHRA0-DR1   | RGB Color, 12 Degree CRA, mPLCC, HiSPi    | Dry Pack, No Protective film, Low MOQ   |
| AR0238CSSC12SHRA0-DP1   | RGB Color, 12 Degree CRA, mPLCC, HiSPi    | Dry Pack, with Protective film, Low MOQ |
| AR0238CSSC12SHRA0-DR    | RGB Color, 12 Degree CRA, mPLCC, HiSPi    | Without protective film                 |
| AR0238CSSC12SHRA0-DP    | RGB Color, 12 Degree CRA, mPLCC, HiSPi    | With protective film                    |
| AR0238CSSC12SPRA0-DR    | RGB Color, 12 Degree CRA, mPLCC, Parallel | Without Protective Film                 |
| AR0238CSSC12SPRA0-DR1   | RGB Color, 12 Degree CRA, mPLCC, Parallel | Dry Pack, No Protective film, Low MOQ   |
| AR0238CSSC12SUD20       | RGB Color, 12 Degree CRA, Recon die       | RGB Recon die                           |
| AR0238IRSH12SUD20       | RGB-IR, 12 Degree CRA, Recon die          | RGB-IR Recon die                        |
| AR0238CSSC12SHRAH3-GEVB | RGB Color, 12 Degree CRA, HiSPi           | Evaluation Board                        |

NOTE: See the **onsemi** Device Nomenclature document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at [www.onsemi.com](http://www.onsemi.com).

## GENERAL DESCRIPTION

The **onsemi** AR0238 can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode output is a 1080p- resolution image at 60 frames per second (fps) through the HiSPi port. In linear mode, it outputs 12-bit or 10-bit A-Law compressed raw data, using the parallel or serial (HiSPi) output port. In high dynamic range mode, it outputs two exposure values that the ISP will combine into an HDR image. The device may be operated in video (master) mode or in single frame trigger mode.

FRAME\_VALID and LINE\_VALID signals are output on dedicated pins, along with a synchronized pixel clock in parallel mode.

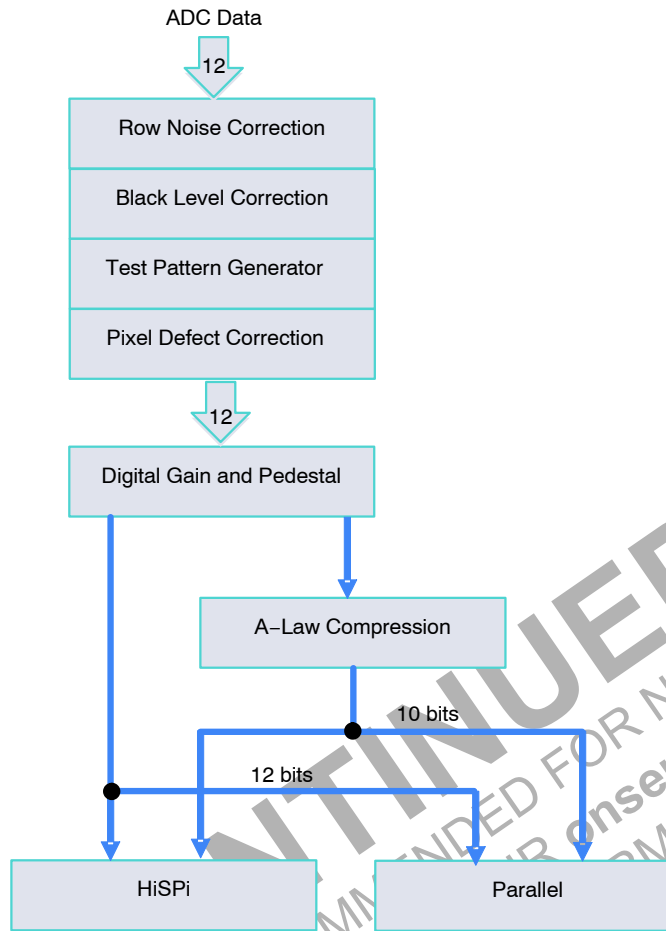
The AR0238 includes additional features to allow application-specific tuning: windowing and offset, auto

black level correction, and on-board temperature sensor. Optional register information and histogram statistic information can be embedded in the first and last 2 lines of the image frame.

The AR0238 is designed to operate over a wide temperature range of -30°C to +85°C ambient.

## FUNCTIONAL OVERVIEW

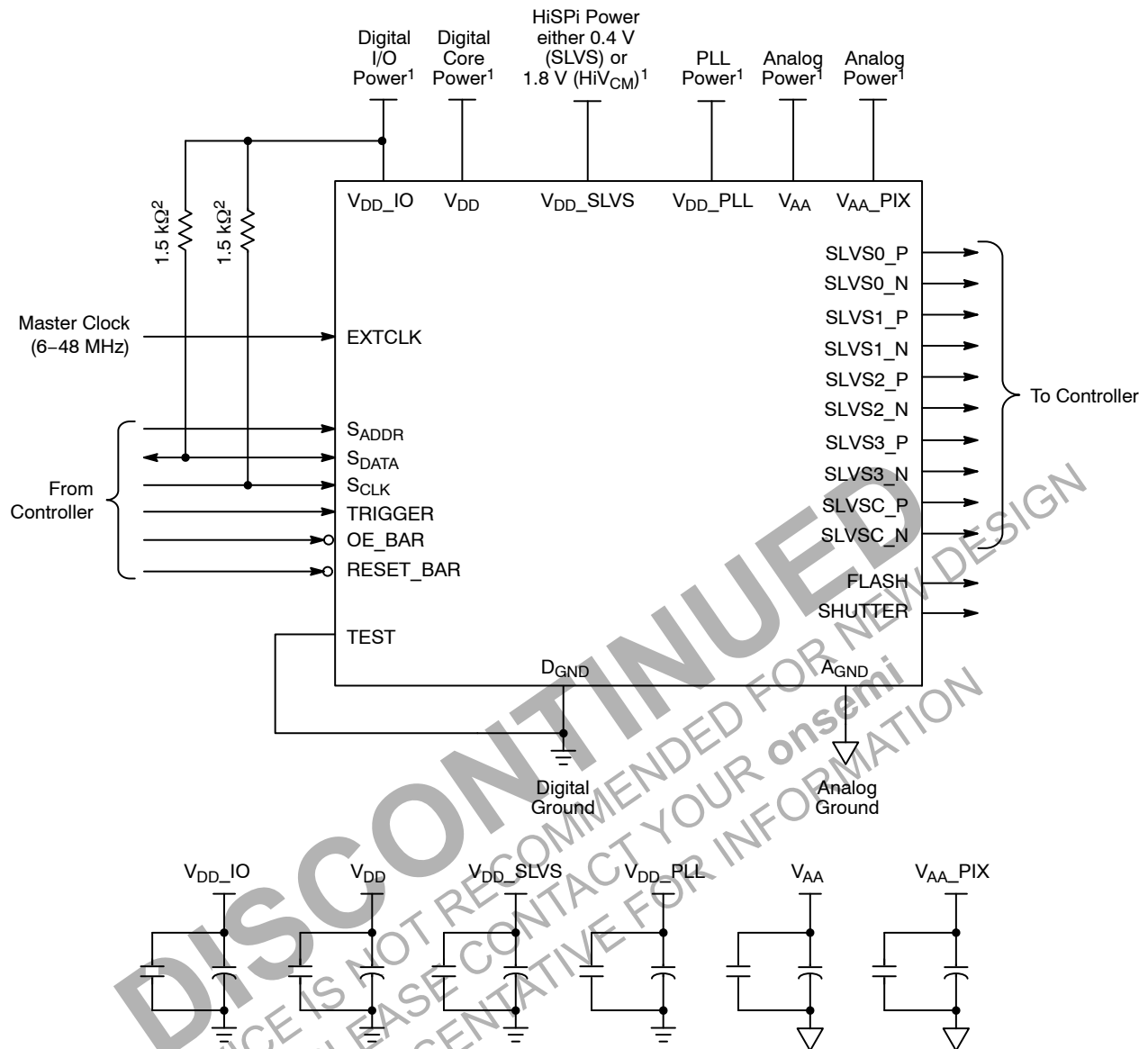
The AR0238 is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip, phase-locked loop (PLL) that can be optionally enabled to generate all internal clocks from a single master input clock running between 6 and 48 MHz. The maximum output pixel rate is 148.5 Mp/s, corresponding to a clock rate of 74.25 MHz. Figure 1 shows a block diagram of the sensor configured in linear mode, and in HDR mode.



**Figure 1. Block Diagram of AR0238**

User interaction with the sensor is through the two-wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 2.1 Mp Active-Pixel Sensor array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain

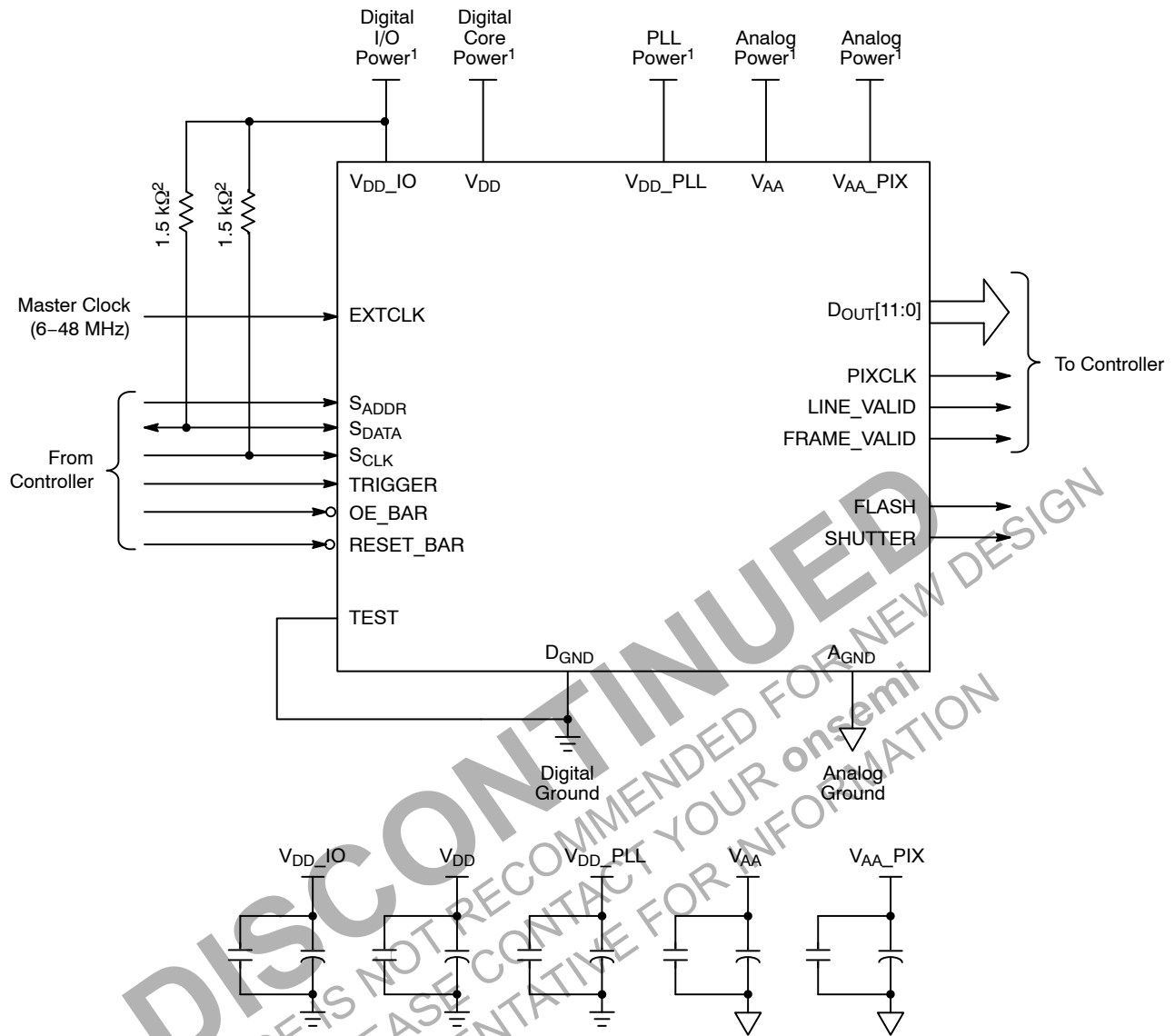
(providing offset correction and gain), and then through an analog-to-digital converter (ADC). The output from the ADC is a 12-bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain). The sensor also offers a high dynamic range mode of operation where two images are taken using different exposures. These images are output from the sensor and the ISP must combine them into one high dynamic range image.



## Notes:

1. All power supplies must be adequately decoupled.
2. **onsemi** recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two-wire speed.
3. The parallel interface output pads can be left unconnected if the serial output interface is used.
4. **onsemi** recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on the layout and design considerations. Refer to the AR0237AT demo headboard schematics for circuit recommendations.
5. **onsemi** recommends that analog power planes be placed in a manner such that coupling with the digital power planes is minimized.
6. I/O signals voltage must be configured to match VDD\_IO voltage to minimize any leakage currents.

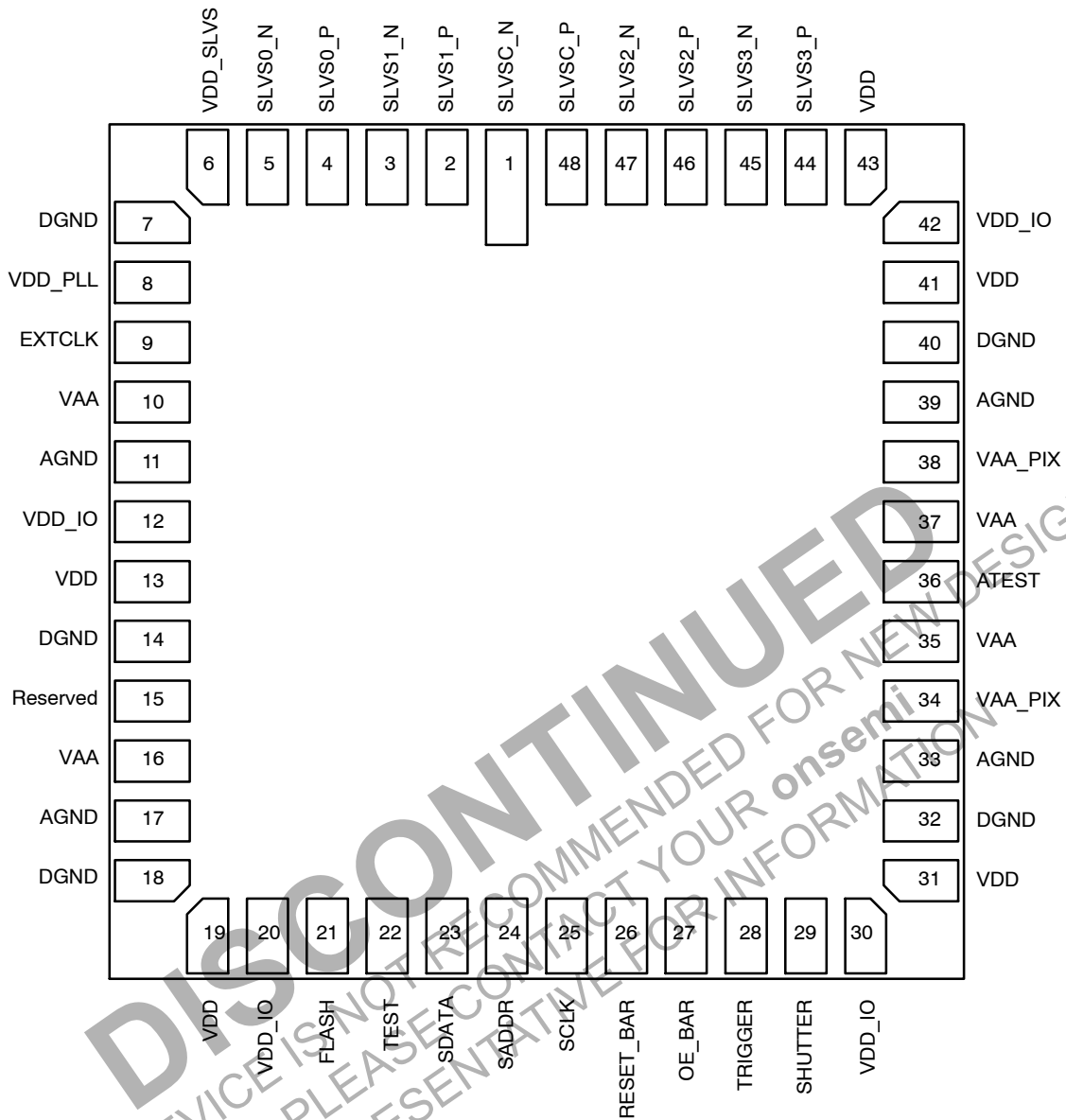
**Figure 2. Typical Configuration: Serial Four-Lane HiSPi Interface**



## Notes:

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5. **onsemi** recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
6. I/O signals voltage must be configured to match VDD\_IO voltage to minimize any leakage currents.
7. The EXTCLK input is limited to 6-48 MHz.

Figure 3. Typical Configuration: Parallel Pixel Data Interface



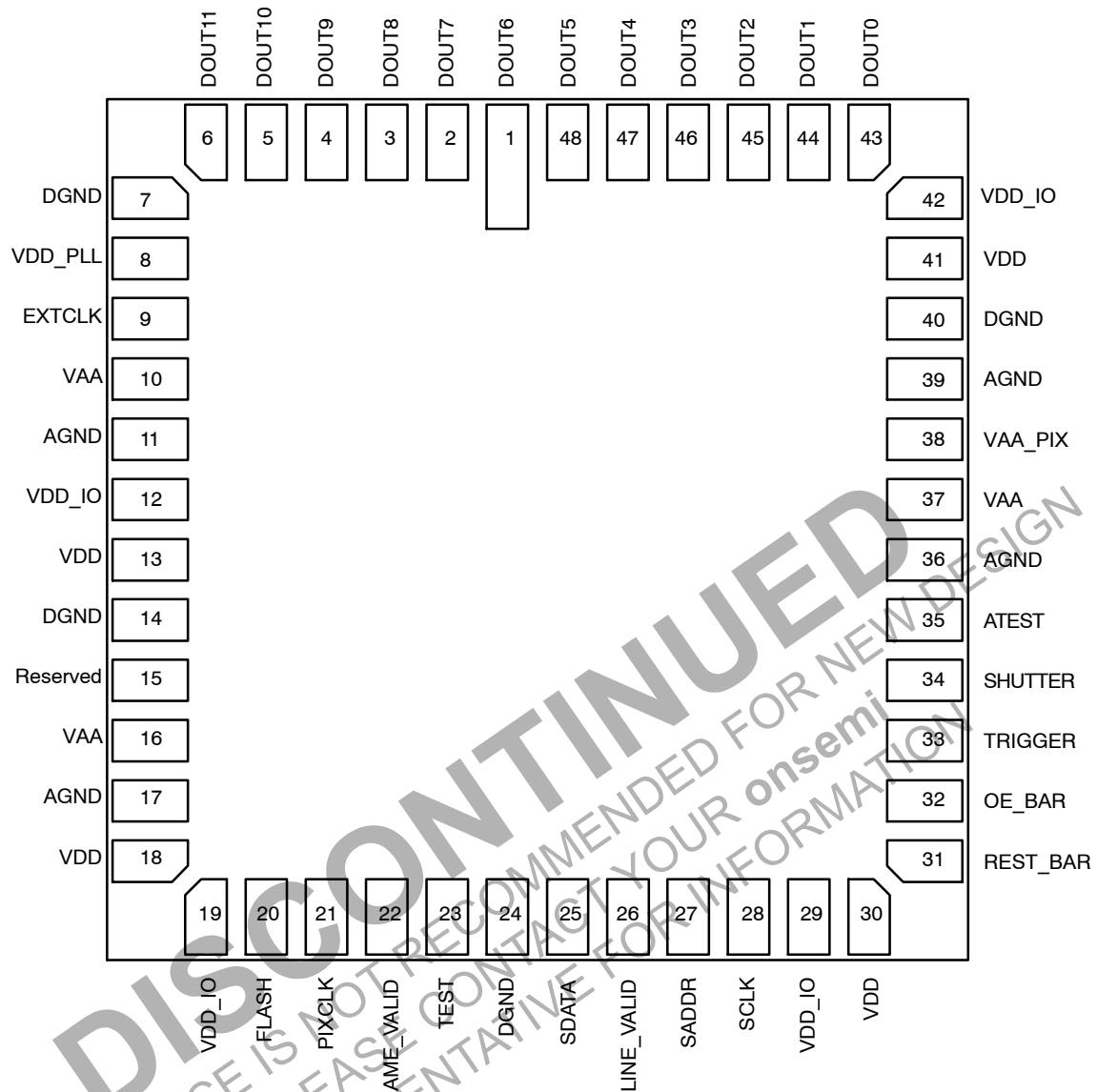
(Top View - Lead Down)

**Figure 4. HiSPi 48-Lead mPLCC Package**

Table 3. PIN DESCRIPTIONS, HiSPi 48-Lead mPLCC

| DS Name   | mPLCC Pin          | Type   | Description                                                                                                                                  |
|-----------|--------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------|
| SLVSC_N   | 1                  | Output | HiSPi serial DDR clock differential N                                                                                                        |
| SLVS1_P   | 2                  | Output | HiSPi serial data, lane 1, differential P                                                                                                    |
| SLVS1_N   | 3                  | Output | HiSPi serial data, lane 1, differential N                                                                                                    |
| SLVS0_P   | 4                  | Output | HiSPi serial data, lane 0, differential P                                                                                                    |
| SLVS0_N   | 5                  | Output | HiSPi serial data, lane 0, differential N                                                                                                    |
| VDD_SLVS  | 6                  | Power  | 0.3 V–0.6 V or 1.7 V – 1.9 V port to HiSPi Output Driver. Set the High_VCM (R0x306E[9]) bit to 1 when configuring VDD_SLVS to 1.7 V – 1.9 V. |
| DGND      | 7, 14, 18, 32, 40  | Power  | Digital ground                                                                                                                               |
| VDD_PLL   | 8                  | Power  | PLL power, 2.8 V nominal                                                                                                                     |
| EXTCLK    | 9                  | Input  | External input clock                                                                                                                         |
| VAA       | 10, 16, 35, 37     | Power  | Analog power, 2.8 V nominal                                                                                                                  |
| AGND      | 11, 17, 33, 39     | Power  | Analog ground.                                                                                                                               |
| VDD_IO    | 12, 20, 30, 42     | Power  | I/O supply power, 1.8/2.8 V nominal                                                                                                          |
| VDD       | 13, 19, 31, 41, 43 | Power  | Digital power, 1.8 V nominal                                                                                                                 |
| Reserved  | 15                 | –      | Reserved, NC                                                                                                                                 |
| FLASH     | 21                 | Output | Flash control output                                                                                                                         |
| TEST      | 22                 | Input  | Manufacturing test enable pin (connect to Dgnd)                                                                                              |
| SDATA     | 23                 | I/O    | Two-Wire Serial data I/O                                                                                                                     |
| SADDR     | 24                 | Input  | Two-Wire Serial address select. 0: 0x20. 1: 0x30                                                                                             |
| SCLK      | 25                 | Input  | Two-Wire Serial clock input                                                                                                                  |
| RESET_BAR | 26                 | Input  | Asynchronous reset (active LOW). All settings are restored to factory default.                                                               |
| OE_BAR    | 27                 | Input  | Output enable (active LOW)                                                                                                                   |
| TRIGGER   | 28                 | Input  | Exposure synchronization input                                                                                                               |
| SHUTTER   | 29                 | Output | Control for external mechanical shutter. Can be left floating if not used.                                                                   |
| VAA_PIX   | 34, 38             | Power  | Pixel power, 2.8 V nominal                                                                                                                   |
| ATEST     | 36                 | –      | Reserved, NC                                                                                                                                 |
| SLVS3_P   | 44                 | Output | HiSPi serial data, lane 3, differential P                                                                                                    |
| SLVS3_N   | 45                 | Output | HiSPi serial data, lane 3, differential N                                                                                                    |
| SLVS2_P   | 46                 | Output | HiSPi serial data, lane 2, differential P                                                                                                    |
| SLVS2_N   | 47                 | Output | HiSPi serial data, lane 2, differential N                                                                                                    |
| SLVSC_P   | 48                 | Output | HiSPi serial DDR clock differential P                                                                                                        |

NOTE: The 36 thermal connection pads should be all soldered to DGND plane for better thermal conductivity. Refer to PACKAGE DIMENSIONS for details..



(Top View – Lead Down)

**Figure 5. 48–Lead Parallel mPLCC**

Table 4. 48–Lead PARALLEL mPLCC

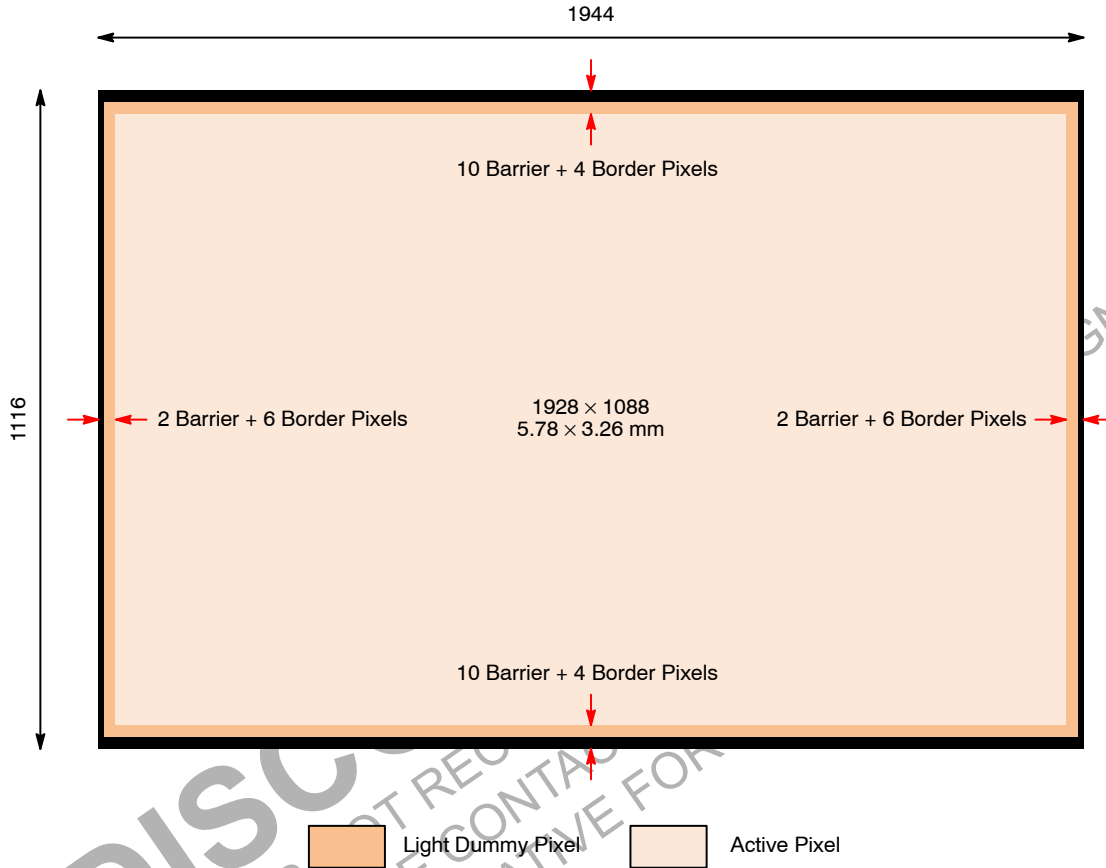
| Name        | mPLCC Pin      | Type   | Description                                                                   |
|-------------|----------------|--------|-------------------------------------------------------------------------------|
| DOUT6       | 1              | Output | Data output 6                                                                 |
| DOUT7       | 2              | Output | Data output 7                                                                 |
| DOUT8       | 3              | Output | Data output 8                                                                 |
| DOUT9       | 4              | Output | Data output 9                                                                 |
| DOUT10      | 5              | Output | Data output 10                                                                |
| DOUT11      | 6              | Power  | Data output 11                                                                |
| DGND        | 7, 14, 24, 40  | Power  | Digital ground                                                                |
| VDD_PLL     | 8              | Power  | PLL power, 2.8 V nominal                                                      |
| EXTCLK      | 9              | Input  | External input clock                                                          |
| VAA         | 10, 16, 37     | Power  | Analog power, 2.8 V nominal                                                   |
| AGND        | 11, 17, 36, 39 | Power  | Analog Ground                                                                 |
| VDD_IO      | 12, 19, 29, 42 | Power  | I/O supply power, 1.8/2.8 V nominal                                           |
| VDD         | 13, 18, 30, 41 | Power  | Digital power, 1.8 V nominal                                                  |
| Reserved    | 15             | –      | Reserved, NC                                                                  |
| FLASH       | 20             | Power  | Flash control output                                                          |
| PIXCLK      | 21             | Output | Pixel Clock                                                                   |
| FRAME_VALID | 22             | Output | Frame Valid                                                                   |
| TEST        | 23             | Input  | Manufacturing test enable pin (connect to DGND)                               |
| SDATA       | 25             | I/O    | Two-Wire Serial data I/O                                                      |
| LINE_VALID  | 26             | Output | Line Valid                                                                    |
| SADDR       | 27             | Input  | Two-Wire Serial address select. 0: 0x20, 1: 0x30                              |
| SCLK        | 28             | Input  | Two-Wire Serial clock input                                                   |
| RESET_BAR   | 31             | Input  | Asynchronous reset (active LOW). All settings are restored to factory default |
| OE_BAR      | 32             | Input  | Output enable (active LOW)                                                    |
| TRIGGER     | 33             | Input  | Exposure synchronization input                                                |
| SHUTTER     | 34             | Output | Control for external mechanical shutter. Can be left floating if not used.    |
| ATEST       | 35             | –      | Reserved, NC                                                                  |
| VAA_PIX     | 38             | Power  | Pixel power, 2.8 V nominal                                                    |
| DOUT0       | 43             | Output | Data Output 0                                                                 |
| DOUT1       | 44             | Output | Data Output 1                                                                 |
| DOUT2       | 45             | Output | Data Output 2                                                                 |
| DOUT3       | 46             | Output | Data Output 3                                                                 |
| DOUT4       | 47             | Output | Data Output 4                                                                 |
| DOUT5       | 48             | Output | Data Output 5                                                                 |

NOTE: The 29 thermal connection pads should be all soldered to DGND plane for better thermal conductivity. Refer to PACKAGE DIMENSIONS for details.

**PIXEL DATA FORMAT****PIXEL ARRAY STRUCTURE**

While the sensor's format is 1928 x 1088, additional active columns and active rows are included for use when horizontal or vertical mirrored readout is enabled, to allow

readout to start on the same pixel. The pixel adjustment is always performed for mono-chrome or color versions. The active area is surrounded with optically transparent dummy pixels to improve image uniformity within the active area. Not all dummy pixels or barrier pixels can be read out.



**Figure 6. Pixel Array Description**

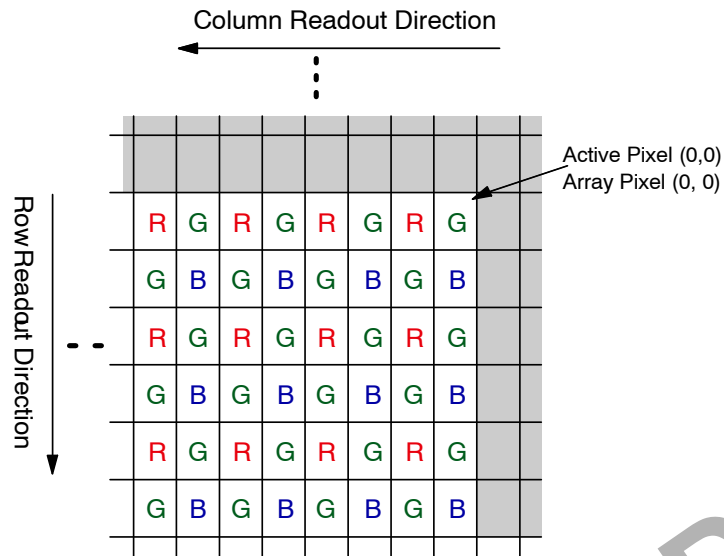


Figure 7. Pixel Color Pattern Detail (RGB) (Top Right Corner)

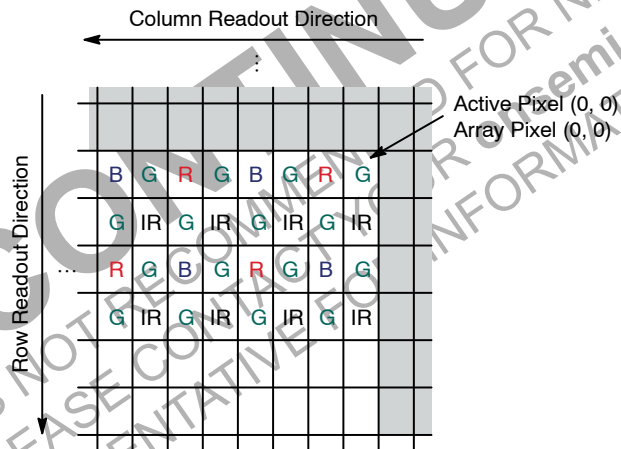


Figure 8. Pixel Color Pattern Detail (RGB-IR) (Top Right Corner)

**DEFAULT READOUT ORDER**

By convention, the sensor core pixel array is shown with pixel (0,0) in the top right corner (see Figure 7). This reflects the actual layout of the array on the die. Also, the first pixel data read out of the sensor in default condition is that of pixel (10, 14).

When the sensor is imaging, the active surface of the sensor faces the scene as shown in Figure 9. When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced as shown in Figure 9.

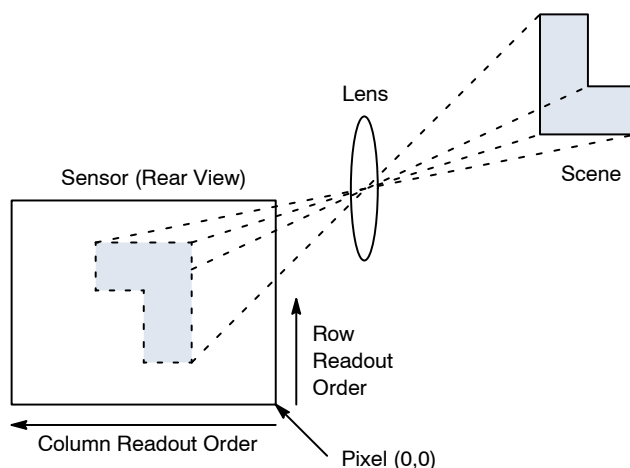


Figure 9. Imaging a Scene

## FEATURES OVERVIEW

For a complete description, recommendations, and usage guidelines for product features, refer to the AR0238 Developer Guide.

### 3.0 $\mu\text{m}$ Dual Conversion Gain Pixel

To improve the low light performance and keep the high dynamic range, a large (3.0  $\mu\text{m}$ ) dual conversion gain pixel is implemented for better image optimization. With a dual conversion gain pixel, the conversion gain of the pixel may be dynamically changed to better adapt the pixel response based on dynamic range of the scene. This gain can be switched manually or automatically by an auto exposure control module.

### HDR

By default, the sensor powers up in Linear Mode. One can change to HDR Mode. The HDR scheme used is multi-exposure HDR. This allows the sensor to handle up to 96 dB of dynamic range. In HDR mode, the sensor sequentially captures two exposures by maintaining two separate read and reset pointers that are interleaved within the rolling shutter readout. The exposure ratio may be set to 4x, 8x, 16x, or 32x. Sensor also provides flexibility to choose any exposure ratio by setting number of t2 exposure rows independent of the t1 exposure. The data will be output as line interleaved data as described in the T1/T2 Line Interleaved Mode section. There is also an option to output either T1 only or T2 only.

### RESOLUTION

The active array supports a maximum of 1928x1088 pixels to support 1080p resolution. Utilizing a 3.0  $\mu\text{m}$  pixel will result in an optical format of 1/2.7-inch (approximately 6.6 mm diagonal).

### FRAME RATE

At full (1080p) resolution, the AR0238 is capable of running up to 60 fps in linear mode and 30 fps in line interleaved mode.

## IMAGE ACQUISITION MODE

The AR0238 supports two image acquisition modes:

- Electronic rolling shutter (ERS) mode

This is the normal mode of operation. When the AR0238 is streaming, it generates frames at a fixed rate, and each frame is integrated (exposed) using the ERS. When ERS mode is in use, timing and control logic within the sensor sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and subsequently reading that row, the pixels in the row integrate incident light. The integration (exposure) time is controlled by varying the time between row reset and row readout. For each row in a frame, the time between row reset and row readout is the same, leading to a uniform integration time across the frame. When the integration time is changed (by using the two-wire serial interface to change register settings), the timing and control logic controls the transition from old to new integration time in such a way that the stream of output frames from the AR0238 switches cleanly from the old integration time to the new while only generating frames with uniform integration. See “Changes to Integration Time” in the AR0238 Register Reference.

- Global reset mode.

This mode can be used to acquire a single image at the current resolution. In this mode, the end point of the pixel integration time is controlled by an external electromechanical shutter, and the AR0238 provides control signals to interface to that shutter. The benefit of using an external electromechanical shutter is that it eliminates the visual artifacts associated with ERS operation. Visual artifacts arise in ERS operation, particularly at low frame rates, because an ERS image effectively integrates each row of the pixel array at a different point in time.

## EMBEDDED DATA AND STATISTICS

The AR0238 has the capability to output image data and statistics embedded within the frame timing. There are two types of information embedded within the frame readout.

- **Embedded Data:**  
If enabled, these are displayed on the two rows immediately before the first active pixel row is displayed.
- **Embedded Statistics:**  
If enabled, these are displayed on the two rows immediately after the last active pixel row is displayed.

## MULTI-CAMERA SYNCHRONIZATION

### SLAVE MODE

The slave mode feature of the AR0238 supports triggering the start of a frame readout from an input signal that is supplied from an external ASIC. The slave mode signal allows for precise control of frame rate and register change updates.

### Context Switching and Register Updates

The user has the option of using the highly configurable context memory, or a simplified implementation in which

only a subset of registers is available for switching. The AR0238 supports a highly configurable context switching RAM of size 256 x 16. Within this Context Memory, changes to any register may be stored. The register set for each context must be the same, but the number of contexts and registers per context are limited only by the size of the context memory.

Alternatively, the user may switch between two predefined register sets A and B by writing to a context switch change bit. When the context switch is configured to context A the sensor will reference the context A registers. If the context switch is changed from A to B during the readout of frame n, the sensor will then reference the context B coarse\_integration\_time registers in frame n+1 and all other context B registers at the beginning of reading frame n+2. The sensor will show the same behavior when changing from context B to context A. The registers listed in Table 5 are context-switchable:

**Table 5. LIST OF CONFIGURABLE REGISTERS FOR CONTEXT A AND CONTEXT B**

| Context A                | Context B                   |
|--------------------------|-----------------------------|
| Register Description     | Register Description        |
| coarse_integration_time  | coarse_integration_time_cb  |
| line_length_pck          | line_length_pck_cb          |
| frame_length_lines       | frame_length_lines_cb       |
| row_bin                  | row_bin_cb                  |
| col_bin                  | col_bin_cb                  |
| fine_gain                | fine_gain_cb                |
| coarse_gain              | coarse_gain_cb              |
| coarse_integration_time2 | coarse_integration_time2_cb |
| dcg_manual_set           | dcg_manual_set_cb           |
| dcg_manual_set_t1        | dcg_manual_set_t1_cb        |
| bypass_pix_comb          | bypass_pix_cb               |
| coarse_gain_t1           | coarse_gain_t1_cb           |
| fine_gain_t1             | fine_gain_t1_cb             |
| x_addr_start             | x_addr_start_cb             |
| y_addr_start             | y_addr_start_cb             |
| x_addr_end               | x_addr_end_cb               |
| y_addr_end               | y_addr_end_cb               |
| y_odd_inc                | y_odd_inc_cb                |
| x_odd_inc                | x_odd_inc_cb                |
| green1_gain              | green1_gain_cb              |
| blue_gain                | blue_gain_cb                |
| red_gain                 | red_gain_cb                 |
| green2_gain              | green2_gain_cb              |
| global_gain              | global_gain_cb              |
| operation_mode_ctrl      | operation_mode_ctrl_cb      |
| bypass_pix_comb          | bypass_pix_comb_cb          |

## ANALOG/DIGITAL GAINS

A programmable analog gain of 1.0x to 16x (linear and HDR) applied simultaneously to all color channels will be featured along with a digital gain of 1x to 16x that may be configured on a per color channel basis. Analog gain can be applied per exposure in line interleaved mode.

## SKIPPING/BINNING MODES

The AR0238 supports subsampling. Subsampling allows the sensor to read out a smaller set of active pixels by either skipping, binning, or summing pixels within the readout window. Horizontal binning is achieved in the digital readout. The sensor will sample the combined 2x adjacent pixels within the same color plane. Vertical row binning is applied in the pixel readout. Row binning can be configured as 2x rows within the same color plane. Pixel skipping can be configured up to 2x in both the x-direction and y-direction. Skipping pixels in the x-direction will not reduce the row time. Skipping pixels in the y direction will reduce the number of rows from the sensor effectively reducing the frame time. Skipping will introduce image artifacts from aliasing.

The AR0238 supports row wise vertical binning. Row wise vertical summing is only supported in monochrome sensors.

## CLOCKING OPTIONS

The sensor contains a phase-locked loop (PLL) that is used for timing generation and control. The required VCO clock frequency is attained through the use of a pre-PLL clock divider followed by a multiplier. The PLL multiplier should be an even integer. If an odd integer (M) is programmed, the PLL will default to the lower (M-1) value to maintain an even multiplier value. The multiplier is followed by a set of dividers used to generate the output clocks required for the sensor array, the pixel analog and digital readout paths, and the output parallel and serial interfaces. Use of the PLL is required when using the HiSPi interface.

## TEMPERATURE SENSOR

The AR0238 sensor has a built-in PTAT-based temperature sensor, accessible through registers, that is capable of measuring die junction temperature. The value read out from the temperature sensor register is an ADC output value that needs to be converted downstream to a final temperature value in degrees Celsius. Since the PTAT device characteristic response is quite linear in the temperature range of operation required, a simple linear function can be used to convert the ADC output value to the final temperature in degrees Celsius.

A single reference point will be made available via register read as well as a slope for back-calculating the junction temperature value. An error of +/-5% or better over the full specified operating range of the sensor is to be expected.

## SILICON / FIRMWARE / SEQUENCER REVISION INFORMATION

A revision register will be provided to read out (via I<sup>2</sup>C) silicon and sequencer/OTPM revision information. This will be helpful to distinguish among different lots of material if there are future OTPM or sequencer revisions.

## LENS SHADING CORRECTION

The latest lens shading correction algorithm will be included for potential low Z height applications.

## COMPRESSION

When the AR0238 is configured for linear mode operation, the sensor can optionally compress 12-bit data to 10-bit using A-law compression. The A-law compression is disabled by default.

## PACKAGING

The AR0238 will be offered in a 11.43 x 11.43 48-Lead mPLCC package.

## PARALLEL INTERFACE

The parallel pixel data interface uses these output-only signals:

- FRAME\_VALID
- LINE\_VALID
- PIXCLK
- DOUT[11:0]

## HIGH SPEED SERIAL PIXEL (HiSPi) INTERFACE

The HiSPi interface supports three protocols, Streaming-S, Streaming-SP, and Packetized SP. The streaming protocols conform to a standard video application where each line of active or intra-frame blanking provided by the sensor is transmitted at the same length. The Packetized SP protocol will transmit only the active data ignoring line-to-line and frame-to-frame blanking data.

The HiSPi interface building block is a unidirectional differential serial interface with four data and one double data rate (DDR) clock lanes. One clock for every four serial data lanes is provided for phase alignment across multiple lanes. The AR0238 supports serial data widths of 10 or 12 bits on one, two, or four lanes. The specification includes a DLL to compensate for differences in group delay for each data lane. The DLL is connected to the clock lane and each data lane, which acts as a control master for the output delay buffers. Once the DLL has gained phase lock, each lane can be delayed in

1/8 unit interval (UI) steps. This additional delay allows the user to increase the setup or hold time at the receiver circuits and can be used to compensate for skew introduced in PCB design. Delay compensation may be set for clock and/or data lines in the hispi\_timing register R0x31C0. If the DLL timing adjustment is not required, the data and clock lane delay settings should be set to a default code of 0x0000 to reduce jitter, skew, and power dissipation.

### SENSOR CONTROL INTERFACE

The two-wire serial interface bus enables read/write access to control and status registers within the AR0238. The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (SCLK) that is an input to the sensor and is used to synchronize transfers.

Data is transferred between the master and the slave on a bidirectional signal (SDATA). SDATA is pulled up to VDD\_IO off-chip by a 1.5 k $\Omega$  resistor. Either the slave or master

device can drive SDATA LOW—the interface protocol determines which device is allowed to drive SDATA at any given time. The two-wire serial interface can run at 100 kHz or 400 kHz.

### T1/T2 LINE INTERLEAVED MODE

The AR0238 outputs the T1 and T2 exposures separately, in a line interleaved format. The purpose of this is to enable off chip HDR linear combination and processing. See the AR0238 Developer Guide for more information.

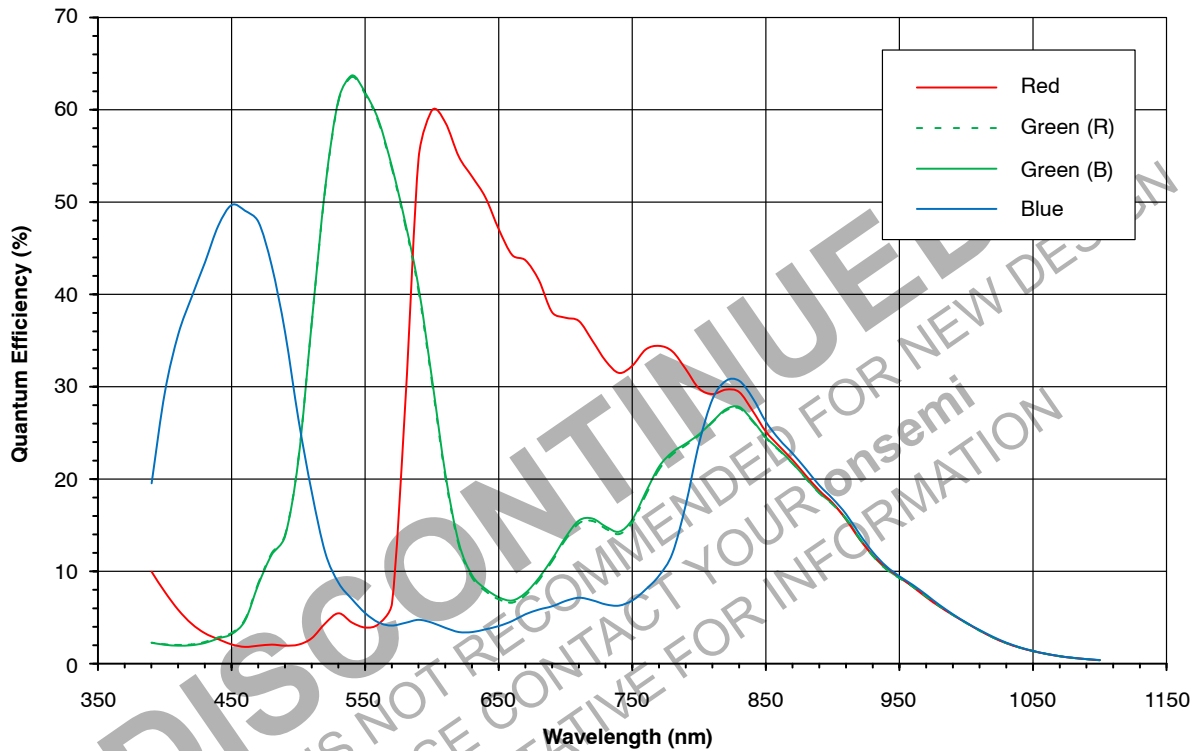


Figure 10. Quantum Efficiency - RGB

# AR0238

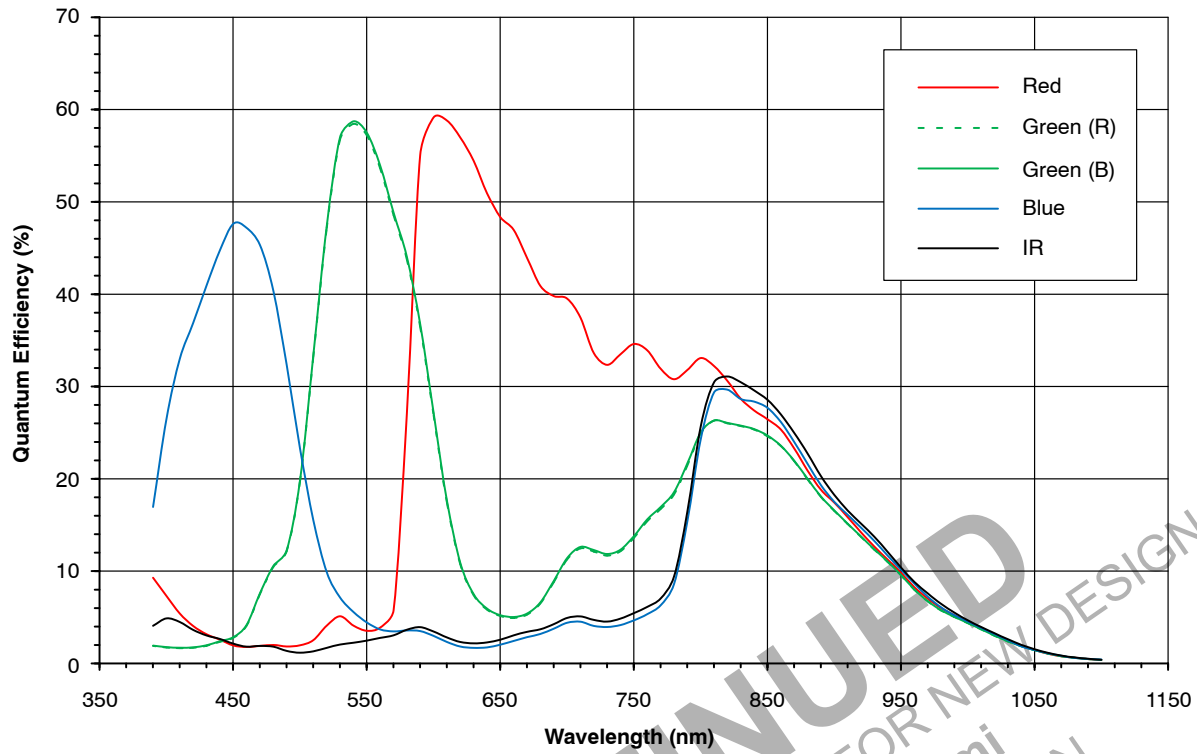
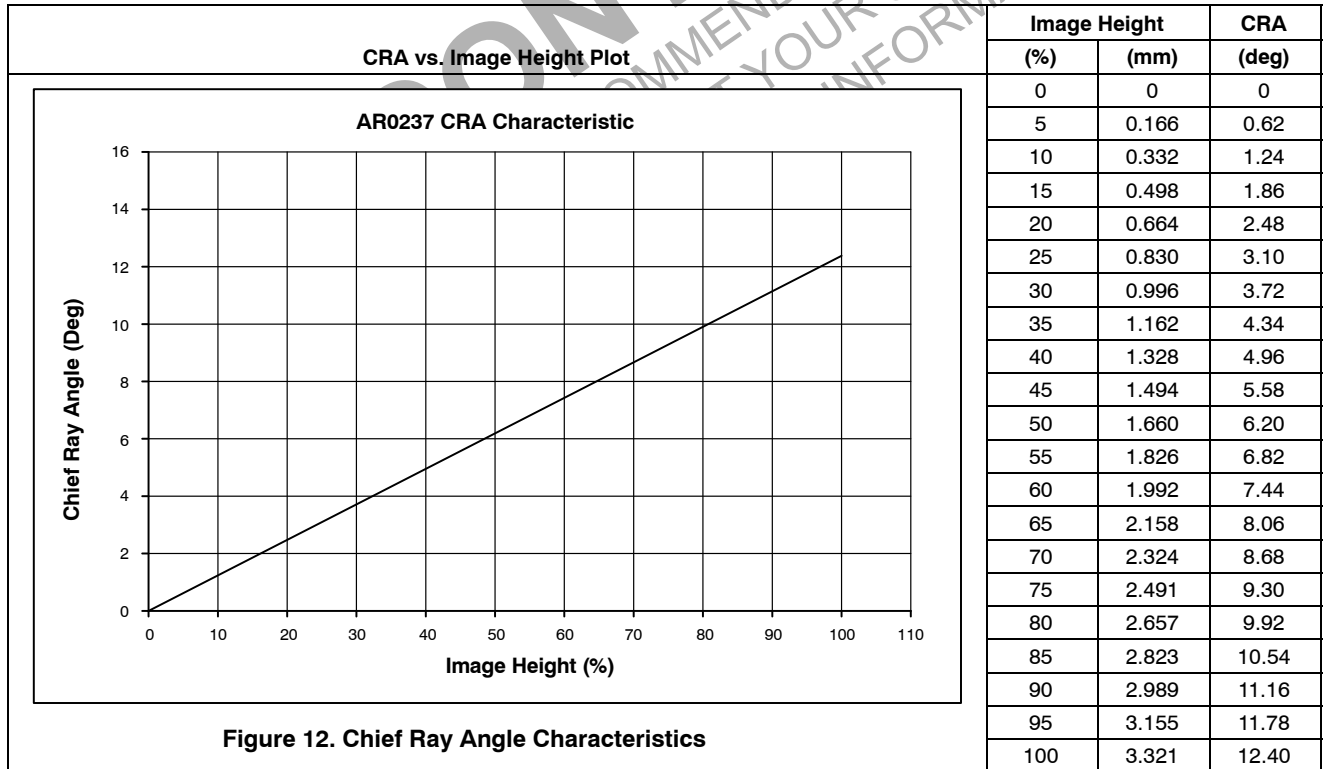


Figure 11. Quantum Efficiency - RGB-IR



## ELECTRICAL SPECIFICATIONS

Unless otherwise stated, the following specifications apply under the following conditions:

$$V_{DD} = 1.8 \text{ V } -0.10/+0.15;$$
$$\text{VDD\_IO} = \text{VDD\_PLL} = \text{VAA} = \text{VAA\_PIX} = 2.8 \text{ V} \pm 0.3 \text{ V};$$
$$\text{VDD\_SLVS} = 0.4 \text{ V} - 0.1/+0.2;$$

TA =  $-30^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ;

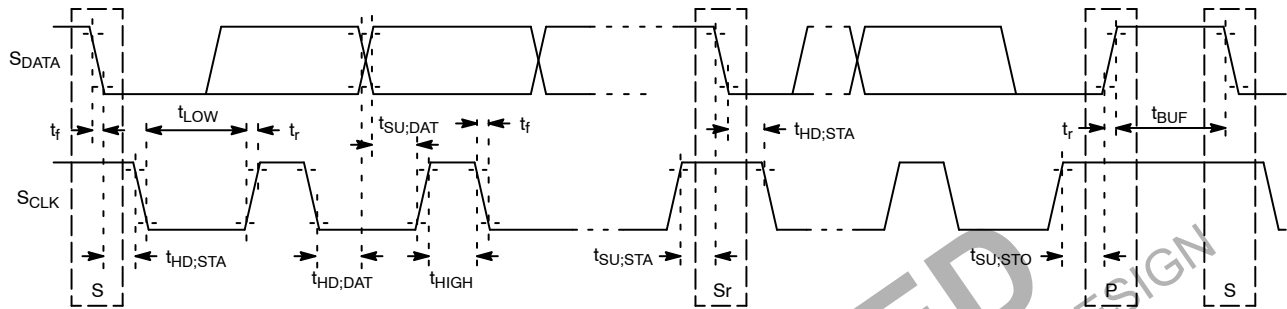
Output load = 10 pF;

Frequency = 74.25 MHz;

HiSPi off.

## TWO-WIRE SERIAL REGISTER INTERFACE

The electrical characteristics of the two-wire serial register interface (SCLK, SDATA) are shown in Figure 13 and Table 6.



NOTE: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

### Figure 13. Two-Wire Serial Bus Timing Parameters

**Table 6. Two-Wire Serial Bus Characteristics**fEXTCLK = 27 MHz; VDD = 1.8 V; VDD\_IO = 2.8 V; VAA = 2.8 V; VAA\_PIX = 2.8 V; VDD\_PLL = 2.8 V; T<sub>A</sub> = 25°C

| Parameter                                                                                   | Symbol   | Standard Mode  |                   | Fast Mode               |                  | Unit |
|---------------------------------------------------------------------------------------------|----------|----------------|-------------------|-------------------------|------------------|------|
|                                                                                             |          | Min            | Max               | Min                     | Max              |      |
| SCLK Clock Frequency                                                                        | fSCL     | 0              | 100               | 0                       | 400              | KHz  |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated | tHD;STA  | 4.0            | –                 | 0.6                     | –                | μs   |
| LOW period of the SCLK clock                                                                | tLOW     | 4.7            | –                 | 1.3                     | –                | μs   |
| HIGH period of the SCLK clock                                                               | tHIGH    | 4.0            | –                 | 0.6                     | –                | μs   |
| Set-up time for a repeated START condition                                                  | tSU;STA  | 4.7            | –                 | 0.6                     | –                | μs   |
| Data hold time                                                                              | tHD;DAT  | 0<br>(Note 11) | 3.45<br>(Note 12) | 0 (Note 13)             | 0.9<br>(Note 12) | μs   |
| Data set-up time                                                                            | tSU;DAT  | 250            | –                 | 100 (Note 13)           | –                | ns   |
| Rise time of both SDATA and SCLK signals                                                    | tr       | –              | 1000              | 20 + 0.1Cb<br>(Note 14) | 300              | ns   |
| Fall time of both SDATA and SCLK signals                                                    | tf       | –              | 300               | 20 + 0.1Cb<br>(Note 14) | 300              | ns   |
| Set-up time for STOP condition                                                              | tSU;STO  | 4.0            | –                 | 0.6                     | –                | μs   |
| Bus free time between a STOP and START condition                                            | tBUF     | 4.7            | –                 | 1.3                     | –                | μs   |
| Capacitive load for each bus line                                                           | Cb       | –              | 400               | –                       | 400              | pF   |
| Serial interface input pin capacitance                                                      | CIN_SI   | –              | 3.3               | –                       | 3.3              | pF   |
| SDATA max load capacitance                                                                  | CLOAD_SD | –              | 30                | –                       | 30               | pF   |
| SDATA pull-up resistor                                                                      | RSD      | 1.5            | 4.7               | 1.5                     | 4.7              | kΩ   |

8. This table is based on I2C standard (v2.1 January 2000), Philips Semiconductor.

9. Two-wire control is I2C-compatible.

10. All values referred to VIHmin = 0.9 VDD and VILmax = 0.1 VDD levels. Sensor EXCLK = 27 MHz.

11. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of SCLK.

12. The maximum tHD;DAT has only to be met if the device does not stretch the LOW period (tLOW) of the SCLK signal.

13. A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement tSU;DAT 250 ns must then be met.

This will automatically be the case if the device does not stretch the LOW period of the SCLK signal. If such a device does stretch the LOW period of the SCLK signal, it must output the next data bit to the SDATA line  $t_{r\max} + t_{SU;DAT} = 1000 + 250 = 1250$  ns (according to the Standard-mode I2C-bus specification) before the SCLK line is released.

14. Cb = total capacitance of one bus line in pF.

## I/O TIMING

By default, the AR0238 launches pixel data, FV, and LV with the falling edge of PIXCLK. The expectation is that the user captures DOUT[11:0], FV, and LV using the rising edge of PIXCLK.

See Figure 14 below and Table 7 on page 19 for I/O timing (AC) characteristics.

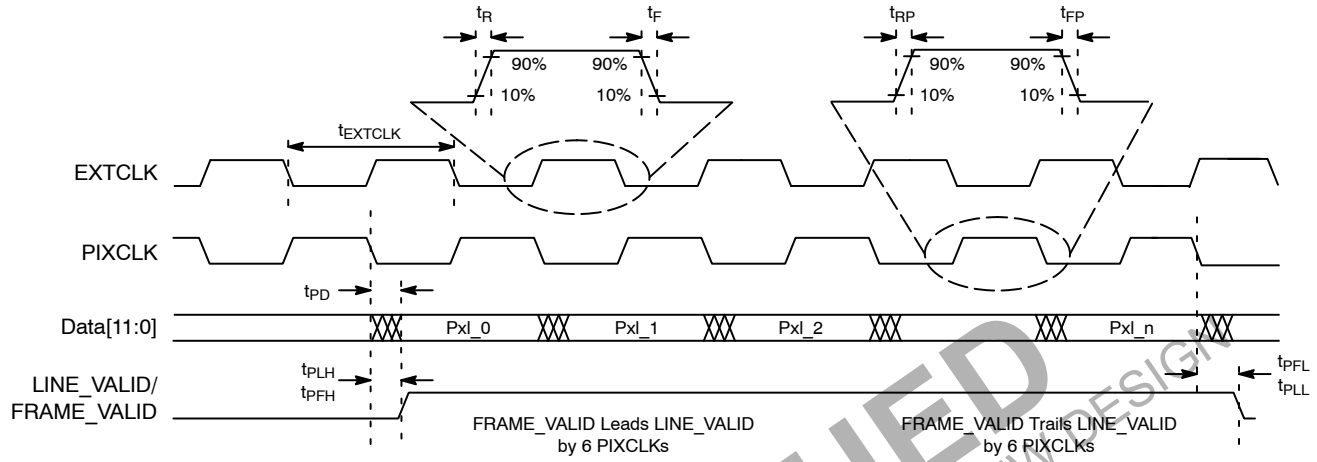


Figure 14. I/O Timing Diagram

Table 7. I/O TIMING CHARACTERISTICS

| Symbol         | Definition                         | Condition                      | Min  | Typ  | Max   | Unit |
|----------------|------------------------------------|--------------------------------|------|------|-------|------|
| $f_{EXTCLK1s}$ | Input Clock Frequency              |                                | 6    | –    | 48    | MHz  |
| $t_{EXTCLK1}$  | Input Clock Period                 |                                | 20.8 | –    | 166   | ns   |
| $t_R$          | Input Clock Rise Time              |                                | –    | 3    | –     | ns   |
| $t_F$          | Input Clock Fall Time              |                                | –    | 3    | –     | ns   |
| $t_{RP}$       | Pixclk Rise Time                   |                                | 2    | 3.5  | 5     | ns   |
| $t_{FP}$       | Pixclk Fall Time                   |                                | 2    | 3.5  | 5     | ns   |
|                | Clock Duty Cycle                   |                                | 45   | 50   | 55    | %    |
| $t_{CP}$       | EXTCLK to PIXCLK Propagation Delay | Nominal Voltages, PLL Disabled | 10   | 14   | 18    | ns   |
| $f_{PIXCLK}$   | PIXCLK Frequency                   | Default, Nominal Voltages      | 6    | –    | 74.25 | MHz  |
| $t_{PD}$       | PIXCLK to Data Valid               | Default, Nominal Voltages      | 0    | 2.5  | 5     | ns   |
| $t_{PFH}$      | PIXCLK to FV HIGH                  | Default, Nominal Voltages      | –2   | 3    | 6     | ns   |
| $t_{PLH}$      | PIXCLK to LV HIGH                  | Default, Nominal Voltages      | –2   | 3    | 6     | ns   |
| $t_{PFL}$      | PIXCLK to FV LOW                   | Default, Nominal Voltages      | –2   | 2.5  | 6     | ns   |
| $t_{PLL}$      | PIXCLK to LV LOW                   | Default, Nominal Voltages      | –2   | 2.5  | 6     | ns   |
| $C_{LOAD}$     | Output Load Capacitance            |                                | –    | < 10 | –     | pF   |
| $C_{IN}$       | Input Pin Capacitance              |                                | –    | 2.5  | –     | pF   |

NOTE: I/O timing characteristics are measured under the following conditions:

- Temperature is 25°C ambient
- 10 pF load
- 1.8 V I/O supply voltage

**DC ELECTRICAL CHARACTERISTICS**

The DC electrical characteristics are shown in the tables below.

**Table 8. DC ELECTRICAL CHARACTERISTICS**

| Symbol   | Definition            | Condition                                 | Min        | Typ     | Max        | Unit |
|----------|-----------------------|-------------------------------------------|------------|---------|------------|------|
| VDD      | Core digital voltage  |                                           | 1.7        | 1.8     | 1.95       | V    |
| VDD_IO   | I/O digital voltage   |                                           | 1.7/2.5    | 1.8/2.8 | 1.9/3.1    | V    |
| VAA      | Analog voltage        |                                           | 2.5        | 2.8     | 3.1        | V    |
| VAA_PIX  | Pixel supply voltage  |                                           | 2.5        | 2.8     | 3.1        | V    |
| VDD_PLL  | PLL supply voltage    |                                           | 2.5        | 2.8     | 3.1        | V    |
| VDD_SLVS | HiSPi supply voltage  |                                           | 0.3        | 0.4     | 0.6        | V    |
| VIH      | Input HIGH voltage    |                                           | VDD_IO*0.7 | –       | –          | V    |
| VIL      | Input LOW voltage     |                                           | –          | –       | VDD_IO*0.3 | V    |
| IIN      | Input leakage current | No pull-up resistor; VIN = VDD_IO or DGND | 20         | –       | –          | μA   |
| VOH      | Output HIGH voltage   |                                           | VDD_IO–0.3 | –       | –          | V    |
| VOL      | Output LOW voltage    |                                           | –          | –       | 0.4        | V    |
| IOH      | Output HIGH current   | At specified VOH                          | –22        | –       | –          | mA   |
| IOL      | Output LOW current    | At specified VOL                          | –          | –       | 22         | mA   |

**Table 9. ABSOLUTE MAXIMUM RATINGS**

| Symbol       | Definition                | Condition | Min  | Max | Unit |
|--------------|---------------------------|-----------|------|-----|------|
| VDD_MAX      | Core digital voltage      |           | –0.3 | 2.4 | V    |
| VDD_IO_MAX   | I/O digital voltage       |           | –0.3 | 4   | V    |
| VAA_MAX      | Analog voltage            |           | –0.3 | 4   | V    |
| VAA_PIX      | Pixel supply voltage      |           | –0.3 | 4   | V    |
| VDD_PLL      | PLL supply voltage        |           | –0.3 | 4   | V    |
| VDD_SLVS_MAX | HiSPi I/O digital voltage |           | –0.3 | 2.4 | V    |
| tST          | Storage temperature       |           | –40  | 85  | °C   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 10. 1080p30 LINEAR 74 MHZ PARALLEL 2.8 V**

(Operating currents are measured in mA at the following conditions:  $V_{AA} = V_{AA\_PIX} = V_{DD\_PLL} = V_{DD\_IO} = 2.8$  V;  $V_{DD} = 1.8$  V; PLL Enabled and PIXCLK = 74.25 MHz; Low power mode enabled;  $T_A = 25^\circ\text{C}$ )

| Definition                    | Condition         | Symbol        | Voltage      | Min   | Typ    | Max   | Unit |
|-------------------------------|-------------------|---------------|--------------|-------|--------|-------|------|
| Digital Operating Current     | Streaming 1080p30 | $I_{DD}$      | 1.8          | 20    | 34     | 50    | mA   |
| I/O Digital Operating Current | Streaming 1080p30 | $I_{DD\_IO}$  | 2.8          | 15    | 28     | 50    | mA   |
| Analog Operating Current      | Streaming 1080p30 | $I_{AA}$      | 2.8          | 15    | 26     | 50    | mA   |
| Pixel Supply Current          | Streaming 1080p30 | $I_{AA\_PIX}$ | 2.8          | 1     | 3      | 7     | mA   |
| PLL Supply Current            | Streaming 1080p30 | $I_{DD\_PLL}$ | 2.8          | 5.5   | 6.4    | 7     | mA   |
|                               |                   |               | <b>Power</b> | 138.2 | 238.72 | 409.2 | mW   |

**Table 11. 1080p30 LINEAR 74 MHZ PARALLEL 1.8 V**

(Operating currents are measured in mA at the following conditions:  $V_{AA} = V_{AA\_PIX} = V_{DD\_PLL} = 2.8$  V;  $V_{DD} = V_{DD\_IO} = 1.8$  V; PLL Enabled and PIXCLK = 74.25 MHz; Low power mode enabled;  $T_A = 25^\circ\text{C}$  Dark Image, 8x Analog Gain, HCG, 20 ms integration time)

| Definition                    | Condition         | Symbol        | Voltage      | Min   | Typ    | Max   | Unit |
|-------------------------------|-------------------|---------------|--------------|-------|--------|-------|------|
| Digital Operating Current     | Streaming 1080p30 | $I_{DD}$      | 1.8          | 20    | 34     | 50    | mA   |
| I/O Digital Operating Current | Streaming 1080p30 | $I_{DD\_IO}$  | 1.8          | 10    | 14     | 30    | mA   |
| Analog Operating Current      | Streaming 1080p30 | $I_{AA}$      | 2.8          | 15    | 26     | 50    | mA   |
| Pixel Supply Current          | Streaming 1080p30 | $I_{AA\_PIX}$ | 2.8          | 1     | 3      | 7     | mA   |
| PLL Supply Current            | Streaming 1080p30 | $I_{DD\_PLL}$ | 2.8          | 5.5   | 6.4    | 7     | mA   |
|                               |                   |               | <b>Power</b> | 114.2 | 185.52 | 323.2 | mW   |

**Table 12. 1080p30 LINEAR 74 MHZ HISPI SLVS**

(Operating currents are measured in mA at the following conditions:  $V_{AA} = V_{AA\_PIX} = V_{DD\_PLL} = 2.8$  V;  $V_{DD} = V_{DD\_IO} = 1.8$  V;  $V_{DD\_SLVS} = 0.4$  V; PLL Enabled and PIXCLK = 74.25 MHz; 4-lane HiSPi mode; Low power mode enabled;  $T_A = 25^\circ\text{C}$  Dark Image, 8x Analog Gain, HCG, 20 ms integration time)

| Definition                | Condition         | Symbol         | Voltage      | Min | Typ   | Max | Unit |
|---------------------------|-------------------|----------------|--------------|-----|-------|-----|------|
| Digital Operating Current | Streaming 1080p30 | $I_{DD}$       | 1.8          | 25  | 44    | 65  | mA   |
| Analog Operating Current  | Streaming 1080p30 | $I_{AA}$       | 2.8          | 15  | 26    | 50  | mA   |
| Pixel Supply Current      | Streaming 1080p30 | $I_{AA\_PIX}$  | 2.8          | 1   | 3     | 7   | mA   |
| PLL Supply Current        | Streaming 1080p30 | $I_{DD\_PLL}$  | 2.8          | 6   | 7.5   | 8.5 | mA   |
| SLVS Supply Current       | Streaming 1080p30 | $I_{DD\_SLVS}$ | 0.4          | 6   | 9.5   | 14  | mA   |
|                           |                   |                | <b>Power</b> | 109 | 185.2 | 306 | mW   |

**Table 13. 1080p30 LINEAR 74 MHZ HISPI HIV<sub>CM</sub>**

(Operating currents are measured in mA at the following conditions:  $V_{AA} = V_{AA\_PIX} = V_{DD\_PLL} = 2.8$  V;  $V_{DD} = V_{DD\_IO} = V_{DD\_SLVS} = 1.8$  V; PLL Enabled and PIXCLK = 74.25 MHz; 4-lane HiSPi mode; Low power mode enabled;  $T_A = 25^\circ\text{C}$  Dark Image, 8x Analog Gain, HCG, 20 ms integration time)

| Definition                | Condition         | Symbol         | Voltage      | Min   | Typ   | Max   | Unit |
|---------------------------|-------------------|----------------|--------------|-------|-------|-------|------|
| Digital Operating Current | Streaming 1080p30 | $I_{DD}$       | 1.8          | 25    | 44    | 65    | mA   |
| Analog Operating Current  | Streaming 1080p30 | $I_{AA}$       | 2.8          | 15    | 26    | 50    | mA   |
| Pixel Supply Current      | Streaming 1080p30 | $I_{AA\_PIX}$  | 2.8          | 1     | 3     | 7     | mA   |
| PLL Supply Current        | Streaming 1080p30 | $I_{DD\_PLL}$  | 2.8          | 6     | 7.5   | 8.5   | mA   |
| SLVS Supply Current       | Streaming 1080p30 | $I_{DD\_SLVS}$ | 1.8          | 12    | 20    | 35    | mA   |
|                           |                   |                | <b>Power</b> | 128.2 | 217.4 | 363.4 | mW   |

**Table 14. 1080p60 LINEAR 74 MHZ HISPI SLVS**

(Operating currents are measured in mA at the following conditions:  $V_{AA} = V_{AA\_PIX} = V_{DD\_PLL} = 2.8$  V;  $V_{DD} = V_{DD\_IO} = 1.8$  V;  $V_{DD\_SLVS} = 0.4$  V; PLL Enabled and PIXCLK = 74.25 MHz; 4-lane HiSPi mode;  $T_A = 25^\circ\text{C}$  Dark Image, 8× Analog Gain, HCG, 20 ms integration time)

| Definition                | Condition         | Symbol         | Voltage      | Min   | Typ | Max   | Unit |
|---------------------------|-------------------|----------------|--------------|-------|-----|-------|------|
| Digital Operating Current | Streaming 1080p60 | $I_{DD}$       | 1.8          | 50    | 88  | 130   | mA   |
| Analog Operating Current  | Streaming 1080p60 | $I_{AA}$       | 2.8          | 20    | 36  | 60    | mA   |
| Pixel Supply Current      | Streaming 1080p60 | $I_{AA\_PIX}$  | 2.8          | 1     | 4   | 8     | mA   |
| PLL Supply Current        | Streaming 1080p60 | $I_{DD\_PLL}$  | 2.8          | 7     | 8.5 | 9.5   | mA   |
| SLVS Supply Current       | Streaming 1080p60 | $I_{DD\_SLVS}$ | 0.4          | 6     | 9.5 | 14    | mA   |
|                           |                   |                | <b>Power</b> | 170.8 | 298 | 442.6 | mW   |

**Table 15. 1080p60 LINEAR 74 MHZ HISPI HIV<sub>CM</sub>**

(Operating currents are measured in mA at the following conditions:  $V_{AA} = V_{AA\_PIX} = V_{DD\_PLL} = 2.8$  V;  $V_{DD} = V_{DD\_IO} = 1.8$  V;  $V_{DD\_SLVS} = 1.8$  V; PLL Enabled and PIXCLK = 74.25 MHz; 4-lane HiSPi mode;  $T_A = 25^\circ\text{C}$  Dark Image, 8× Analog Gain, HCG, 20 ms integration time)

| Definition                | Condition         | Symbol         | Voltage      | Min | Typ   | Max | Unit |
|---------------------------|-------------------|----------------|--------------|-----|-------|-----|------|
| Digital Operating Current | Streaming 1080p60 | $I_{DD}$       | 1.8          | 50  | 88    | 130 | mA   |
| Analog Operating Current  | Streaming 1080p60 | $I_{AA}$       | 2.8          | 20  | 36    | 60  | mA   |
| Pixel Supply Current      | Streaming 1080p60 | $I_{AA\_PIX}$  | 2.8          | 1   | 4     | 8   | mA   |
| PLL Supply Current        | Streaming 1080p60 | $I_{DD\_PLL}$  | 2.8          | 7   | 8.5   | 9.5 | mA   |
| SLVS Supply Current       | Streaming 1080p60 | $I_{DD\_SLVS}$ | 1.8          | 12  | 20    | 35  | mA   |
|                           |                   |                | <b>Power</b> | 190 | 330.2 | 500 | mW   |

**Table 16. 1080p30 LINE-INLEAVED 74MHZ HISPI SLVS**

(Operating currents are measured in mA at the following conditions:  $V_{AA} = V_{AA\_PIX} = V_{DD\_PLL} = 2.8$  V;  $V_{DD} = V_{DD\_IO} = 1.8$  V;  $V_{DD\_SLVS} = 0.4$  V; PLL Enabled and PIXCLK = 74.25 MHz; 4-lane HiSPi mode;  $T_A = 25^\circ\text{C}$  Dark Image, 8× Analog Gain, HCG, 20 ms integration time)

| Definition                | Condition         | Symbol         | Voltage      | Min   | Typ | Max   | Unit |
|---------------------------|-------------------|----------------|--------------|-------|-----|-------|------|
| Digital Operating Current | Streaming 1080p30 | $I_{DD}$       | 1.8          | 50    | 88  | 130   | mA   |
| Analog Operating Current  | Streaming 1080p30 | $I_{AA}$       | 2.8          | 20    | 36  | 60    | mA   |
| Pixel Supply Current      | Streaming 1080p30 | $I_{AA\_PIX}$  | 2.8          | 1     | 4   | 8     | mA   |
| PLL Supply Current        | Streaming 1080p30 | $I_{DD\_PLL}$  | 2.8          | 7     | 8.5 | 9.5   | mA   |
| SLVS Supply Current       | Streaming 1080p30 | $I_{DD\_SLVS}$ | 0.4          | 6     | 9.5 | 14    | mA   |
|                           |                   |                | <b>Power</b> | 170.8 | 298 | 442.6 | mW   |

**Table 17. 1080p30 LINE-INLEAVED 74MHZ HISPI HIV<sub>CM</sub>**

(Operating currents are measured in mA at the following conditions:  $V_{AA} = V_{AA\_PIX} = V_{DD\_PLL} = 2.8$  V;  $V_{DD} = V_{DD\_IO} = 1.8$  V;  $V_{DD\_SLVS} = 1.8$  V; PLL Enabled and PIXCLK = 74.25 MHz; 4-lane HiSPi mode;  $T_A = 25^\circ\text{C}$  Dark Image, 8× Analog Gain, HCG, 20 ms integration time)

| Definition                | Condition         | Symbol         | Voltage      | Min | Typ   | Max | Unit |
|---------------------------|-------------------|----------------|--------------|-----|-------|-----|------|
| Digital Operating Current | Streaming 1080p30 | $I_{DD}$       | 1.8          | 50  | 88    | 130 | mA   |
| Analog Operating Current  | Streaming 1080p30 | $I_{AA}$       | 2.8          | 20  | 36    | 60  | mA   |
| Pixel Supply Current      | Streaming 1080p30 | $I_{AA\_PIX}$  | 2.8          | 1   | 4     | 8   | mA   |
| PLL Supply Current        | Streaming 1080p30 | $I_{DD\_PLL}$  | 2.8          | 7   | 8.5   | 9.5 | mA   |
| SLVS Supply Current       | Streaming 1080p30 | $I_{DD\_SLVS}$ | 1.8          | 12  | 20    | 35  | mA   |
|                           |                   |                | <b>Power</b> | 190 | 330.2 | 500 | mW   |

**HiSPi ELECTRICAL SPECIFICATIONS**

The ON Semiconductor AR0238 sensor supports both SLVS and HiVCM HiSPi modes. Refer to the High-Speed Serial Pixel (HiSPi) Interface Physical Layer Specification v2.00.00 for electrical definitions, specifications, and timing information. The VDD\_SLVS supply in this datasheet

corresponds to VDD\_TX in the HiSPi Physical Layer Specification. Similarly, VDD is equivalent to VDD\_HiSPi as referenced in the specification. The DLL as implemented on AR0238 is limited in the number of available delay steps and differs from the HiSPi specification as described in this section.

**Table 18. CHANNEL SKEW**

Measurement Conditions: VDD\_HiSPi = 1.8 V; VDD\_HiSPi\_TX = 0.4V; Data Rate = 480 Mbps;  
DLL set to 0

|                                      |             |      |    |
|--------------------------------------|-------------|------|----|
| Data Lane Skew in Reference to Clock | tCHSKEW1PHY | -150 | ps |
|--------------------------------------|-------------|------|----|

**DISCONTINUED**  
THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN  
PLEASE CONTACT YOUR onsemi  
REPRESENTATIVE FOR INFORMATION

## POWER-ON RESET AND STANDBY TIMING

## POWER-UP SEQUENCE

The recommended power-up sequence for the AR0238 is shown in Figure 15. The available power supplies (VDD\_IO, VDD, VDD\_SLVS, VDD\_PLL, VAA, VAA\_PIX) must have the separation specified below.

1. Turn on VDD\_PLL power supply.
2. After 100  $\mu$ s, turn on VAA and VAA\_PIX power supply.
3. After 100  $\mu$ s, turn on VDD\_IO power supply.
4. After 100  $\mu$ s, turn on VDD power supply.
5. After 100  $\mu$ s, turn on VDD\_SLVS power supply.
6. After the last power supply is stable, enable EXTCLK.
7. Assert RESET\_BAR for at least 1 ms. The parallel interface will be tri-stated during this time.
8. Wait 150000 EXTCLKs (for internal initialization into software standby).
9. Configure PLL, output, and image settings to desired values.
10. Wait 1ms for the PLL to lock.
11. Set streaming mode (R0x301a[2] = 1).

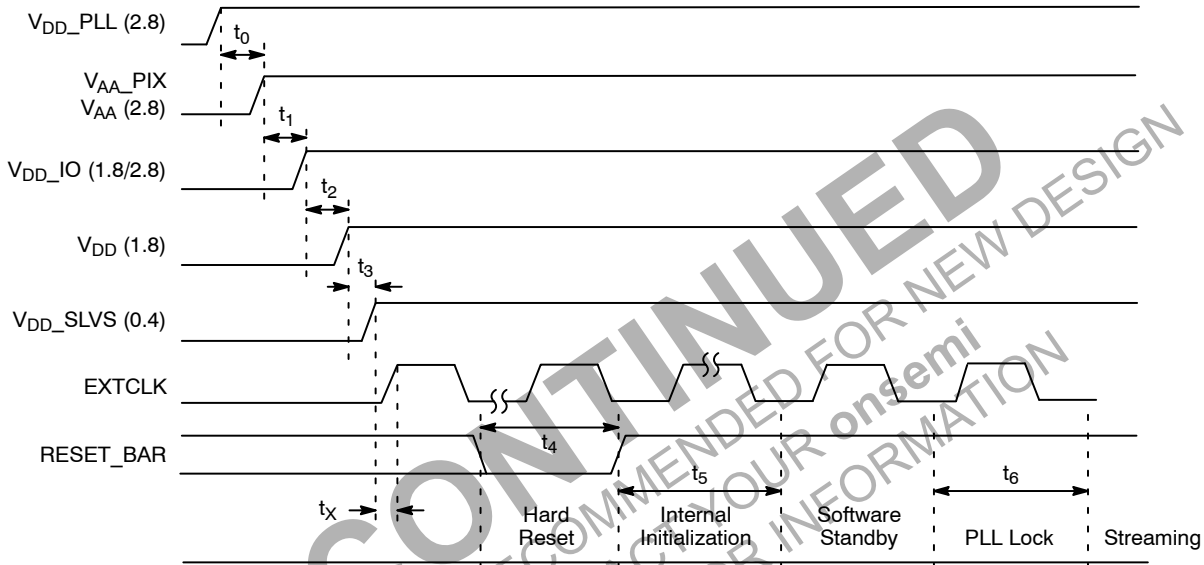


Figure 15. Power Up

Table 19. POWER-UP SEQUENCE

| Definition                       | Symbol | Min            | Typ             | Max | Unit    |
|----------------------------------|--------|----------------|-----------------|-----|---------|
| VDD_PLL to VAA/VAA_PIX (Note 17) | t0     | 0              | 100             | –   | $\mu$ s |
| VAA/VAA_PIX to VDD_IO            | t1     | 0              | 100             | –   | $\mu$ s |
| VDD_IO to VDD                    | t2     | 0              | 100             | –   | $\mu$ s |
| VDD to VDD_SLVS                  | t3     | 0              | 100             | –   | $\mu$ s |
| Xtal settle time                 | tx     | –              | 30<br>(Note 15) | –   | ms      |
| Hard Reset                       | t4     | 1<br>(Note 16) | –               | –   | ms      |
| Internal Initialization          | t5     | 150000         | –               | –   | EXTCLKs |
| PLL Lock Time                    | t6     | 1              | –               | –   | ms      |

15. Xtal settling time is component-dependent, usually taking about 10 – 100 ms.

16. Hard reset time is the minimum time required after power rails are settled. In a circuit where Hard reset is held down by RC circuit, then the RC time must include the all power rail settle time and Xtal settle time.

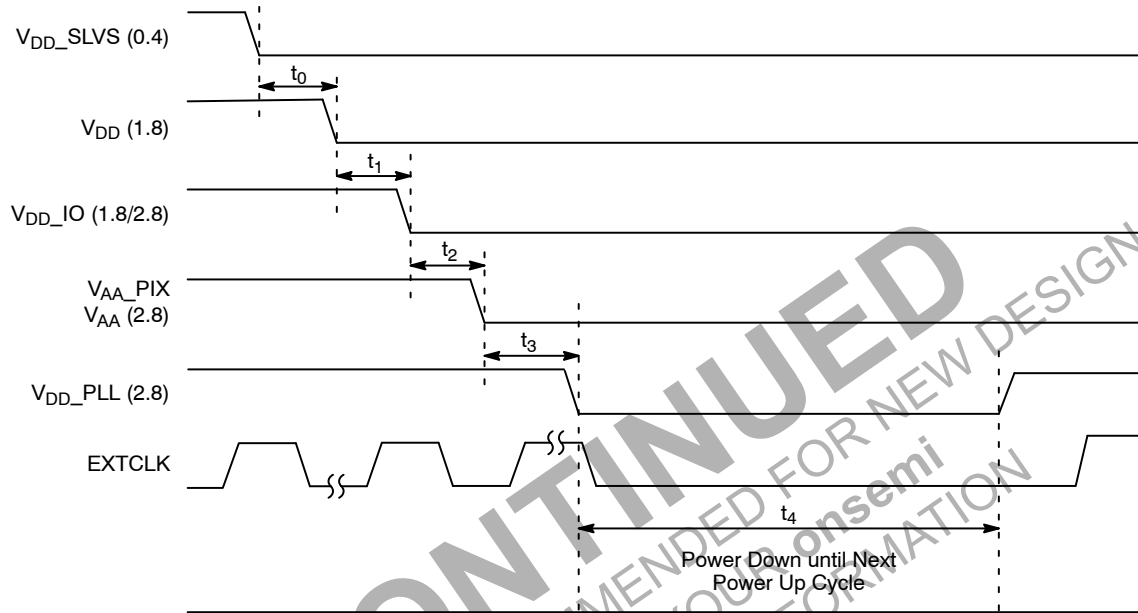
17. It is critical that VDD\_PLL is not powered up after the other power supplies. It must be powered before or at least at the same time as the others. If the case happens that VDD\_PLL is powered after other supplies then sensor may have functionality issues and will experience high current draw on this supply.

**POWER-DOWN SEQUENCE**

The recommended power-down sequence for the AR0238 is shown in Figure 16. The available power supplies (VDD\_IO, VDD, VDD\_SLVS, VDD\_PLL, VAA, VAA\_PIX) must have the separation specified below.

1. Disable streaming if output is active by setting standby R0x301a[2] = 0

2. The soft standby state is reached after the current row or frame, depending on configuration, has ended.
3. Turn off VDD\_SLVS.
4. Turn off VDD.
5. Turn off VDD\_IO.
6. Turn off VAA/VAA\_PIX.
7. Turn off VDD\_PLL.



**Figure 16. Power Down**

**Table 20. POWER-DOWN SEQUENCE**

| Definition                          | Symbol | Min | Typ | Max | Unit |
|-------------------------------------|--------|-----|-----|-----|------|
| VDD_SLVS to VDD                     | t0     | 0   | –   | –   | μs   |
| VDD to VDD_IO                       | t1     | 0   | –   | –   | μs   |
| VDD_IO to VAA/VAA_PIX               | t2     | 0   | –   | –   | μs   |
| VAA/VAA_PIX to VDD_PLL              | t3     | 0   | –   | –   | μs   |
| Power Down until Next Power Up Time | t4     | 100 | –   | –   | ms   |

NOTE: t4 is required between power down and next power up time; all decoupling caps from regulators must be completely discharged.

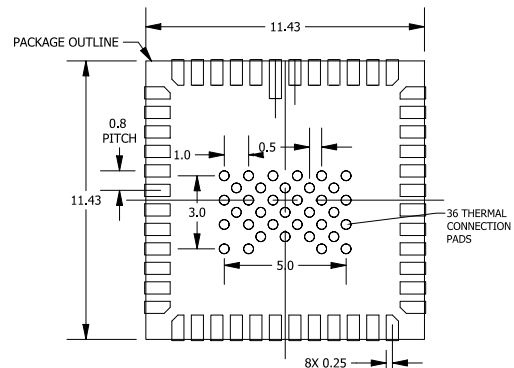
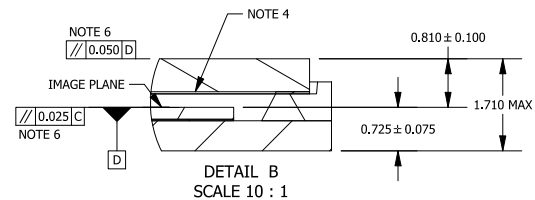
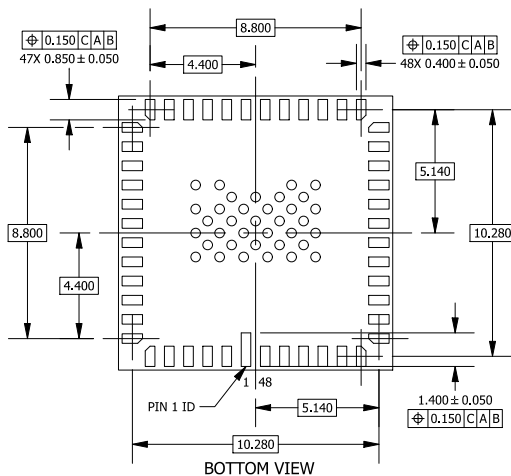
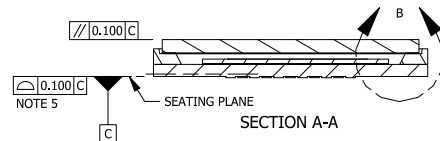
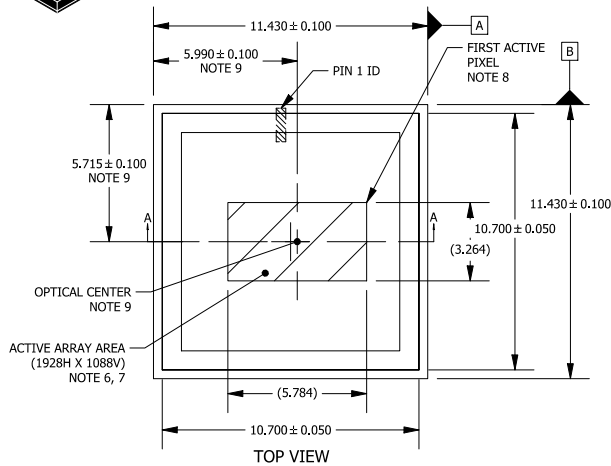
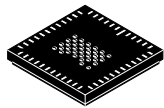
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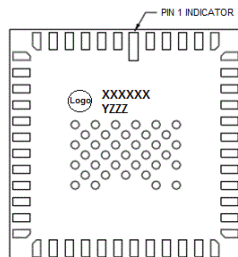
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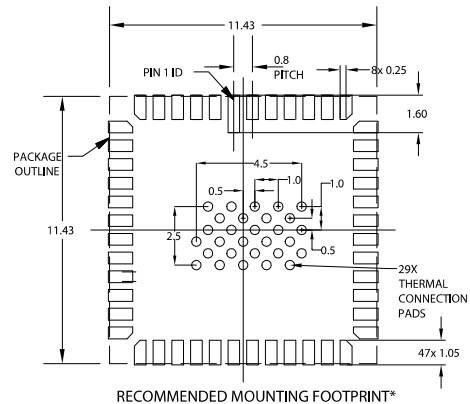
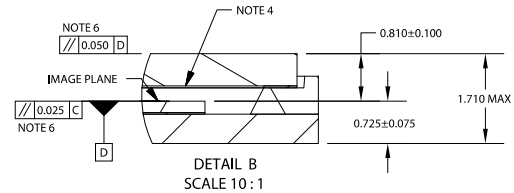
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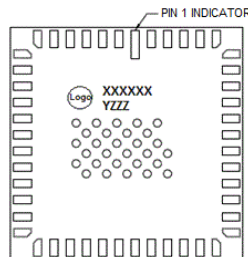
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