MP5048A

60V, 4A, 14mΩ $R_{DS(ON)}$, Hot-Swap Intelli-Fuse Solution

DESCRIPTION

The MP5048A is a monolithic, integrated controller and switch. It contains a power MOSFET and circuitry that enable it to operate as a standalone device, or to be controlled by a hot-swap controller. The MP5048A is capable of driving up to 4A of continuous current per device.

The device limits the inrush current to the load when a circuit card is inserted into a live backplane power source. This limits the backplane's voltage drop. The MP5048A also limits the internal MOSFET current by controlling the gate voltage (V_{GATE}) via the current-limit reference input.

The MP5048A offers many features to simplify system design. Its integrated solution monitors the output current (I_{OUT}) and die temperature, which eliminates the need for an external current-sense resistor, power MOSFET, or thermal sensing.

The MP5048A detects the power MOSFET gate, source, and drain short conditions to provide feedback for the controller. The device can be paralleled for higher current applications.

The MP5048A is available in a QFN-30 (5mmx5mm) package.

FEATURES

- 24V to 60V Operating Input Voltage (V_{IN}) Range
- 4A Maximum Output Current (I_{OUT})
- 14mΩ Integrated Power MOSFET
- Built-In MOSFET Driver
- Integrated Current Sensing with Sense Output
- Separate Current-Sense Output to Configure the Over-Current Limit
- Built-In Soft Start (SS) and Insertion Delay
- Output Short-Circuit Protection (SCP)
- Over-Temperature Protection (OTP)
- Built-In Fuse Health Diagnostics
- Fault Signal Output
- Parallel Operation for Higher Current Applications
- Integrated Intelli-Fuse Temperature Sensing
- Output Voltage (V_{OUT}) Shutdown Control
- Available in a QFN-30 (5mmx5mm) Package

APPLICATIONS

- Industrial Applications
- Servers
- Networking

TYPICAL APPLICATIONS

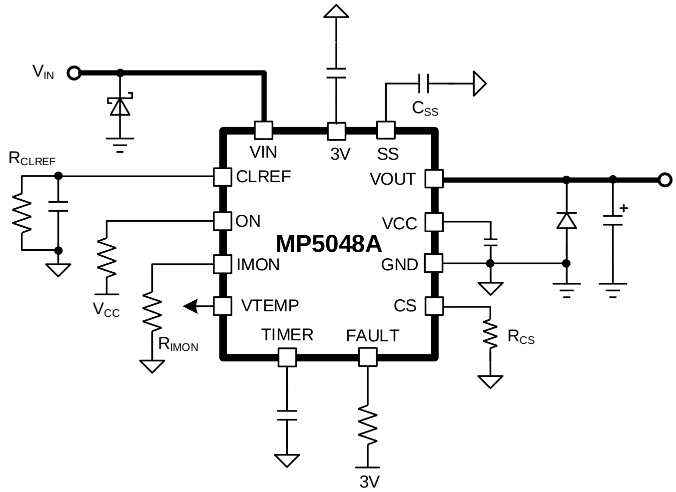


Figure 1: Standalone Operation ($R_{IMON} \geqslant R_{CS}$)

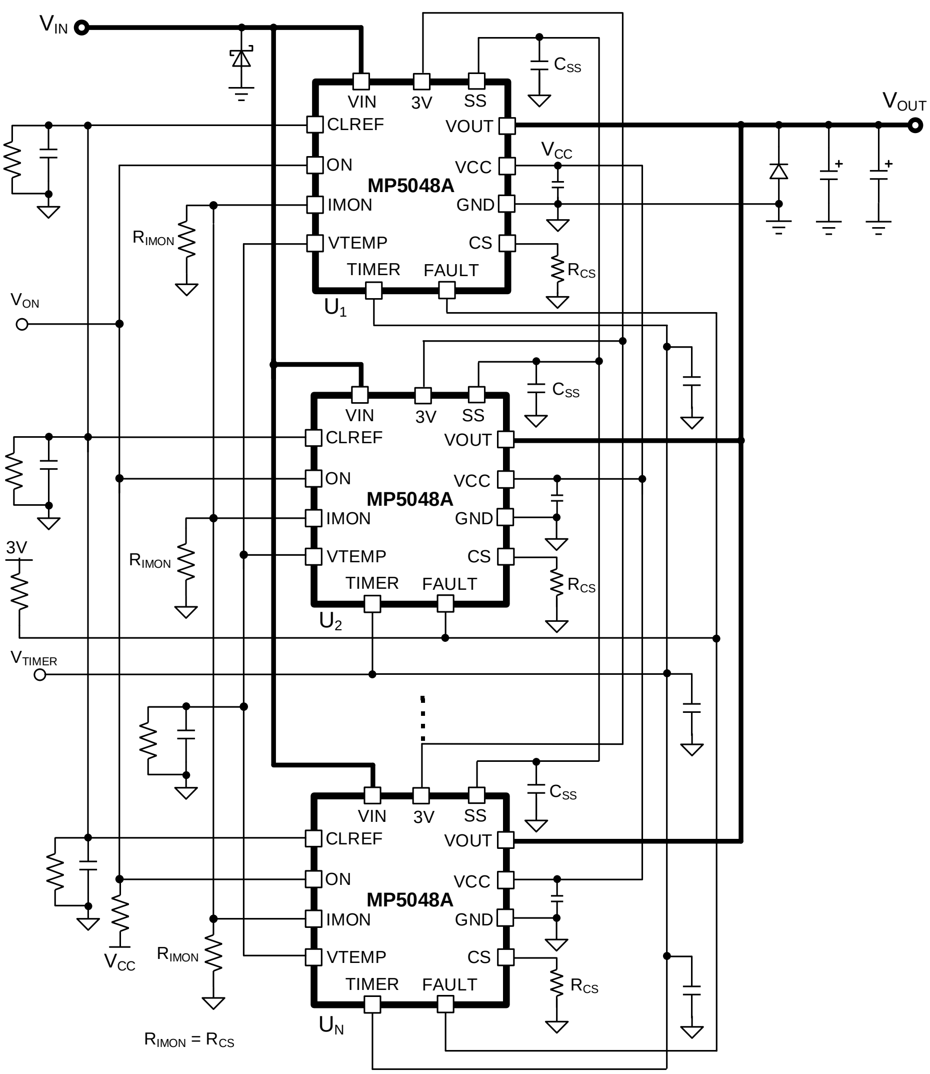


Figure 2: Parallel Operation

TYPICAL APPLICATIONS *(continued)*

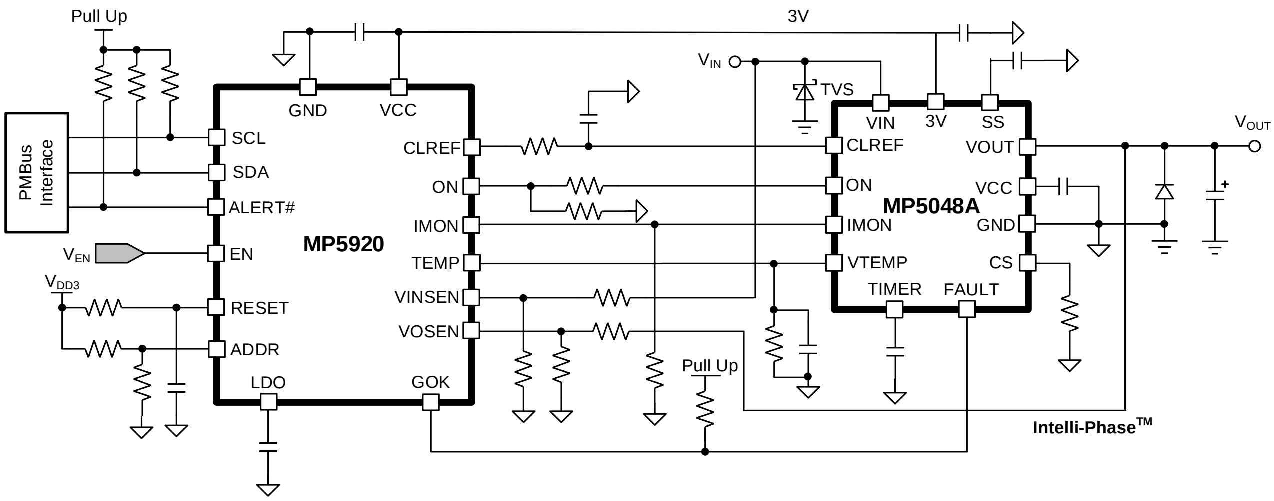


Figure 3: MP5048A Controlled by Hot-Swap Controller (MP5920)

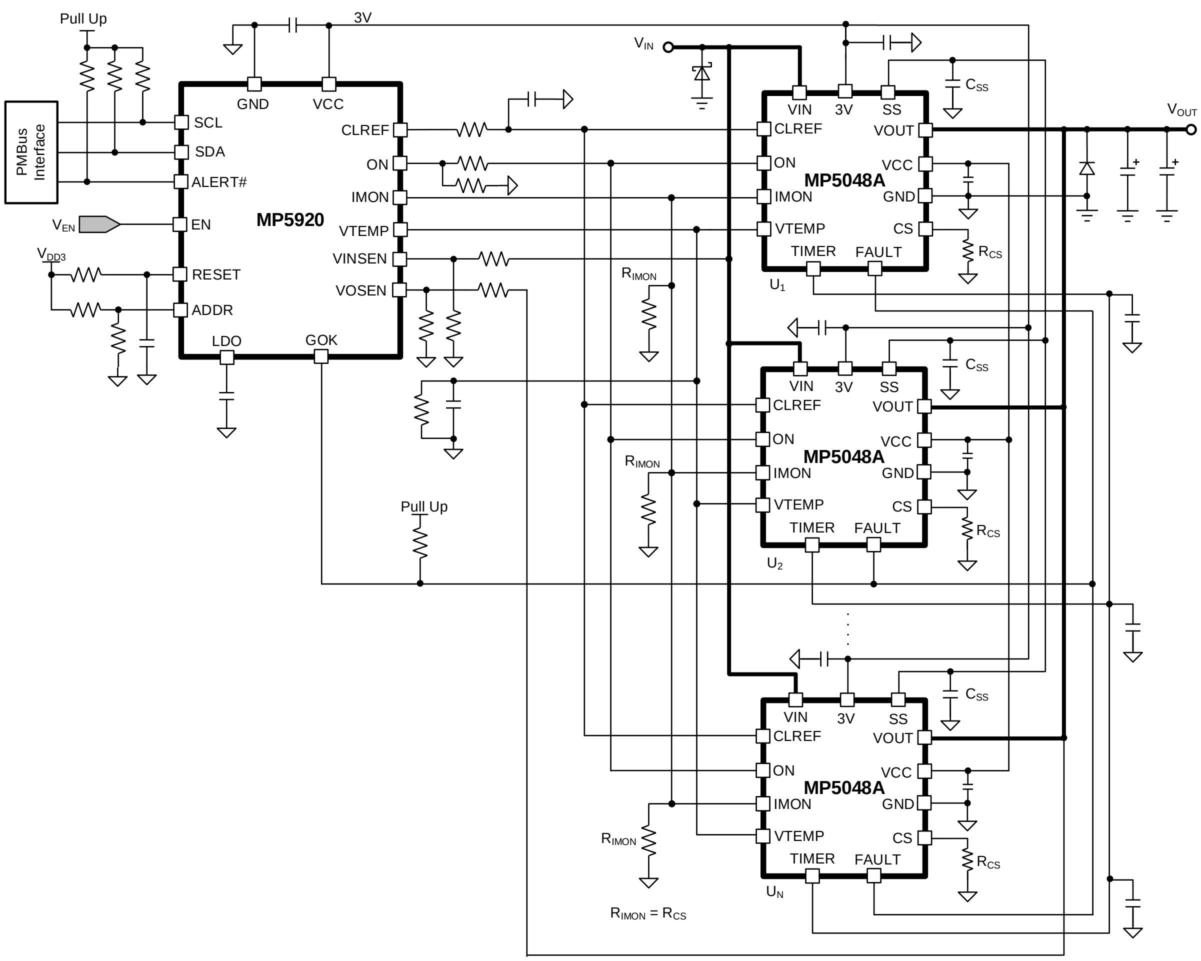


Figure 4: MP5048A Controlled by Hot-Swap Controller (MP5920) in Parallel Operation

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP5048AGU	QFN-30 (5mmx5mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP5048AGU-Z).

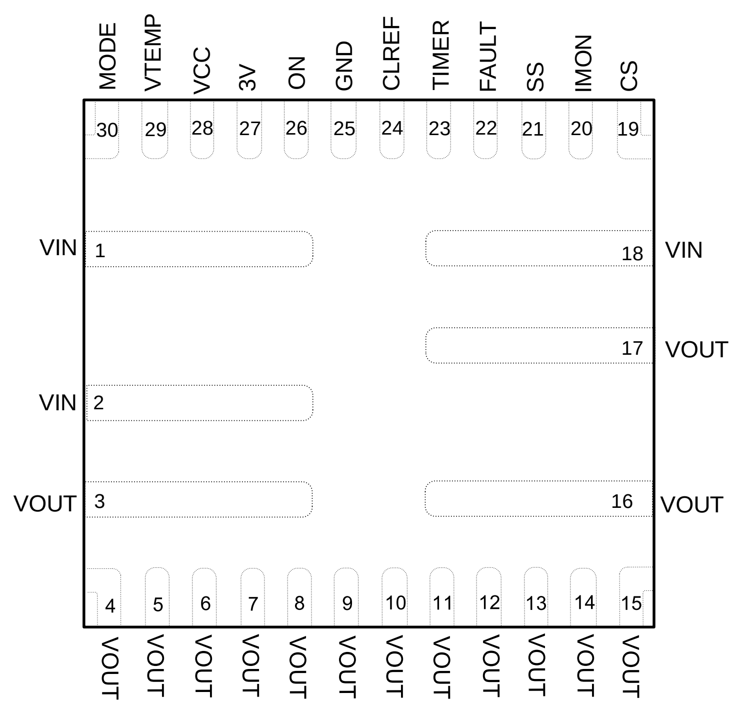
TOP MARKING

MPSYYWW
MP5048A
LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP5048A: Part number
LLLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-30 (5mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 2, 18	VIN	**System input power supply.** The VIN pin is connected to the drain of the integrated power MOSFET.
3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17	VOUT	**Output voltage.** The VOUT pin is connected to the source of the integrated power MOSFET.
19	CS	**Current-sense output.** The CS voltage (V_{CS}) is compared to the CLREF voltage (V_{CLREF}) to determine the over-current (OC) limit. Connect a resistor between the CS and GND pins to generate V_{CS}.
20	IMON	**Current-monitoring output.** The output current (I_{OUT}) is proportional to the current flowing through the powered device. Place a resistor (R_{IMON}) between the IMON and GND pins to set the output gain. Place a 100nF capacitor close to IMON to filter noise.
21	SS	**Soft start.** Place an external capacitor between the SS and GND pins to set the soft-start time (t_{SS}). The internal circuitry controls the slew rate of the output voltage (V_{OUT}) during start-up.
22	FAULT	**Fault indication.** The FAULT pin is an open-drain output. If a fault occurrs, then FAULT is pulled low and latches.
23	TIMER	**Timer setting.** An external capacitor sets the insertion delay time, start-up short-current protection (SCP) delay time, over-current protection (OCP) delay time, and auto-retry delay time.
24	CLREF	**Current-limit reference voltage input.** The CLREF pin sets the reference voltage (V_{CLREF}) for the OCP threshold. Connect a resistor between the CLREF and GND pins, or drive CLREF via an external source to generate V_{CLREF}. Place a 1nF to 10nF capacitor close to CLREF to filter the noise.
25	GND	**Ground.**
26	ON	**Power MOSFET enable control.** Pull the ON pin high to enable the MP5048A; pull ON low to turn it off.
27	3V	**Internal 3V LDO output.** Place a 2.2µF decoupling capacitor close to the 3V and GND pins.
28	VCC	**Internal 4.5V LDO output.** Place a 2.2µF decoupling capacitor close to the VCC and GND pins.
29	VTEMP	**Junction temperature sense output.** The VTEMP pin is the output of the internal temperature sensor.
30	MODE	**Latch or auto-retry mode selection.** If the MODE pin is pulled high, then the part latches off if a fault occurs. Pull MODE up to 5V externally or float MODE to have the part operate in latch mode. Pull MODE low externally to have the part operate in auto-retry mode.

ABSOLUTE MAXIMUM RATINGS [1]

V_{IN} (DC)..-0.3V to +65V
V_{IN} (25ns).. 72V
V_{OUT}.. -0.3V to +65V
All other pins ....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) [2]
……………………………………………5.58W
Junction temperature ....150°C
Lead temperature ....260°C
Storage temperature .... -65°C to +155°C

Recommended Operating Conditions [3]

Input voltage (V_{IN}) ....24V to 60V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance [4]	θ_{JA}	θ_{JC}	
QFN-30 (5mmx5mm)	22.4	9.6	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the device to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 48V, R_{CS} = 2.2kΩ, C_{OUT} = 470µF, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Quiescent current	I_Q	ON is pulled high, no load		2.4	3	mA
		V_{ON} = 0V		1.8	2.4	mA
VCC Regulator and Under-Voltage Lockout (UVLO) Protection						
VCC regulator voltage	V_{CC}		4.45	4.6	4.75	V
VCC load regulation		I_{CC} = 10mA		5		%
VCC UVLO rising threshold	$V_{CC\_UVLO\_RISING}$		3.5	3.65	3.8	V
VCC UVLO hysteresis	$V_{CC\_UVLO\_HYS}$			380		mV
3V regulator voltage	V_{3V}		2.9	3	3.1	V
V_{IN} Under-Voltage Protection (UVP) and Over-Voltage Protection (OVP)						
V_{IN} UVP rising threshold	$V_{IN\_UVP\_RISING}$	V_{CC} = 5V		6.2		V
V_{IN} UVP falling threshold	$V_{IN\_UVP\_FALLING}$	V_{CC} = 5V		5.25		V
V_{IN} OVP fault threshold	V_{IN_OVP}	V_{ON} = 0V		64		V
V_{IN} OVP hysterisis	$V_{IN\_OVP\_HYS}$			2		V
Power MOSFET						
On resistance	$R_{DS(ON)}$	T_J = 25°C		14		mΩ
		T_J = 85°C (5)		18		mΩ
Off state leakage current	I_{OFF}	V_{ON} = 0V			5	µA
Maximum continuous output current (5)	I_{OUT_MAX}				5	A
Thermal Shutdown and Recovery						
Thermal shutdown threshold (5)	T_{SD}			153		°C
Thermal shutdown hysteresis (5)	T_{SD_HYS}	Auto-retry mode only		26		°C
Current-Limit Reference Voltage Input (CLREF)						
Internal current during normal operation	I_{CLREF_NOR}			36		µA
Internal current during soft start (SS)	I_{CLREF_SS}			18		µA
Current-Sense Output (CS)						
Current-sense gain accuarcy	G_{CS_ACCR}	1A ≤ I_{OUT} ≤ 4A	-2.5		+2.5	%
Current-sense gain	G_{CS}			144		µA/A
Soft Start (SS)						
Soft-start pull-up current	I_{SS}	V_{IN} = 48V		11.5		µA
Over-Current Protection (OCP) and Short-Circuit Protection (SCP)						
OCP current limit during normal operation	I_{LIMIT_OCP}	R_{CS} = 2.2kΩ, R_{CLREF} = 27kΩ		3.1		A
OCP response time (5)	t_{OCP_DELAY}	I_{LIMIT_OCP} = 3A		10		µs
Short-circuit protection (SCP) current limit (5)	I_{LIMIT_SCP}	Regardless of R_{CS}		6.85		A
SCP response time (5)	t_{SC}			200		ns

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 48V, R_{ISET} = 2.2kΩ, C_{OUT} = 470µF, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Output Current Monitoring						
I_{MON} / I_{OUT} gain	G_{IMON}			144		µA/A
I_{MON} / I_{OUT} gain accuracy	G_{IMON_ACCR}	1A ⩽ I_{OUT} ⩽ 4A	-1.5		+1.5	%
Maximum IMON pin voltage (5)	V_{IMON}				2	V
MOSFET Short Detection						
MOSFET drain-to-source short fault flag	V_{OUT_DSTH}			0.9 x V_{IN}		V
Fault release high flag while removing drain-to-source short	V_{OUT_FAULTH}			0.7 x V_{IN}		V
MOSFET gate-to-source short detection time	t_{GS_SHRT}			270		ms
Maximum soft-start time	t_{SS_MAX}			270		ms
Power MOSFET Enable Control (ON)						
Rising threshold	V_{ON_VTH}		1.13	1.23	1.31	V
Hysteresis	V_{ON_HYS}			450		mV
Mode Selection (MODE)						
MODE rising voltage threshold	V_{MODE_RISING}		1	1.2	1.4	V
MODE hysteresis	V_{MODE_HYS}			450		mV
MODE pull-up current	I_{MODE_PU}			4		µA
Fault						
Output low voltage	V_{OL_FAULT}	1mA sink current			0.2	V
Fault off-state leakage current	I_{FAULT_LKG}	V_{FAULT} = 5V			5	µA

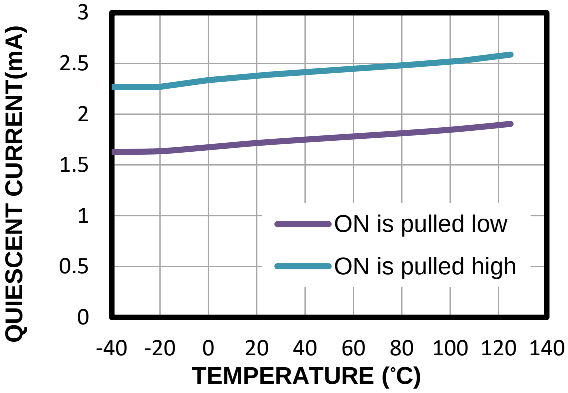
Note:

5) Guaranteed by design.

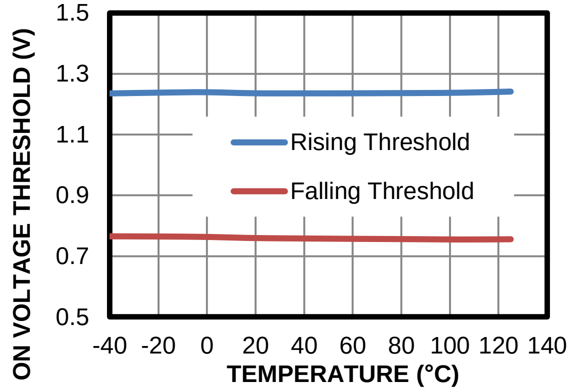
TYPICAL CHARACTERISTICS

V_{IN} = 48V, C_{OUT} = 330µF, R_{CS} = R_{IMON} = 2.2kΩ, C_{TIMER} = 10nF, T_J = 25°C, unless otherwise noted.

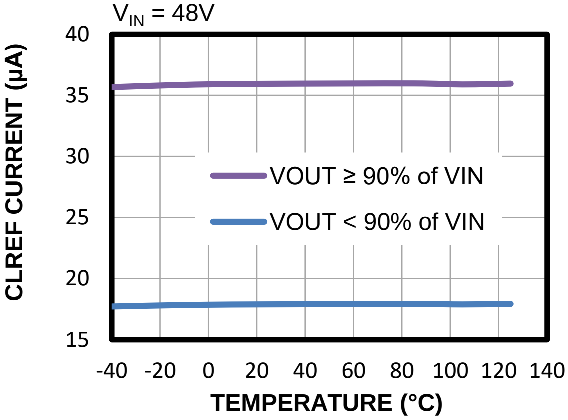
Quiescent Current vs. Temperature
V_{IN} = 48V



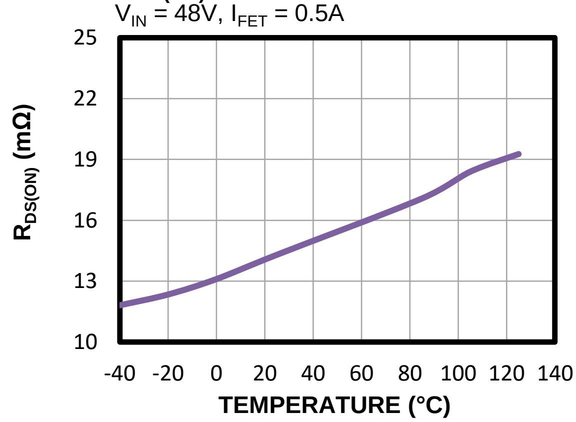
ON Voltage Threshold vs. Temperature
V_{IN} = 48V, no load



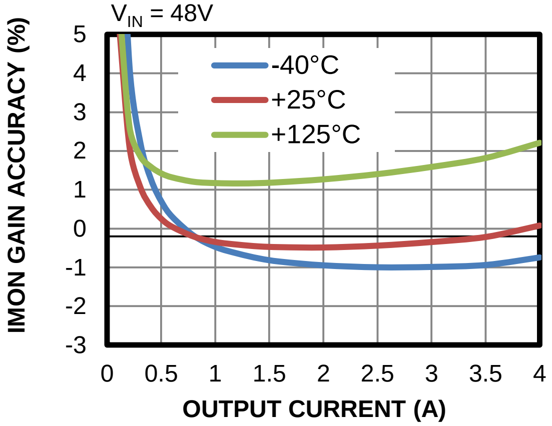
CLREF Current vs. Temperature
V_{IN} = 48V



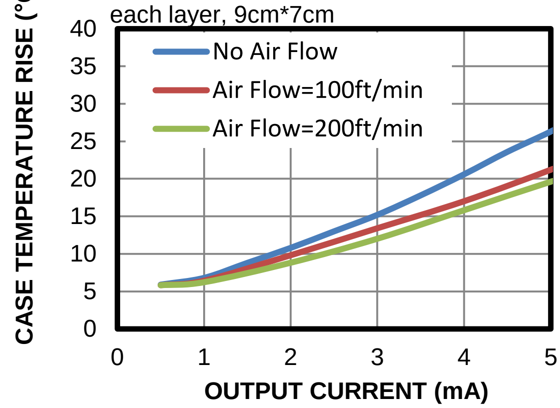
$R_{DS(ON)}$ vs. Temperature
V_{IN} = 48V, I_{FET} = 0.5A



IMON Gain Accuracy
V_{IN} = 48V



Case Temperature Rise vs. Output Current
EV5048A-V-1PHASE-00A, 4-Layers, 2Oz each layer, 9cm*7cm

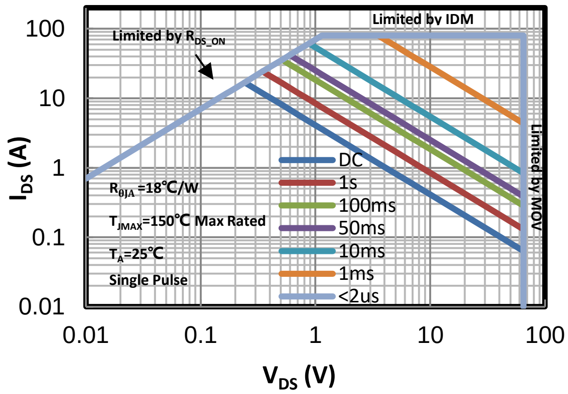


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 48V, C_{OUT} = 330μF, R_{CS} = R_{IMON} = 2.2kΩ, C_{TIMER} = 10nF, T_J = 25°C, unless otherwise noted.

Safe Operating Area (SOA)

Tested on the EV5048A-V-1PHASE-00A (9cmx7cm), 4-layer PCB, 2oz per layer

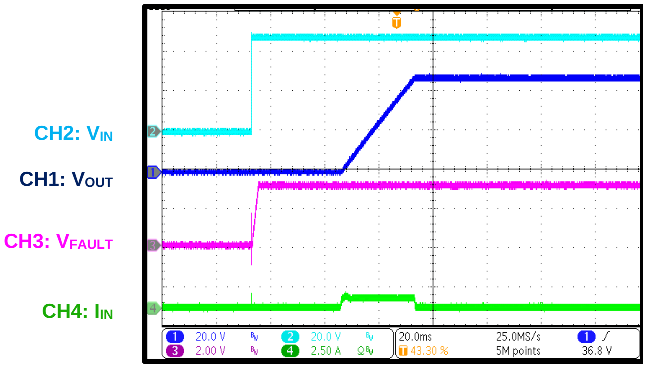


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 48V, C_{OUT} = 330µF, R_{CS} = R_{IMON} = 2.2kΩ, C_{TIMER} = 10nF, T_J = 25°C, unless otherwise noted.

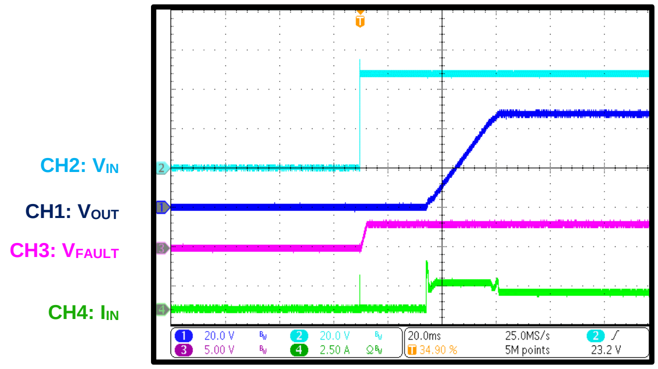
V_{IN} Hot Swap

I_{OUT} = 0A



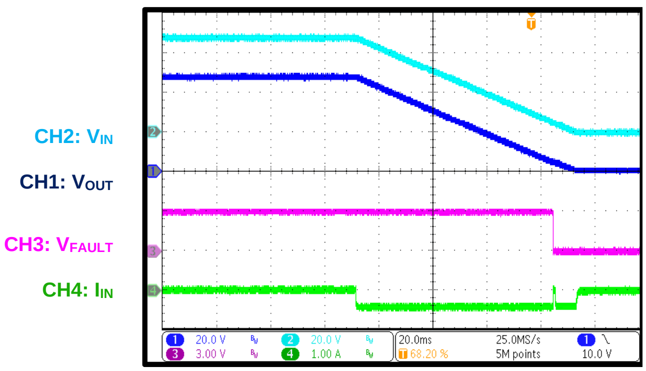
V_{IN} Hot Swap

I_{OUT} = 1A



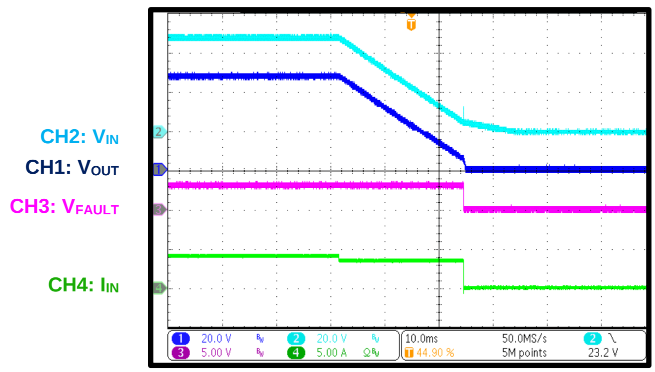
Shutdown through VIN

I_{OUT} = 0A



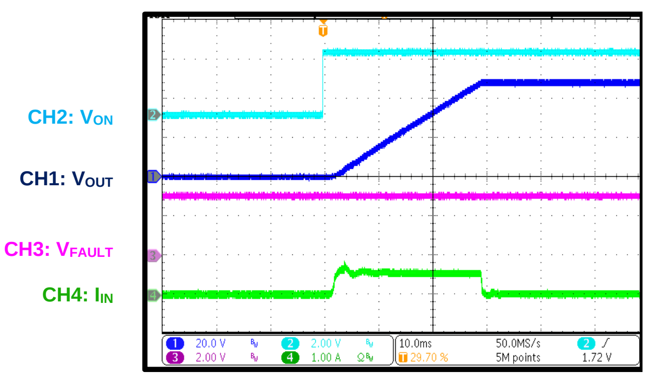
Shutdown through VIN

I_{OUT} = 4A



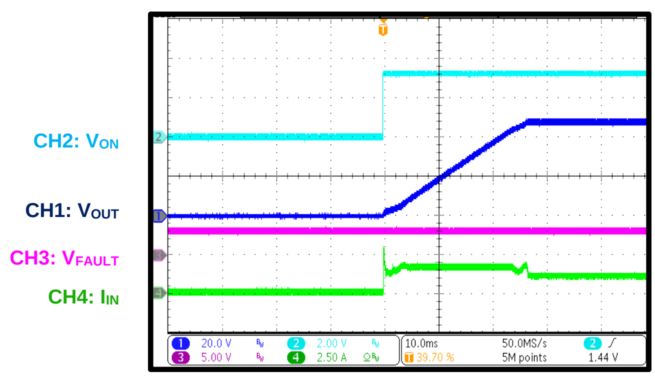
Start-Up through ON

I_{OUT} = 0A



Start-Up through ON

I_{OUT} = 1A

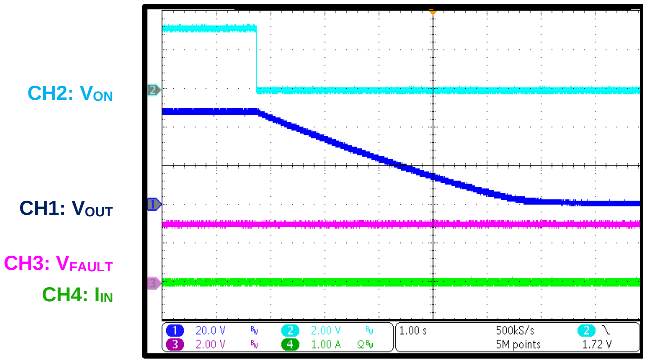


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, C_{OUT} = 330µF, R_{CS} = R_{IMON} = 2.2kΩ, C_{TIMER} = 10nF, T_J = 25°C, unless otherwise noted.

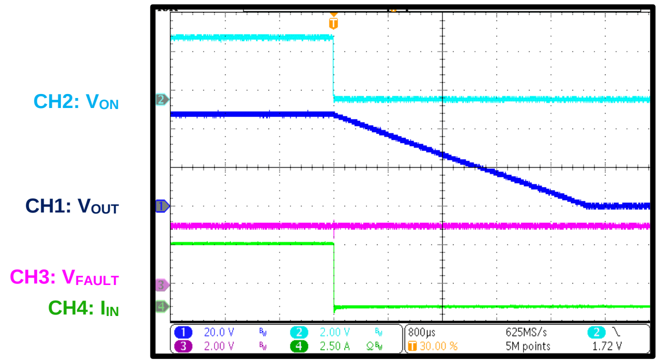
Shutdown through ON

I_{OUT} = 0A



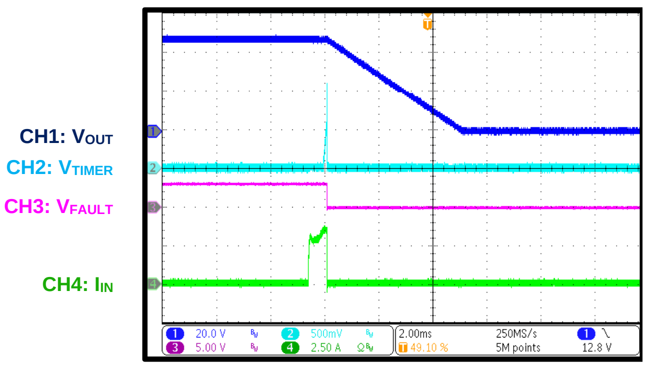
Shutdown through ON

I_{OUT} = 4A



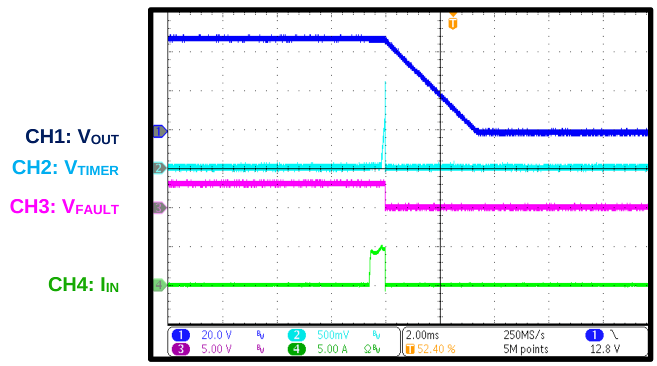
OCP Entry

I_{LIMIT_OCP} = 3A, latch mode



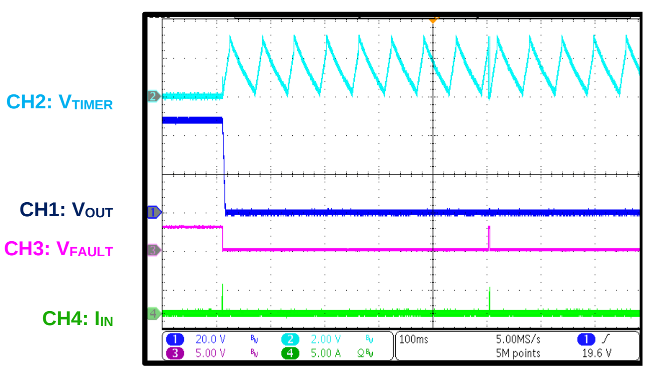
OCP Entry

I_{LIMIT_OCP} = 4.5A, latch mode



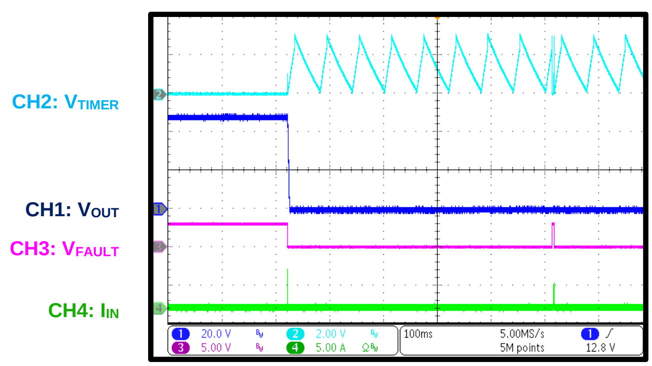
OCP Entry

I_{LIMIT_OCP} = 3A, auto-retry mode



OCP Entry

I_{LIMIT_OCP} = 4.5A, auto-retry mode

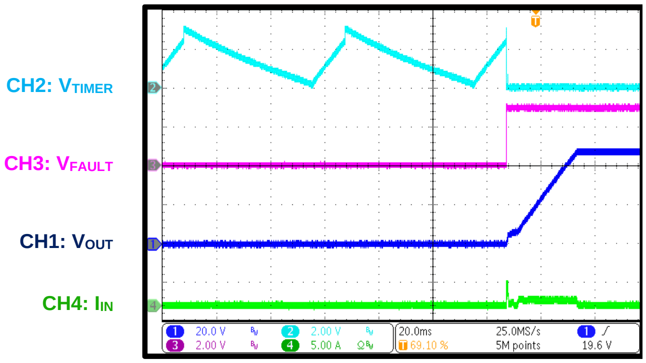


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, C_{OUT} = 330µF, R_{CS} = R_{IMON} = 2.2kΩ, C_{TIMER} = 10nF, T_J = 25°C, unless otherwise noted.

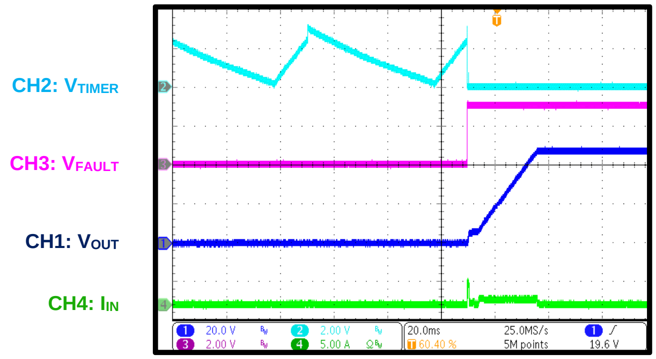
OCP Recovery

I_{LIMIT_OCP} = 3A, auto-retry mode



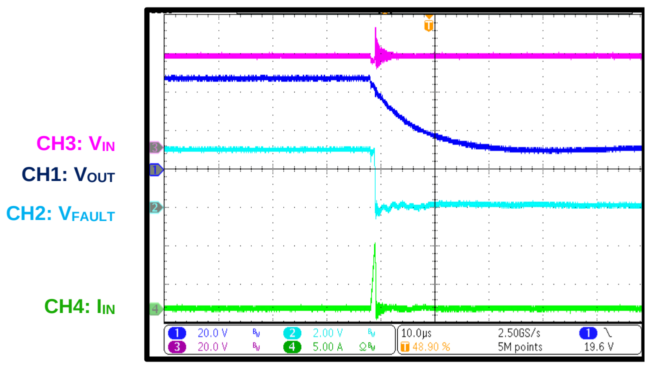
OCP Recovery

I_{LIMIT_OCP} = 4.5A, auto-retry mode



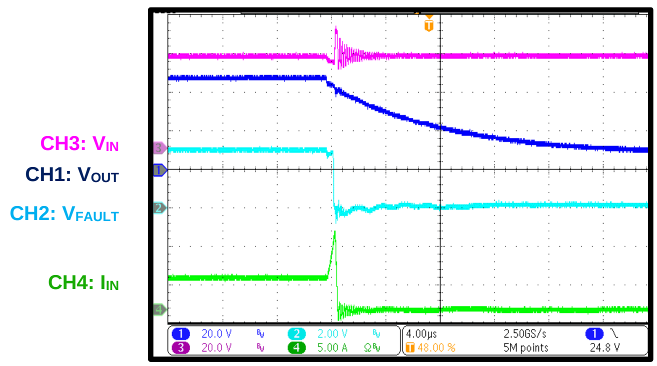
SCP Entry

Latch mode



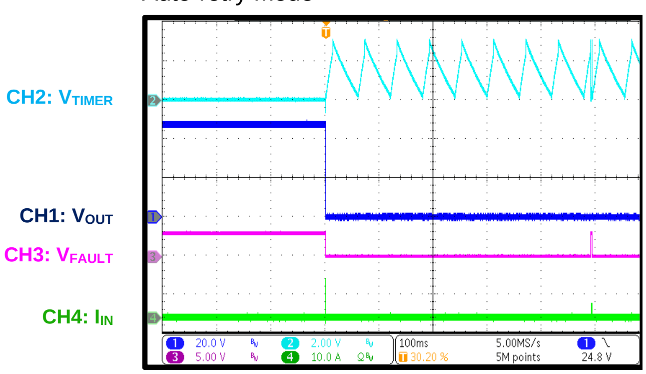
SCP Entry

I_{OUT} = 4A, then short V_{OUT} to GND, latch mode



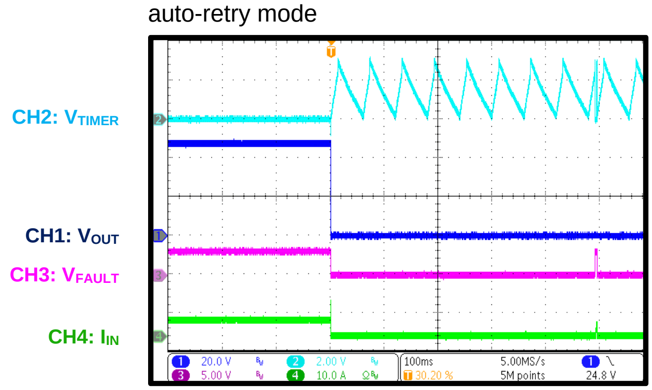
SCP Entry

Auto-retry mode



SCP Entry

I_{OUT} = 4A, then short V_{OUT} to GND, auto-retry mode

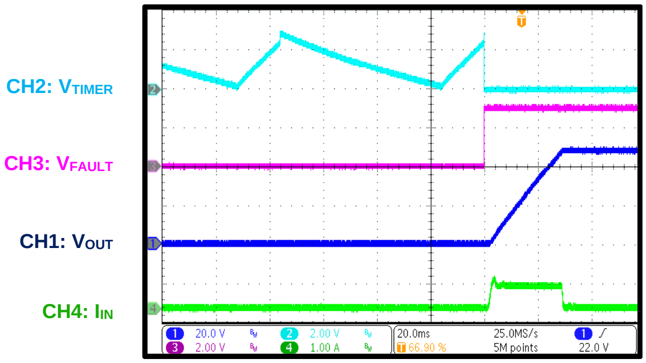


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, C_{OUT} = 330µF, R_{CS} = R_{IMON} = 2.2kΩ, C_{TIMER} = 10nF, T_J = 25°C, unless otherwise noted.

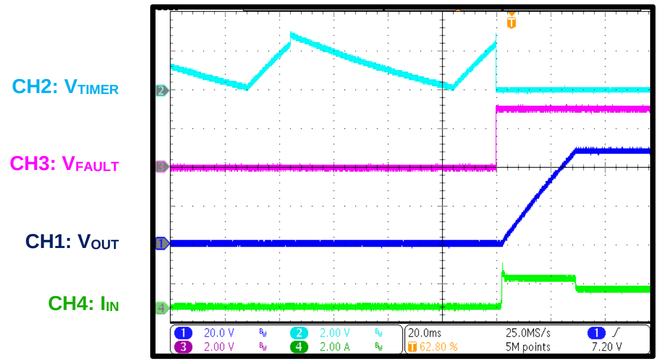
SCP Recovery

Auto-retry mode



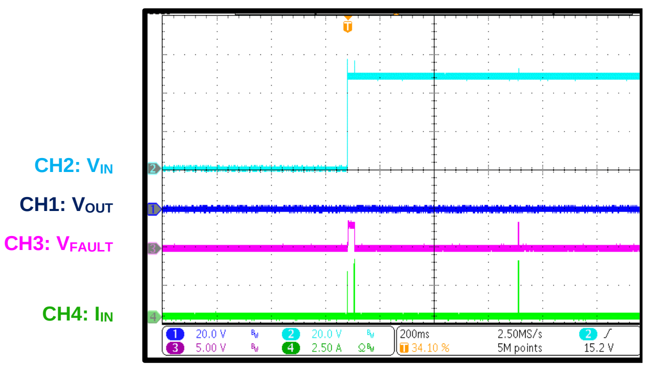
SCP Recovery

I_{OUT} = 0.9A, auto-retry mode



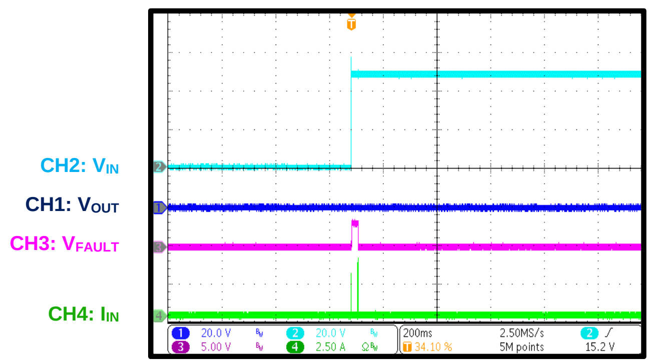
SCP Start-Up through VIN

Auto-retry mode



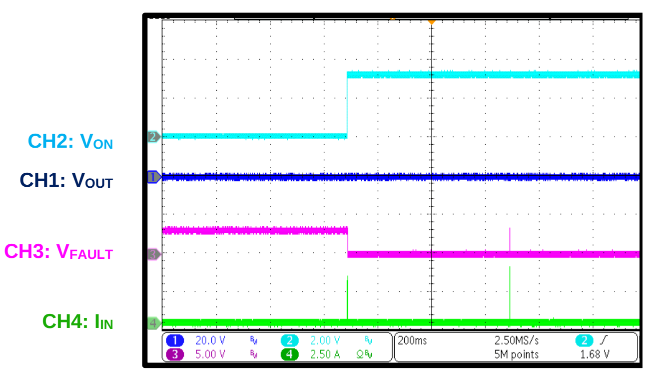
SCP Start-Up through VIN

Latch mode



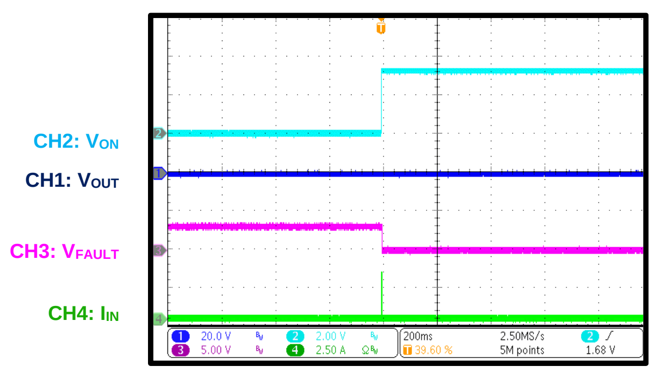
SCP Start-Up through ON

Auto-retry mode



SCP Start-Up through ON

Latch mode

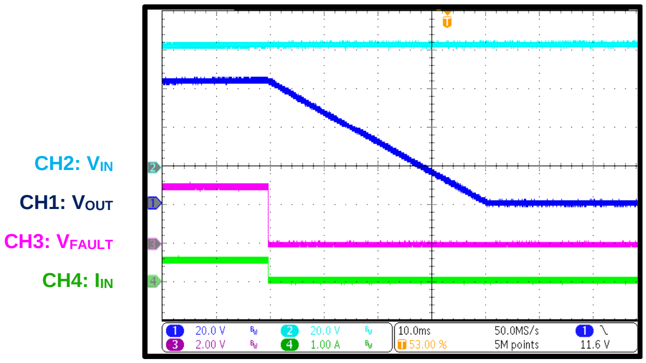


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, C_{OUT} = 330µF, R_{CS} = R_{IMON} = 2.2kΩ, C_{TIMER} = 10nF, T_J = 25°C, unless otherwise noted.

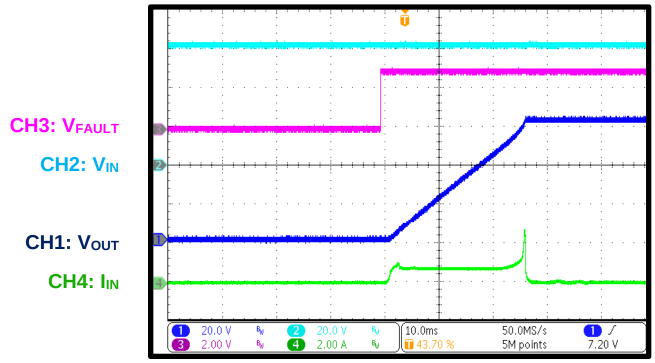
V_{IN} OVP Shutdown

I_{OUT} = 0.5A, apply 64V to the VIN pin



V_{IN} OVP Recovery

Auto-retry mode, OVP has been triggered, then V_{IN} is reduced



FUNCTIONAL BLOCK DIAGRAM

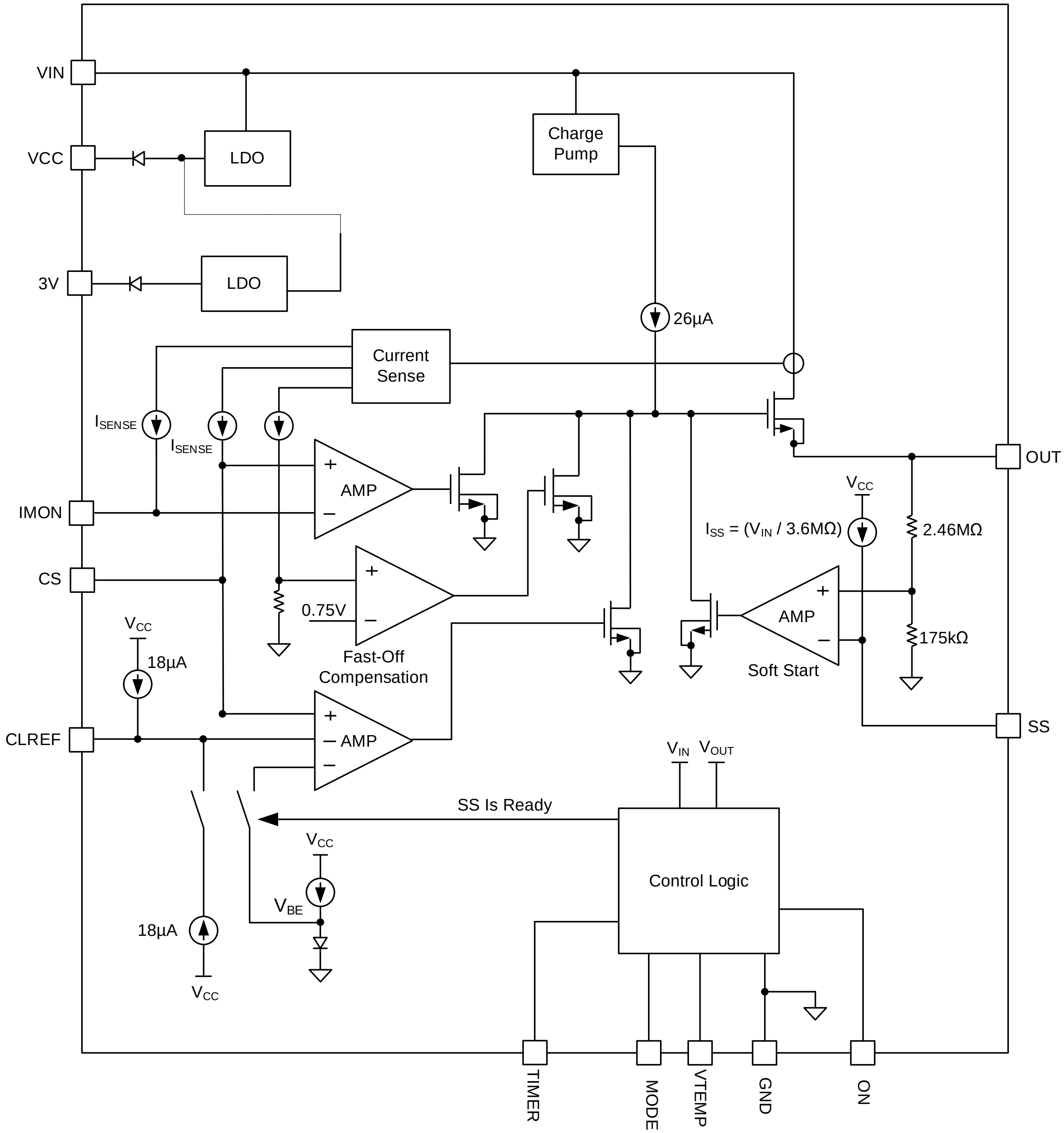


Figure 5: Functional Block Diagram

OPERATION

The MP5048A is a monolithic, integrated controller and switch. It has a power MOSFET with a 14mΩ on resistance ($R_{DS(ON)}$), which makes it ideal for multi-fuse hot-swap or e-fuse applications. The MP5048A as a standalone device, or it can be sequenced with the hot-swap controller (e.g. the MP5920 or MP5922). Multiple MP5048A devices can be used in parallel to support all power levels required by the system. All devices operating in parallel actively share current during soft start (SS). This distributes the load current (I_{LOAD}) evenly during SS. The MP5048A supports 4A of continuous output current (I_{OUT}) per device at room temperature.

The MP5048A provides a controlled start-up voltage, and limits the inrush current when a circuit card is inserted into an active power source. The MP5048A provides support for e-fuse and hot-swap applications. It integrates a power MOSFET, temperature sensing, current monitoring, current protection, temperature protection, and power sequencing into a single device. The MP5048A monitors the current flowing through the device, as well as the die temperature, eliminating the need for an external sense resistor and thermal sensing.

Start-Up Sequence

The MP5048A has two operation modes. It can be controlled by a hot-swap controller, or can act as a standalone device.

If the MP5048A is controlled by a hot-swap controller, then the power MOSFET remains off until the ON pin is pulled high.

A capacitor on the timer pin (C_{TIMER}) sets the insertion delay time, start-up short-circuit protection (SCP) delay time, over-current protection (OCP) delay time, and auto-retry delay time. The insertion delay time starts once V_{IN} exceeds the under-voltage lockout (UVLO) threshold. Once the ON pin is pulled high and the insertion delay time is finished, the power MOSFET is charged up via the internal charge pump. Once the power MOSFET's voltage (V_{GS}) reaches its threshold (V_{GSTH}), the output voltage (V_{OUT}) rises (see Figure 6).

V_{OUT} rises according to the the soft-start slew rate. The rise time is determined by the soft-start capacitor (C_{SS}).

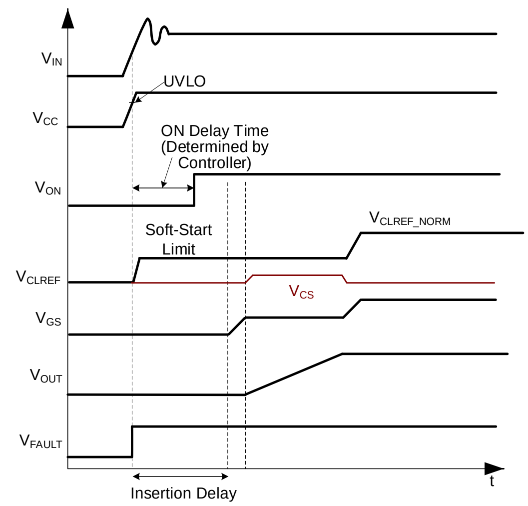


Figure 6: Start-Up while the MP5048A Is Controlled by Hot-Swap Controller

During SS, the current limit (I_{LIMIT}) is reduced via the internal soft-start limit (V_{SS_LIMIT}). Once SS is complete, I_{LIMIT} increases to the full-scale I_{LIMIT} set by the CLREF resistor (R_{CLREF}).

The ON pin is low by default since it is pulled to GND internally via a 1.1MΩ resistor. If the MP5048A is operating in standalone mode, the ON pin should be pulled up externally to the VCC voltage (V_{CC}) (see Figure 7).

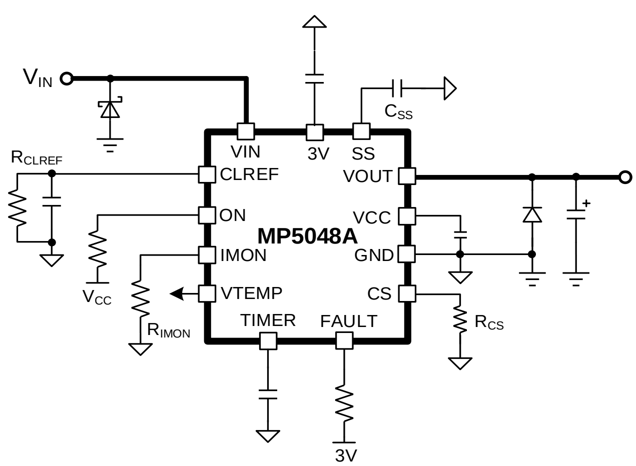


Figure 7: Standalone Operation

If the ON voltage (V_{ON}) exceeds its rising threshold while the insertion delay time finishes, the power MOSFET is charged up via the internal current source (26μA). The power MOSFET turns on once V_{GS} reaches V_{GSTH}, and V_{OUT} rises (see Figure 8 on page 18).

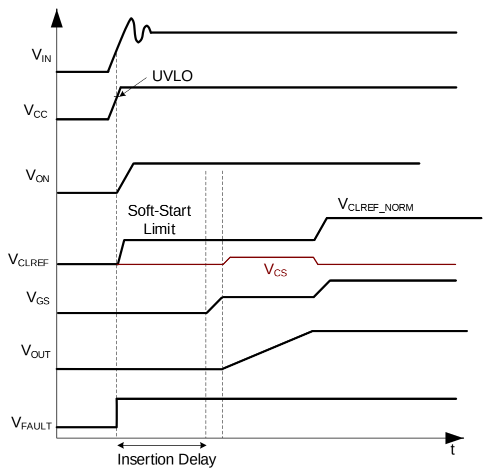


Figure 8: Start-Up during Standalone Opeation

Soft Start (SS)

The soft-start capacitor (C_{SS}) determines the soft-start time (t_{SS}). Once the ON pin is pulled high and the insertion delay time finishes, a constant-current source proportional to the input voltage (V_{IN}) charges the soft-start voltage (V_{SS}). V_{OUT} rises at a similar slew rate to V_{SS}.

C_{SS} can be calculated with Equation (1):

$$C_{SS}(nF) = \frac{15 \times t_{SS}(mS)}{R_{SS}} \quad (1)$$

Where R_{SS} is the soft-start resistor (3.6MΩ).

For example, a 100nF capacitor provides a t_{SS} of 24ms. If the load capacitance is extremely large, then the current required to maintain the preset t_{SS} exceeds the start-up I_{LIMIT}. In this case, the rise time is controlled by the load capacitor (C_{LOAD}) and the start-up I_{LIMIT}. Float the SS pin to generate a fast slew rate.

A current source (26μA) pulls up the power MOSFET gate. The gate charge current controls the V_{OUT} rise time. The minimum t_{SS} is 1.5ms.

If the MP5048A is used in multi-phase application, all of the SS pins should be connected together. This ensures that all of the devices have the same t_{SS}.

If a fault occurs, then the FAULT and SS pins are pulled low. If the MP5048A is set to auto-retry mode, then the SS pin is held low until the auto-retry delay time has expired. Once the auto-retry delay time finishes, the MP5048A turns on the MOSFET, and initiates an SS to resume normal operation.

TIMER Pin

The TIMER pin has four functions, listed below:

1. Sets the insertion delay time
2. Sets the SCP start-up delay timer
3. Sets the OCP delay time
4. Sets the auto-retry delay time

Insertion Delay Time

Once the MP5048A's completes the internal power-on reset (POR), then the insertion delay begins by charging the capacitor with a 2μA current source. If the voltage reaches its threshold, then the TIMER pin is pulled up via an internal 4V source for 3.5μs. Then it is pulled to GND for 7.5μs. The timer repeats this, and then the insertion delay time is completed (see Figure 9).

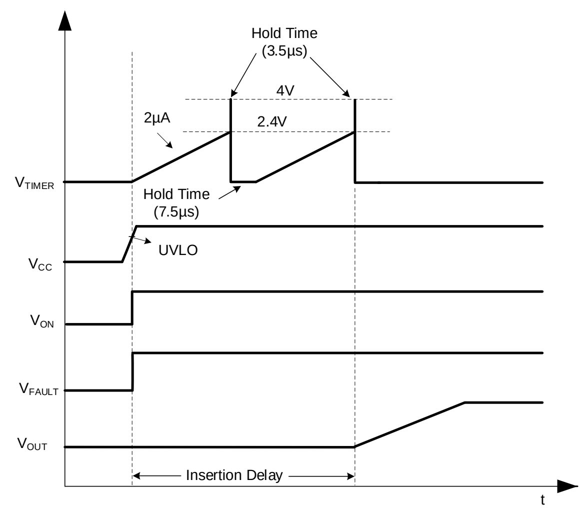


Figure 9: MP5048A Insertion Delay Time

The pull-up voltage is determined by the external TIMER capacitor (C_{TIMER}).

Start-Up SCP Delay Time

If V_{OUT} is below 20% of V_{IN} during start-up, and V_{GS} is regulated by V_{SS_LIMIT}, then the SCP start-up delay timer starts. Once the SCP start-up delay timer is complete, then the power MOSFET turns off and the FAULT pin is pulled low (see Figure 10 on page 19).

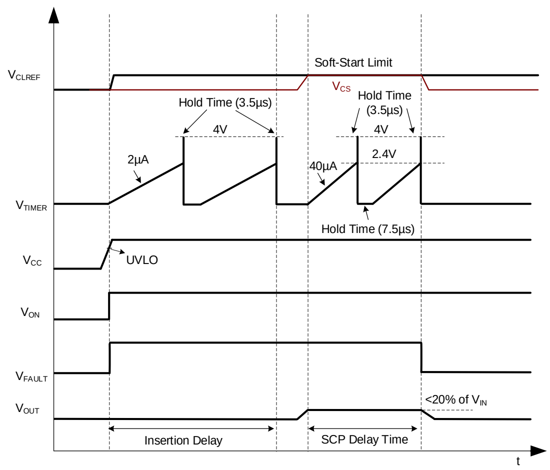


Figure 10: SCP Delay Time

If no fault occurs, then the MP5048A follows the normal start-up sequence, and V_{OUT} rises according to the V_{SS}.

OCP Delay Time

An over-current (OC) fault occurs if the current flowing through the MP5048A exceeds the configured threshold, and is held for the duration of the OCP delay time.

If V_{CS} exceeds the CLREF voltage (V_{CLREF}), then a 40μA current source charges C_{TIMER}. If the TIMER voltage (VTIMER) exceeds the trip threshold (0.6V), then the power MOSFET turns off and the FAULT pin is pulled low to indicate an OC fault has occurred (see Figure 11).

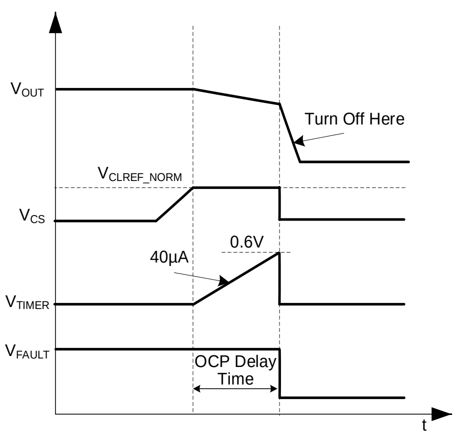


Figure 11: OCP Delay Time

The OCP delay time can be adjusted so that the the system can endure a current transient without forcing a shutdown. A current transient can cause a current that exceeds the OCP threshold for a small amount of time. Adjusting the timer can accommodate this brief OC fault.

Auto-Retry Delay Time

The FAULT pin is pulled low to indicate a fault has occurred. If the MODE pin is configured for auto-retry mode, then the MP5048A charges and discharges the TIMER pin nine times using the same rates as the insertion delay. After the ninth cycle, the MP5048A automatically retries a start-up sequence (see Figure 12).

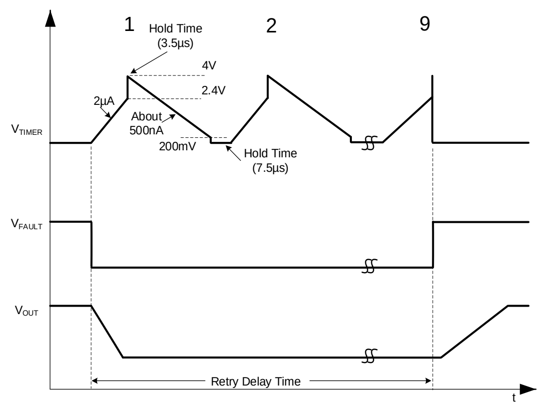


Figure 12: Auto-Retry

Over-Current Protection (OCP)

I_{LOAD} is limited by the current-limit reference input and the external current-sense resistor (R_{CS}). The CS voltage (V_{CS}) is compared to the I_{LIMIT} reference via an amplifier to regulate the power MOSFET's gate voltage (V_{GATE}). This prevents the Intelli-Fuse current from exceeding the I_{LIMIT} defined by the reference.

The current-limit reference voltage (V_{REF}) is set via CLREF, which is clamped low internally during SS to set a low I_{LIMIT}. Once V_{OUT} reaches V_{IN}, the I_{LIMIT} reference can be increased to the full I_{LIMIT} set by V_{CLREF}. At this point, the power MOSFET gate is fully enhanced, and the e-fuse is ready to deliver full power from the input.

Current Limit at Start-Up

To protect the MP5048A from overheating during start-up, the internal maximum current-limit clamp voltage and CS limit reference configuration current are determined by V_{IN} and V_{OUT} (see Figure 13 on page 20).

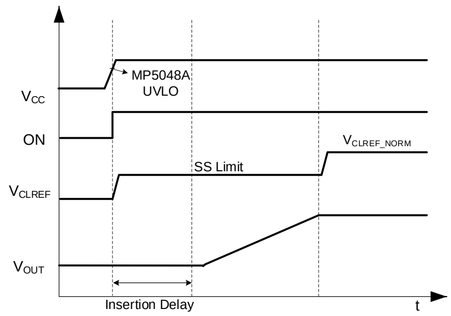


Figure 13: MP5048A SS Current Limit

If V_{OUT} is below 90% of V_{IN}, then the maximum current-limit reference is clamped to the CLREF clamp voltage (V_{CLREF_CLAMP}) (660mV with a negative temperature coefficient), and the thermal shutdown threshold is 153°C.

The CS current-limit reference configuration current is 18μA if V_{OUT} is below 90% of V_{IN}, and V_{CLREF} is determined by the external CLREF resistor (R_{CLREF}). If V_{CLREF} is below V_{CLREF_CLAMP}, then the actual current-limit V_{REF} is determined by the external V_{CLREF}. Otherwise, V_{REF} is determined by V_{CLREF_CLAMP}.

If V_{OUT} ⩾90% of V_{IN}, then V_{CLREF_CLAMP} (660mV) is disabled. The CS current-limit reference configuration current is between 18μA and 36μA(18μA + 18μA), and CS is limited by the CLREF's externally configured value (typically limited to 2V).

If the power MOSFET remains on while V_{OUT} is below 90% of V_{IN} within the maximum t_{SS} (t_{SS_MAX}), then the power MOSFET shuts down once the t_{SS_MAX} (270ms) finishes. If I_{LOAD} is high (but lower than V_{SS_LIMIT}), then the power MOSFET start-up instantaneous loss is large. Thermal shutdown is triggered before t_{SS} is complete, and FAULT is pulled low (see Figure 14).

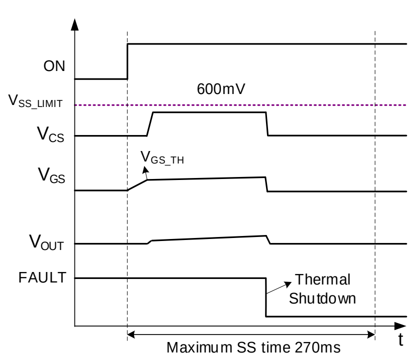


Figure 14: Failed Start-Up within 270ms

If V_{OUT} is below 20% of V_{IN} during start-up, and V_{GS} is regulated by V_{SS_LIMIT} for the start-up SCP delay time, then the power MOSFET latches off, and FAULT is pulled low.

Current Limit during Normal Operation

Once the MP5048A detects that start-up is compelte, the part enters normal operation.

Once V_{CS} (configured by an external resistor) exceeds the normal CLREF threshold during normal operation, the internal circuit regulates V_{GATE} to keep the power MOSFET constant. To limit the current, the gate-to-source voltage (V_{GS}) should be regulated between 5V and V_{TH}. The typical response time is about 10s. I_{OUT} may have a small overshoot during this period.

If I_{LIMIT} is reached, then the internal fault timer starts. If I_{OUT} drops below the I_{LIMIT} threshold before the end of OCP delay time, then the MP5048A resumes normal operation. If I_{OUT} exceeds I_{LIMIT} for longer than the delay time, then the power MOSFET latches off and the FAULT pin is pulled low.

The desired I_{LIMIT} during normal operation is a function of the CS pin's external resistor (R_{CS}).

The MP5048A I_{LIMIT} value can exceed the normal maximum load current (I_{LOAD}) to allow for tolerances in the current-sense value. I_{LIMIT} can be estimated with Equation (2):

$$I_{LIMIT} = \frac{V_{CLREF\_NORM}}{G_{CS} \times R_{CS}} \tag{2}$$

Where V_{CLREF_NORM} is the CLREF voltage during normal operation, and G_{CS} is the current-sense gain once the power MOSFET is fully on (typically 144μA/A). The OCP limit should not exceed 4.8A.

The MOSFET works in the linear region.

Short-Circuit Protection (SCP)

If I_{LOAD} increases rapidly due to a short circuit, then the current may exceed the I_{LIMIT} threshold before the hot-swap control loop can respond. If the Intelli-Fuse current reaches 6.85A, then a fast turn-off circuit in the Intelli-Fuse is activated to turn the power MOSFET off. The total SCP response time is about 200ns. The FAULT signal is pulled low once the power MOSFET's current reaches the I_{LIMIT} (6.85A).

If the device is in latch mode, then there is not a retry response after short-circuit detection. The FAULT pin remains low and the device remains off. To clear the fault, pull the ON pin low and then high. This clears the fault condition, and the MP5048A initiates a new SS. If the short circuit is still present, the device repeats this process. Once the short circuit is removed, the MP5048A ramps up V_{OUT} according to V_{SS}.

If the device is in auto-retry mode, then the retry timer counts nine cycles on the TIMER pin (see Figure 12 on page 19). At the end of the retry timer count, the MP5048A attempts to start up again. If the short is still present, the process continues at the rate of the retry timer for the auto-retry process. If the short has been removed, then the MP5048A ramps up V_{OUT} according to V_{SS}.

FAULT Report

FAULT is an open-drain, active-low signal to report fault conditions. FAULT monitors the following faults in the Intelli-Fuse:

1. Over-current (OC) fault: If the CS voltage exceeds V_{CS} the CLREF threshold during normal operation, then FAULT is pulled low after a configured gate regulation time.
2. Short circuit: If the Intelli-Fuse's I_{LOAD} reaches 6.85A quickly, then FAULT is pulled low.
3. Intelli-Fuse's power MOSFET drain-to-source, gate-to-drain, or gate-to-source short detection: See the Damaged Intelli-Fuse MOSFET Detection section for more details.
4. Over-temperature (OT) fault: If an OT fault is detected (T_J > 153°C), FAULT is pulled low.

If a fault latch occurs, then FAULT is pulled low. The latch can be released by cycling the power on VIN or ON.

Damaged Intelli-Fuse MOSFET Detection

Damaged Intelli-Fuse power MOSFET detection includes MOSFET drain-to-source, gate-to-drain, and gate-to-source short detection. These conditions are described below.

Drain-to-Source Short Detection during Start-Up

Once V_{CC} on the Intelli-Fuse exceeds its under-voltage lockout (UVLO) rising threshold, and V_{ON} exceeds its rising threshold, then the Intelli-Fuse detects the drain-to-source short after the insertion delay ends. In this instance, the Intelli-Fuse treats any V_{OUT} above 90% of V_{IN} during start-up as a short on the MOSFET. FAULT remains low while the Intelli-Fuse detects that V_{OUT} has exceeded 90% of V_{IN} during start up. Once the short is removed and the Intelli-Fuse detects that V_{OUT} has dropped below 70% of V_{IN}, FAULT is pulled high, and the MP5048A starts up and resumes normal operation.

Gate-to-Drain Short Detection during Start-Up

During start-up, the Intelli-Fuse detects a power MOSFET gate-to-drain short by monitoring its drain-to-gate voltage (V_{DG}) and V_{GS}. If V_{GS} exceeds a fault threshold voltage, or if V_{DG} drops below the fault threshold, then FAULT is pulled low until the short is removed.

Gate-to-Source Short Detection during Start-Up

FAULT is pulled low for gate-to-source short detection during the MOSFET turn-on period (if V_{OUT} is below 90% of V_{IN} after the maximum internal 270ms soft-start time). To turn the Intelli-Fuse on again, remove the short and cycle the power on VIN or ON.

Gate-to-Source or Gate-to-Drain Short Detection during Normal Operation

If V_{OUT} exceeds 90% of V_{IN} while the part is operating normally, then the Intelli-Fuse detects the power MOSFET gate-to-to-source or gate-drain short by checking if the difference between the internal charge pump voltage (V_{CP}) and V_{GATE} is below 2V after 270ms (if no other fault has occurred). If this occurs, then FAULT is pulled low. To turn the Intelli-Fuse on again, remove the short and cycle the power on VIN or ON.

FAULT Reset

To restart the part after a fault has occurred, pull the ON pin low and then high. Once the fault is removed, the MP5048A begins the start-up sequence.

V_{IN} Over-Voltage Protection (OVP)

V_{IN} over-voltage protection (OVP) has a fixed limit of 64V. If this level is reached, then the power MOSFET turns off. If the device is set to latch mode, then the fault can be released by cycling the power on VIN or ON. If the device is set to auto-retry mode, then the power MOSFET does not turn on until V_{IN} drops below 62V.

Under-Voltage Lockout (UVLO) Protection

The UVLO threshold can be configured via a resistor divider connected between the input and the ON pin. The network can be adjusted by setting the start-up voltage via the VIN pin.

Current-Sense Output (CS)

The CS pin provides a current proportional to I_{OUT} (the current through the powered device). The current-sense gain is 144µA/A once the power MOSFET is fully on. There is a resistor (R_{CS}) connected to CS that forms an external voltage. The CS current (I_{CS}) can be estimated with Equation (3):

$$I_{CS} = I_{OUT} \times 144\mu A/A \quad (3)$$

The CS reference voltage (V_{CS}) can be calculated with Equation (4):

$$V_{CS} = I_{CS} \times R_{CS} \quad (4)$$

If V_{CS} reaches the CLREF I_{LIMIT} threshold, then the internal circuit regulates V_{GATE} to keep the current in the power MOSFET constant.

Current-Monitoring Output (IMON)

The current monitor gain is 144µA/A. There is a resistor (R_{IMON}) connected between the IMON and GND pins. The IMON voltage (V_{IMON}) should be between 0V and 2V to keep IMON's current (I_{IMON}) linearly proportional to I_{OUT}. I_{IMON} can be calculated with Equation (5):

$$I_{IMON} = I_{OUT} \times 144\mu A/A \quad (5)$$

The IMON reference voltage (V_{IMON}) can be estimated with Equation (6):

$$V_{IMON} = I_{MON} \times R_{IMON} \quad (6)$$

The MP5048A current-monitoring output can be used by the controller to accurately monitor the I_{OUT}. Place a 100nF capacitor between the IMON and GND pins to smooth the indicator voltage.

Temperature-Sense Output (VTEMP)

The VTEMP pin reports the junction temperature (T_J) when there is no thermal gradient on the IC. If V_{CC} exceeds its UVLO threshold and the MP5048A is in active mode, then VTEMP has a voltage output proportional to T_J. The VTEMP voltage (V_{TEMP}) is 11.8mV/°C, which can be calculated with Equation (7):

$$V_{TEMP} = (T_J \times 11.8 + 100)mV \quad (7)$$

For example, if T_J is 100°C, then V_{TEMP} is about 1.3V. If V_{TEMP} is 0V, then T_J is about -8°C. The total temperature-sense range is between -8°C and +150°C. If T_J drops below -8°C, then V_{TEMP} remains at 0V.

In multi-fuse operation, the VTEMP pins of each Intelli-Fuse can be connected to the temperature monitor pin of the controller (see Figure 15).

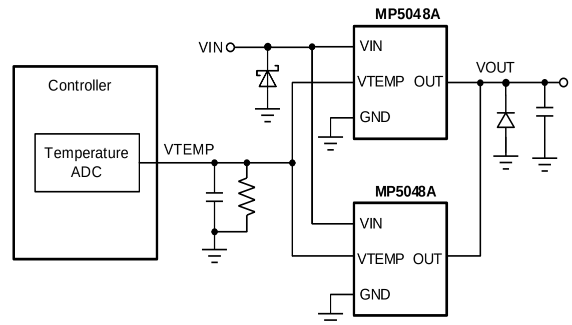


Figure 15: Multi-Fuse Temperature-Sense Utilization during Parallel Operation

Current Balancing during Parallel Operation

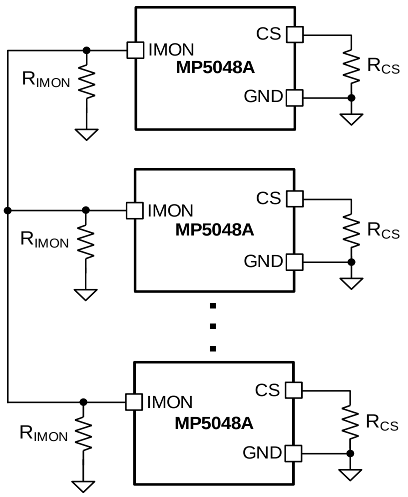
Multiple MP5048A devices can be used in parallel for high-current applications. The current balance loop balances the start-up current per active channel. All IMON pins should be connected together for current balancing in parallel operation.

The sensed currents from each active MP5048A's IMON are summed together and divided by the number of active channels. The resulting average I_{LOAD} provides a measure of the total I_{LOAD}.

Current balancing is achieved by comparing the sensed current of each CS pin to the average current, which makes an appropriate adjustment to the power MOSFET V_{GATE} of each Intelli-Fuse during start-up. The equivalent average IMON resistor (R_{IMON}) can be calculated with Equation (8):

$$R_{IMON\_AVG} = R_{CS} / N \quad (8)$$

Where N is the number of active MP5048A devices (see Figure 16 on page 23).



$$R_{IMON} = R_{CS}$$

$$R_{IMON\_AVG} = \frac{R_{CS}}{N}$$

Figure 16: IMON and CS Connections in Multi-Phase Application

The start-up current balance is essential to achieving the thermal advantage of parallel operation. With good current balancing, the power loss is dissipated across multiple devices equally over a greater area.

MP5048A and MP5920 Controller Operation

The MP5048A can be combined with the MP5920 to provide PMBus telemetry, power sequencing, and black box capabilities (see Figure 17).

Using the internal 3V LDO, the MP5920 can be powered directly by the MP5048A, which allows for power sequencing when only 48V is available. The 3V LDO can be used as a bootstrap source to start up the MP5920; however, it cannot be used for continuous operation. It is expected that a 3.3V source starts up the MP5920 after initial start-up. The 3V LDO can be connected to the main system 3.3V supply via a diode. This disables the current being drawn from the internal 3V LDO, and instead uses the system's 3.3V to power the MP5920.

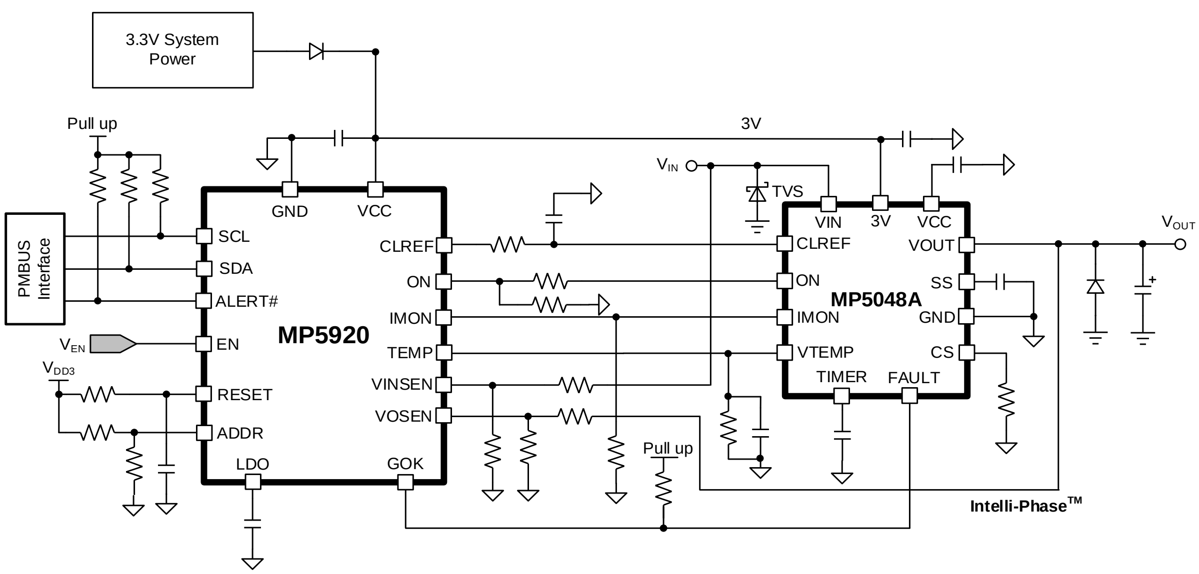


Figure 17: MP5048A and MP5920 Operation

APPLICATION INFORMATION

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. A 4-layer layout is strongly recommended for improved thermal performance. For the best results, refer to Figure 18 and follow the guidelines below:

1. Place the MP5048A close to the board's input connector to minimize trace inductance.
2. Place a small input capacitor (e.g. 100nF) close to the MP5048A's VIN and GND pins to reduce transients on the input supply line. (Transients can occur if I_{LOAD} is shut off.)
3. Place a 2.2µF capacitor as close to VCC as possible.
4. Keep the high-current path between the board's input and load close to and in parallel to the return path to reduce loop inductance.
5. Connect the analog signal ground (AGND) plane to the PCB's power ground (PGND) planes at a single point.
6. If the MP5048A is controlled by a hot-swap device, connect the reference ground of all of the signal pins to the reference ground of the controller.

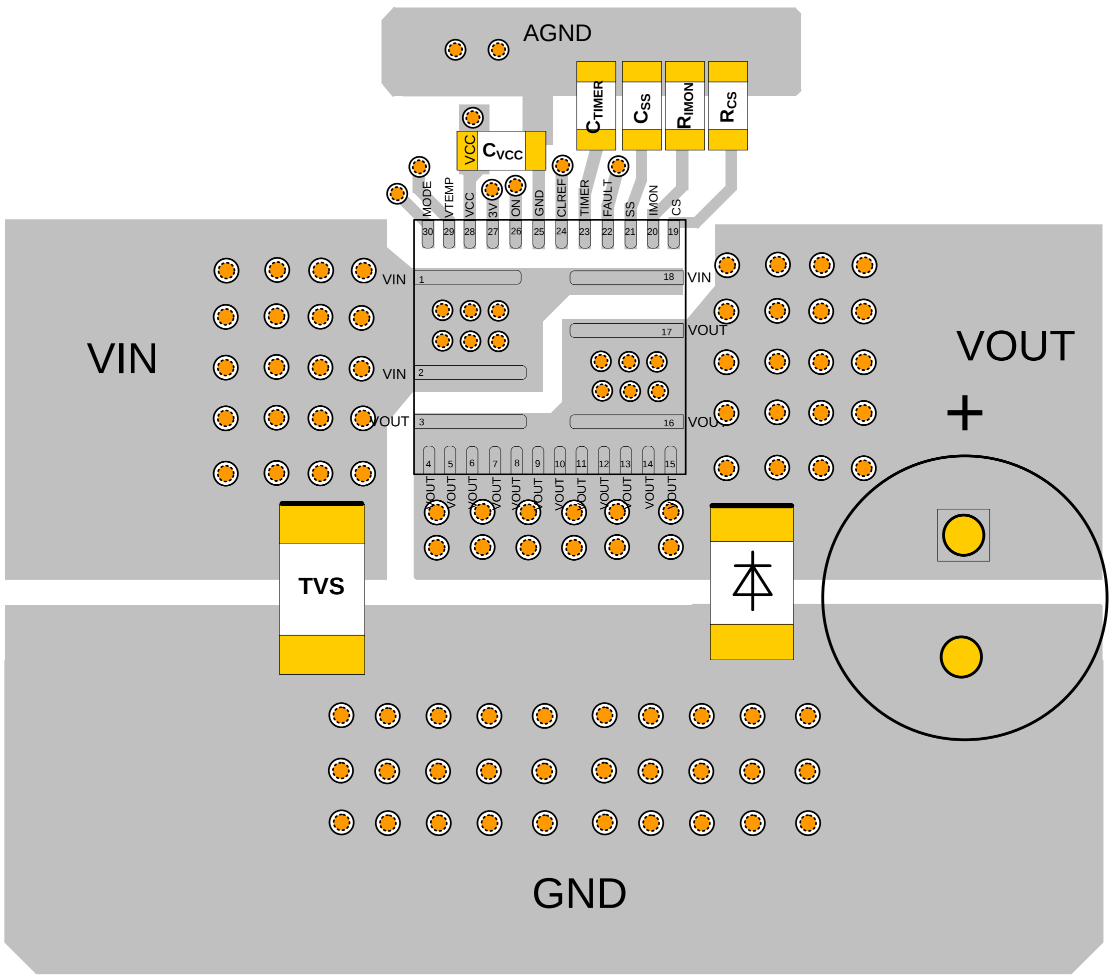


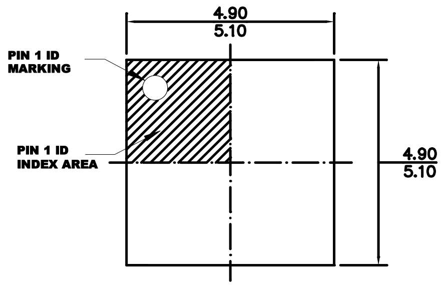
Figure 18: Recommended PCB Layout

VIN TVS Diode: 5.0SMDJ51A

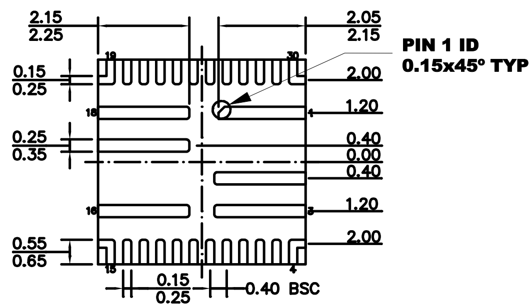
VOUT Diode: B380-13-F

PACKAGE INFORMATION

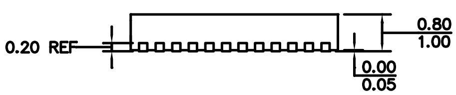
QFN-30 (5mmx5mm)



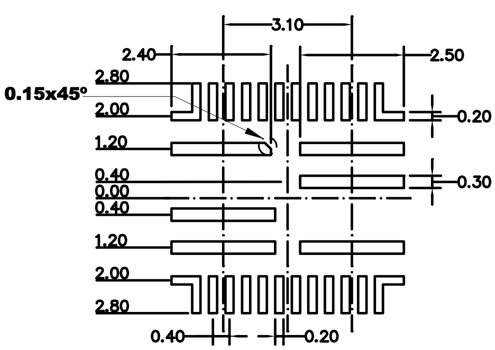
TOP VIEW



BOTTOM VIEW



SIDE VIEW

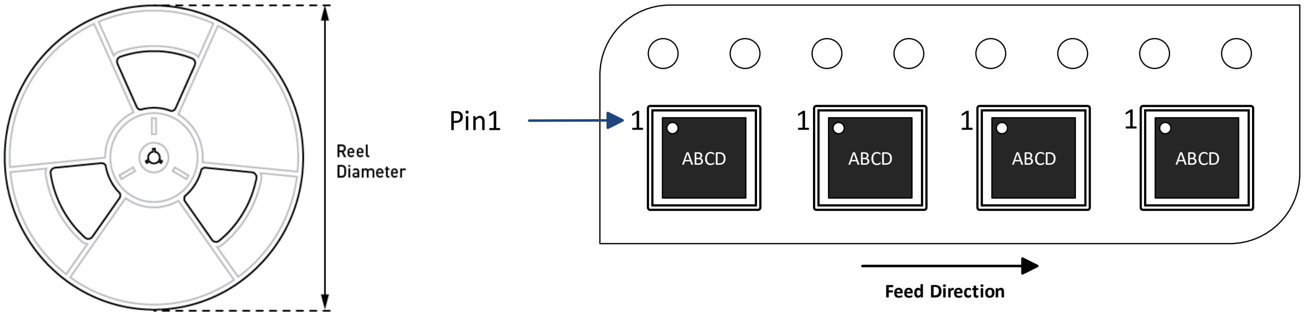


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) REFERENCEIS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP5048AGU-Z	QFN-30 (5mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/8/2022	Initial Release	-