# SN74LVC1G97-EP
# CONFIGURABLE MULTIPLE-FUNCTION GATE

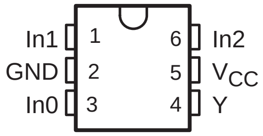
SCES461B − JUNE 2003 − REVISED FEBRUARY 2005

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree**[†]
- **Supports 5-V $V_{CC}$ Operation**
- **Inputs Accept Voltages to 5.5 V**
- **Max $t_{pd}$ of 6.3 ns at 3.3 V**
- **Low Power Consumption, 10-μA Max $I_{CC}$**
- **±24-mA Output Drive at 3.3 V**
- **$I_{off}$ Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **Choose From Nine Specific Logic Functions**

---

[†] Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

**DCK PACKAGE**
**(TOP VIEW)**



## description/ordering information

This configurable multiple-function gate is designed for 1.65-V to 5.5-V $V_{CC}$ operation.

The SN74LVC1G97 features configurable multiple functions. The output state is determined by eight patterns of 3-bit input. The user can choose the logic functions MUX, AND, OR, NAND, NOR, inverter, and noninverter. All inputs can be connected to $V_{CC}$ or GND.

This device functions as an independent gate, but because of Schmitt action, it may have different input threshold levels for positive-going ($V_{T+}$) and negative-going ($V_{T-}$) signals.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### ORDERING INFORMATION

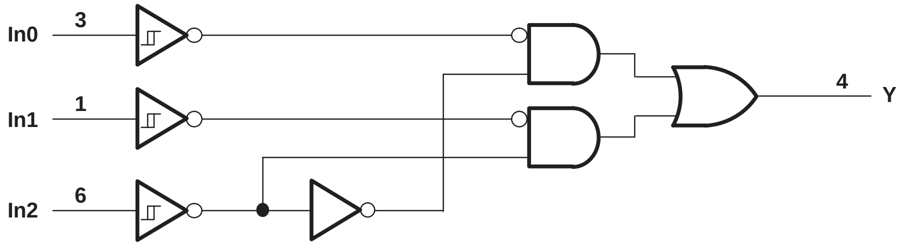
| $T_A$ | PACKAGE[‡] | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −40°C to 85°C | SOT (SC-70) − DCK | Tape and reel | SN74LVC1G97IDCKREP | CSR |

[‡] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| **In2** | **In1** | **In0** | **Y** |
| L | L | L | L |
| L | L | H | L |
| L | H | L | H |
| L | H | H | H |
| H | L | L | L |
| H | L | H | H |
| H | H | L | L |
| H | H | H | H |

## logic diagram (positive logic)



**FUNCTION SELECTION TABLE**

| LOGIC FUNCTION | FIGURE NO. |
|---|---|
| 2-to-1 data selector | 1 |
| 2-input AND gate | 2 |
| 2-input OR gate with one inverted input | 3 |
| 2-input NAND gate with one inverted input | 3 |
| 2-input AND gate with one inverted input | 4 |
| 2-input NOR gate with one inverted input | 4 |
| 2-input OR gate | 5 |
| Inverter | 6 |
| Noninverted buffer | 7 |

## logic configurations

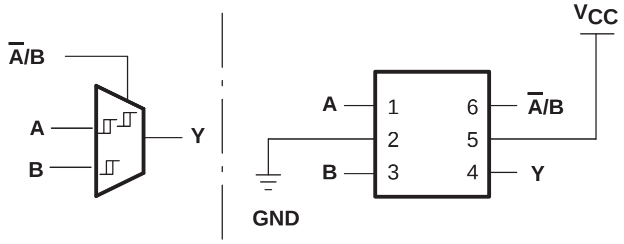


Figure 1. 2-to-1 Data Selector

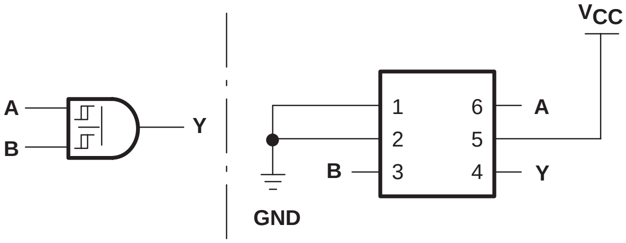


Figure 2. 2-Input AND Gate

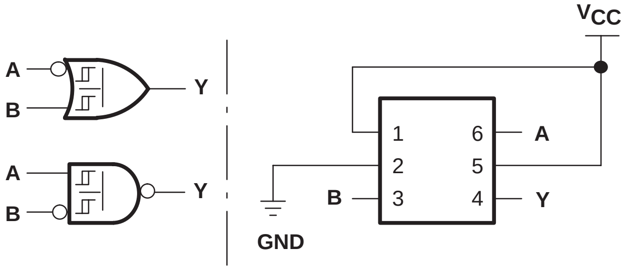


Figure 3. 2-Input OR Gate With One Inverted Input
2-Input NAND Gate With One Inverted Input

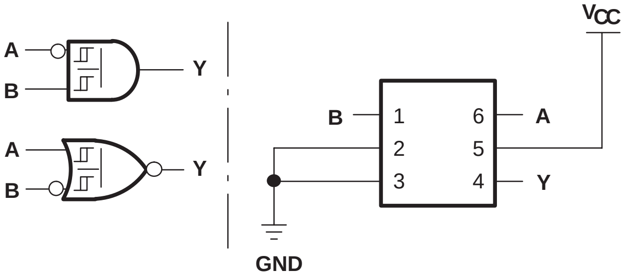


Figure 4. 2-Input AND Gate With One Inverted Input
2-Input NOR Gate With One Inverted Input

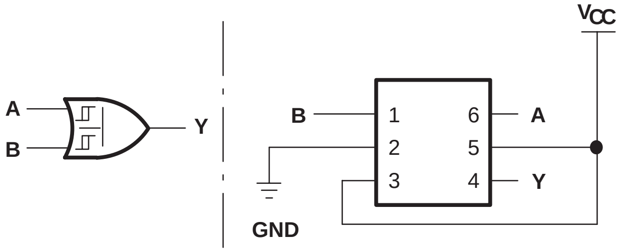


Figure 5. 2-Input OR Gate

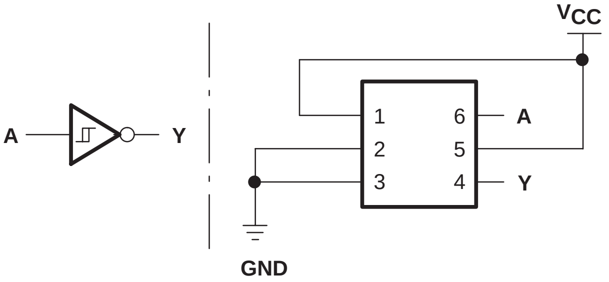


Figure 6. Inverter

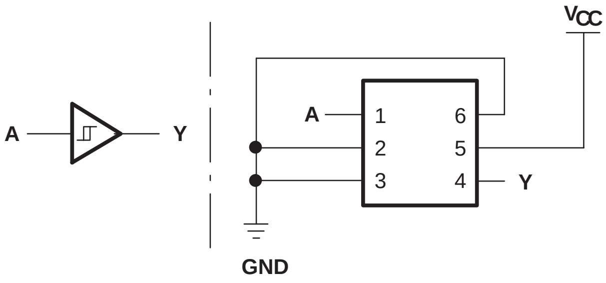


Figure 7. Noninverted Buffer

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|---|---|
| Supply voltage range, $V_{CC}$ | −0.5 V to 6.5 V |
| Input voltage range, $V_I$ (see Note 1) | −0.5 V to 6.5 V |
| Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) | −0.5 V to 6.5 V |
| Voltage range applied to any output in the high or low state, $V_O$ (see Notes 1 and 2) | −0.5 V to $V_{CC}$ + 0.5 V |
| Input clamp current, $I_{IK}$ ($V_I < 0$) | −50 mA |
| Output clamp current, $I_{OK}$ ($V_O < 0$) | −50 mA |
| Continuous output current, $I_O$ | ±50 mA |
| Continuous current through $V_{CC}$ or GND | ±100 mA |
| Package thermal impedance, $\theta_{JA}$ (see Note 3) | 259°C/W |
| Storage temperature range, $T_{stg}$ | −65°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of $V_{CC}$ is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 4)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | Operating | 1.65 | 5.5 | V |
| | | Data retention only | 1.5 | | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65 V | | −4 | mA |
| | | $V_{CC}$ = 2.3 V | | −8 | |
| | | $V_{CC}$ = 3 V | | −16 | |
| | | | | −24 | |
| | | $V_{CC}$ = 4.5 V | | −32 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | | 8 | |
| | | $V_{CC}$ = 3 V | | 16 | |
| | | | | 24 | |
| | | $V_{CC}$ = 4.5 V | | 32 | |
| $T_A$ | Operating free-air temperature | | −40 | 85 | °C |

NOTE 4: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{T+}$ Positive-going input threshold voltage | | 1.65 V | 0.79 | | 1.16 | V |
| | | 2.3 V | 1.11 | | 1.56 | |
| | | 3 V | 1.5 | | 1.87 | |
| | | 4.5 V | 2.16 | | 2.74 | |
| | | 5.5 V | 2.61 | | 3.33 | |
| $V_{T-}$ Negative-going input threshold voltage | | 1.65 V | 0.35 | | 0.62 | V |
| | | 2.3 V | 0.58 | | 0.87 | |
| | | 3 V | 0.84 | | 1.19 | |
| | | 4.5 V | 1.41 | | 1.9 | |
| | | 5.5 V | 1.87 | | 2.29 | |
| $\Delta V_T$ Hysteresis ($V_{T+} - V_{T-}$) | | 1.65 V | 0.3 | | 0.62 | V |
| | | 2.3 V | 0.4 | | 0.8 | |
| | | 3 V | 0.53 | | 0.87 | |
| | | 4.5 V | 0.71 | | 1.04 | |
| | | 5.5 V | 0.71 | | 1.11 | |
| $V_{OH}$ | $I_{OH} = -100$ µA | 1.65 V to 5.5 V | $V_{CC} - 0.1$ | | | V |
| | $I_{OH} = -4$ mA | 1.65 V | 1.2 | | | |
| | $I_{OH} = -8$ mA | 2.3 V | 1.9 | | | |
| | $I_{OH} = -16$ mA | 3 V | 2.4 | | | |
| | $I_{OH} = -24$ mA | | 2.3 | | | |
| | $I_{OH} = -32$ mA | 4.5 V | 3.8 | | | |
| $V_{OL}$ | $I_{OL} = 100$ µA | 1.65 V to 5.5 V | | | 0.1 | V |
| | $I_{OL} = 4$ mA | 1.65 V | | | 0.45 | |
| | $I_{OL} = 8$ mA | 2.3 V | | | 0.3 | |
| | $I_{OL} = 16$ mA | 3 V | | | 0.4 | |
| | $I_{OL} = 24$ mA | | | | 0.55 | |
| | $I_{OL} = 32$ mA | 4.5 V | | | 0.55 | |
| $I_I$ | $V_I = 5.5$ V or GND | 0 to 5.5 V | | | ±5 | µA |
| $I_{off}$ | $V_I$ or $V_O = 5.5$ V | 0 | | | ±10 | µA |
| $I_{CC}$ | $V_I = 5.5$ V or GND, $I_O = 0$ | 1.65 V to 5.5 V | | | 10 | µA |
| $\Delta I_{CC}$ | One input at $V_{CC} - 0.6$ V, Other inputs at $V_{CC}$ or GND | 3 V to 5.5 V | | | 500 | µA |
| $C_i$ | $V_I = V_{CC}$ or GND | 3.3 V | | 3.5 | | pF |

† All typical values are at $V_{CC} = 3.3$ V, $T_A = 25$°C.

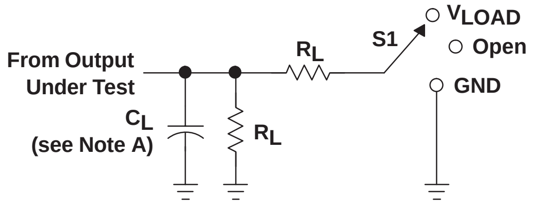
## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 8)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 5 V ± 0.5 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | Any In | Y | 3.2 | 14.4 | 2 | 8.3 | 1.5 | 6.3 | 1.1 | 5.1 | ns |

## operating characteristics, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | $V_{CC}$ = 5 V | UNIT |
|---|---|---|---|---|---|---|---|
| | | | TYP | TYP | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance | f = 10 MHz | 22 | 23 | 23 | 26 | pF |

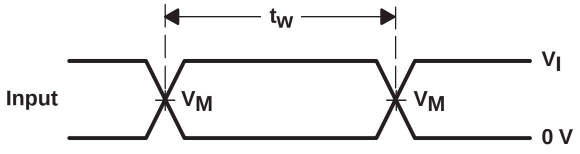
## PARAMETER MEASUREMENT INFORMATION



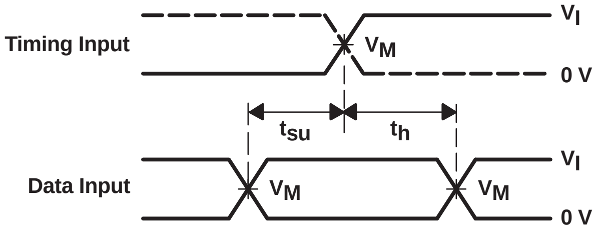
**LOAD CIRCUIT**

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

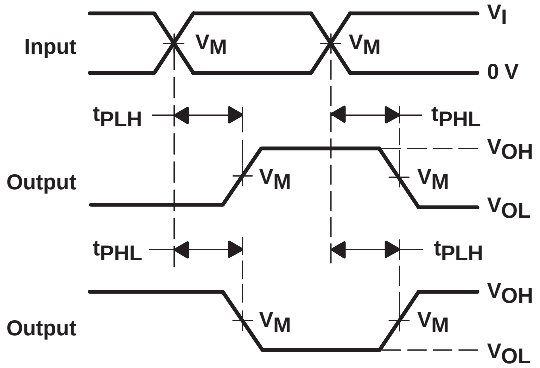
| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 3.3 V ± 0.3 V | 3 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 5 V ± 0.5 V | $V_{CC}$ | ≤2.5 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 50 pF | 500 Ω | 0.3 V |



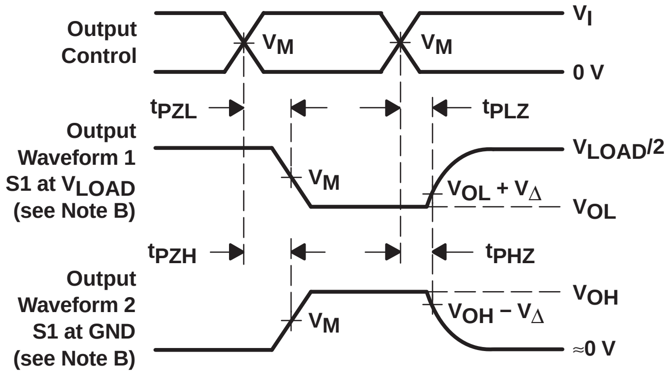
**VOLTAGE WAVEFORMS**
**PULSE DURATION**



**VOLTAGE WAVEFORMS**
**SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS**
**PROPAGATION DELAY TIMES**
**INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS**
**ENABLE AND DISABLE TIMES**
**LOW- AND HIGH-LEVEL ENABLING**

NOTES:
- A. $C_L$ includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
- F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
- G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
- H. All parameters and waveforms are not applicable to all devices.

**Figure 8. Load Circuit and Voltage Waveforms**

# PACKAGE OPTION ADDENDUM

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC1G97IDCKREP | ACTIVE | SC70 | DCK | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CSR | Samples |
| V62/03642-01XE | ACTIVE | SC70 | DCK | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CSR | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LVC1G97-EP :**

- Catalog: SN74LVC1G97

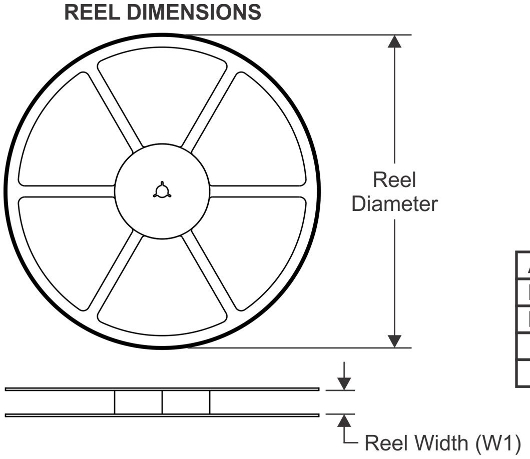
- Automotive: SN74LVC1G97-Q1

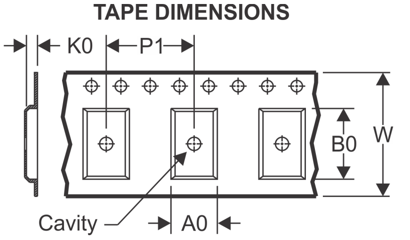
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

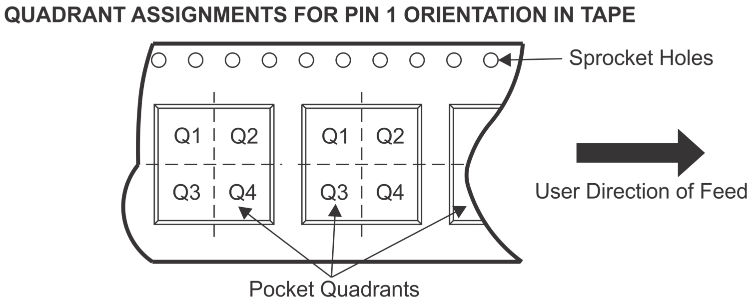
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION





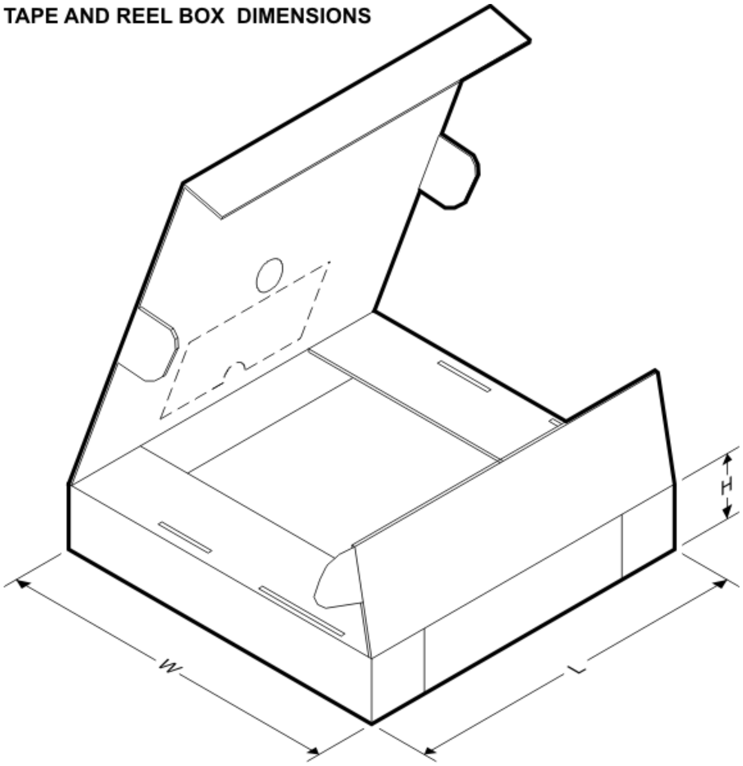
| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC1G97IDCKREP | SC70 | DCK | 6 | 3000 | 180.0 | 8.4 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |

## TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

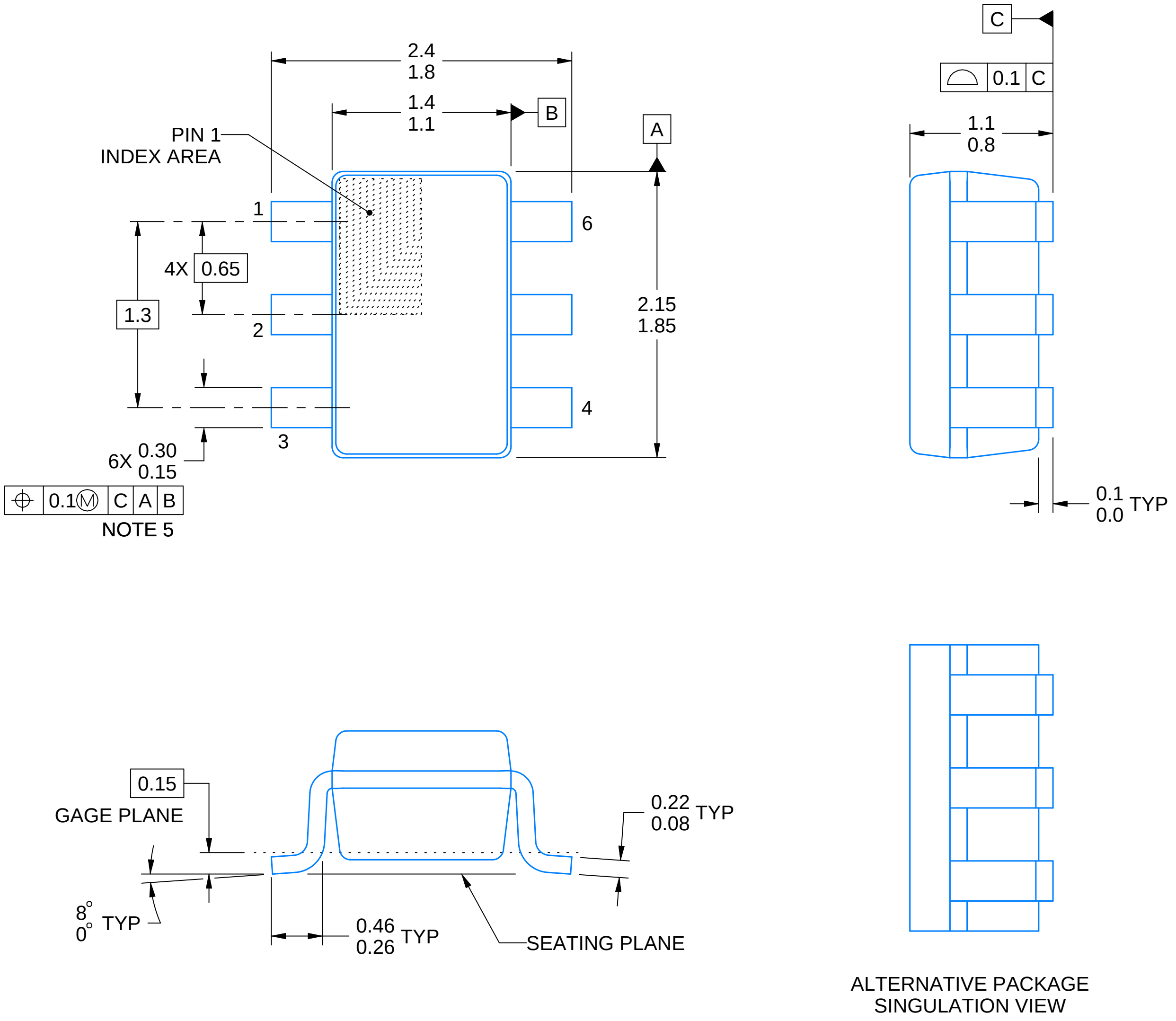
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LVC1G97IDCKREP | SC70 | DCK | 6 | 3000 | 202.0 | 201.0 | 28.0 |

# DCK0006A

# PACKAGE OUTLINE

## SOT - 1.1 max height

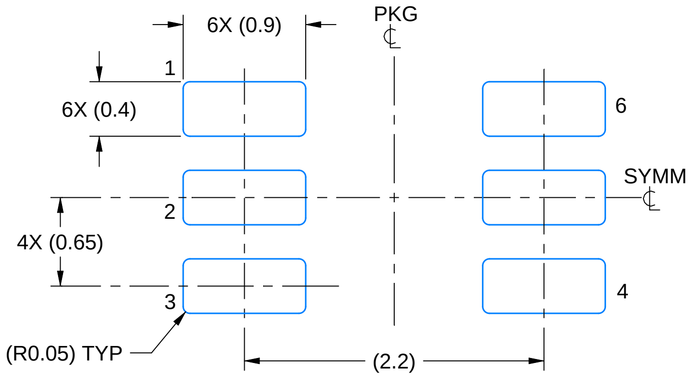
SMALL OUTLINE TRANSISTOR



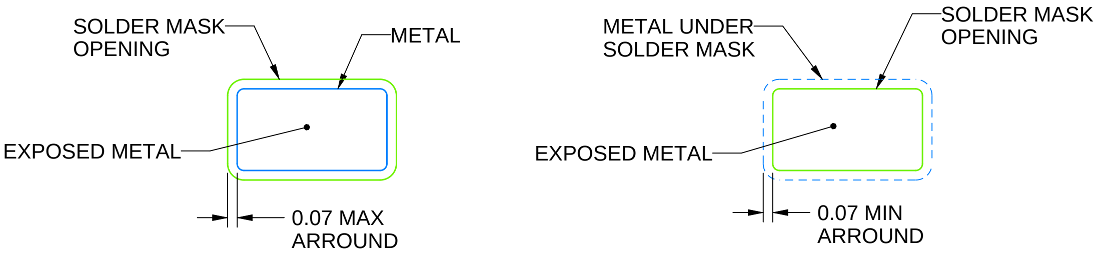
4214835/B 04/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



NON SOLDER MASK
DEFINED
(PREFERRED)

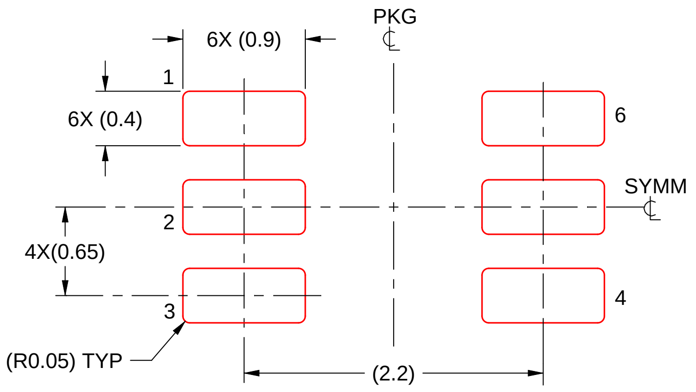
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214835/B 04/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2024, Texas Instruments Incorporated