MC74HCT132A

Quad 2-Input NAND Gate with Schmitt-Trigger Inputs with LSTTL Compatible Inputs

High−Performance Silicon−Gate CMOS

The MC74HCT132A is identical in pinout to the LS132. The device inputs are compatible with standard CMOS outputs; with pull−up resistors, they are compatible with LSTTL outputs.

The MC74HCT132A can be used to enhance noise immunity or to square up slowly changing waveforms.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements as Defined by JEDEC Standard No. 7A
- Chip Complexity: 72 FETs or 18 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
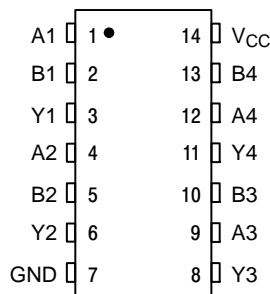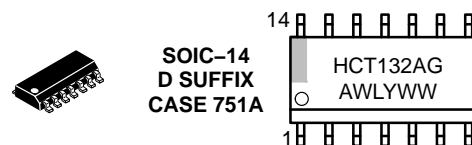- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

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MARKING DIAGRAMS

SOIC−14
D SUFFIX
CASE 751A

HCT132AG
AWLYWW

TSSOP−14
DT SUFFIX
CASE 948G

HCT
132A
ALYW▪

A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

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A1  [ 1 ●      14 ]  V_CC
B1  [ 2        13 ]  B4
Y1  [ 3        12 ]  A4
A2  [ 4        11 ]  Y4
B2  [ 5        10 ]  B3
Y2  [ 6         9 ]  A3
GND [ 7         8 ]  Y3
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Figure 1. Pin Assignment

MC74HCT132A

PIN 14 = V_{CC}
PIN 7 = GND

$$Y = \overline{AB}$$
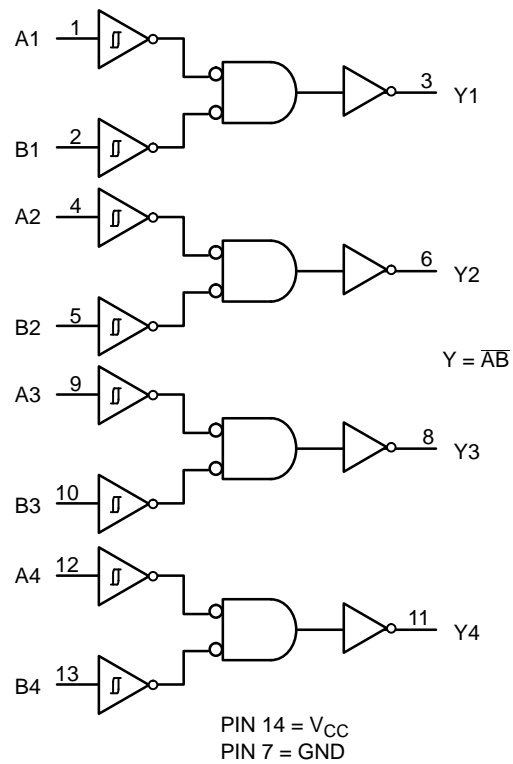
Figure 2. Logic Diagram

ORDERING INFORMATION

Device	Package	Shipping[†]
MC74HCT132ADG	SOIC−14 (Pb−Free)	55 Units / Rail
MC74HCT132ADR2G		2500 / Tape & Reel
NLV74HCT132ADR2G*		2500 / Tape & Reel
MC74HCT132ADTR2G	TSSOP−14 (Pb−Free)	2500 / Tape & Reel
NLVHCT132ADTR2G*		2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

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MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Positive DC Supply Voltage		-0.5 to $+7.0$	V
V_{IN}	Digital Input Voltage		-0.5 to $+7.0$	V
V_{OUT}	DC Output Voltage	Output in 3−State High or Low State	-0.5 to $+7.0$ -0.5 to V_{CC} $+0.5$	V
I_{IK}	Input Diode Current		-20	mA
I_{OK}	Output Diode Current		± 20	mA
I_{OUT}	DC Output Current, per Pin		± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		± 75	mA
I_{GND}	DC Ground Current per Ground Pin		± 75	mA
T_{STG}	Storage Temperature Range		-65 to $+150$	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		$+150$	°C
θ_{JA}	Thermal Resistance	14−SOIC 14−TSSOP	125 170	°C/W
P_D	Power Dissipation in Still Air at 85°C	SOIC TSSOP	500 450	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% − 35%	UL 94 V0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	>2000 >100 >500	V
$I_{Latch-Up}$	Latch−Up Performance	Above V_{CC} and Below GND at 85°C (Note 4)	± 300	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Tested to EIA/JESD22−A114−A.
2. Tested to EIA/JESD22−A115−A.
3. Tested to JESD22−C101−A.
4. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	$+125$	°C
t_r, t_f	Input Rise and Fall Time (Figure 3)	−	No Limit (Note 5)	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
5. When $V_{IN} \sim 0.5\ V_{CC}$, I_{CC} >> quiescent current.
6. Unused inputs may not be left open. All inputs must be tied to a high−logic voltage level or a low−logic input voltage level.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				$-55°C$ to $25°C$	$\leq 85°C$	$\leq 125°C$	
V_{T+}max	Maximum Positive–Going Input Threshold Voltage	V_{OUT} = 0.1 V $|I_{OUT}| \leq 20$ μA	4.5 5.5	1.9 2.1	1.9 2.1	1.9 2.1	V
V_{T+}min	Minimum Positive–Going Input Threshold Voltage	V_{OUT} = 0.1 V $|I_{OUT}| \leq 20$ μA	4.5 5.5	1.2 1.4	1.2 1.4	1.2 1.4	V
V_{T-}max	Maximum Negative–Going Input Threshold Voltage	$V_{OUT} = V_{CC} - 0.1$ V $|I_{OUT}| \leq 20$ μA	4.5 5.5	1.2 1.4	1.2 1.4	1.2 1.4	V
V_{T-}min	Minimum Negative–Going Input Threshold Voltage	$V_{OUT} = V_{CC} - 0.1$ V $|I_{OUT}| \leq 20$ μA	4.5 5.5	0.5 0.6	0.5 0.6	0.5 0.6	V
$V_H$min (Note 7)	Minimum Hysteresis Voltage	V_{OUT} = 0.1 V or $V_{CC} - 0.1$ V $|I_{OUT}| \leq 20$ μA	4.5 5.5	0.4 0.4	0.4 0.4	0.4 0.4	V
V_{OH}	Minimum High–Level Output Voltage	$V_{IN} \leq V_{T-}$min or V_{T+}max $|I_{OUT}| \leq 20$ μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		$V_{IN} \leq -V_{T-}$min or V_{T+}max $\quad\quad |I_{OUT}| \leq 4.0$ mA	4.5	3.98	3.84	3.7	
V_{OL}	Maximum Low–Level Output Voltage	$V_{IN} \geq V_{T+}$max $|I_{OUT}| \leq 20$ μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		$V_{IN} \geq V_{T+}$max $\quad |I_{OUT}| \leq 4.0$ mA	4.5	0.26	0.33	0.4	
I_{IN}	Maximum Input Leakage Current	$V_{IN} = V_{CC}$ or GND	5.5	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{IN} = V_{CC}$ or GND I_{OUT} = 0 μA	5.5	1.0	10	40	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. $V_H$min > (V_{T+}min) − (V_{T-}max); $V_H$max = (V_{T+}max) + (V_{T-}min).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns, V_{CC} = 5.0 V ± 10%)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			$-55°C$ to $25°C$	$\leq 85°C$	$\leq 125°C$	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 3 and 4)	5.0	25	31	38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 4)	5.0	15	19	22	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (per Gate) (Note 8)	24	pF

8. Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

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V_I = GND to 3.0 V
V_M = 1.3 V
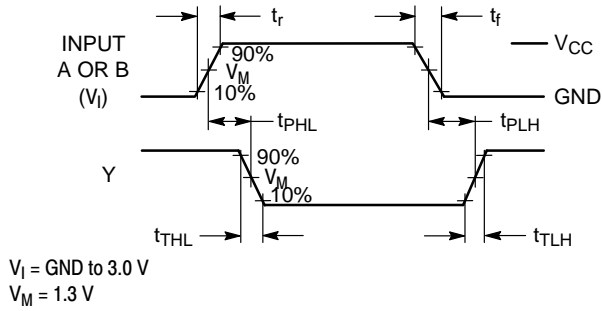
Figure 3. Switching Waveforms

*Includes all probe and jig capacitance

Figure 4. Test Circuit

(a) A SCHMITT TRIGGER SQUARES UP INPUTS
WITH SLOW RISE AND FALL TIMES

(b) A SCHMITT TRIGGER OFFERS MAXIMUM
NOISE IMMUNITY
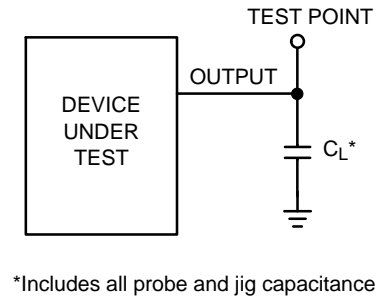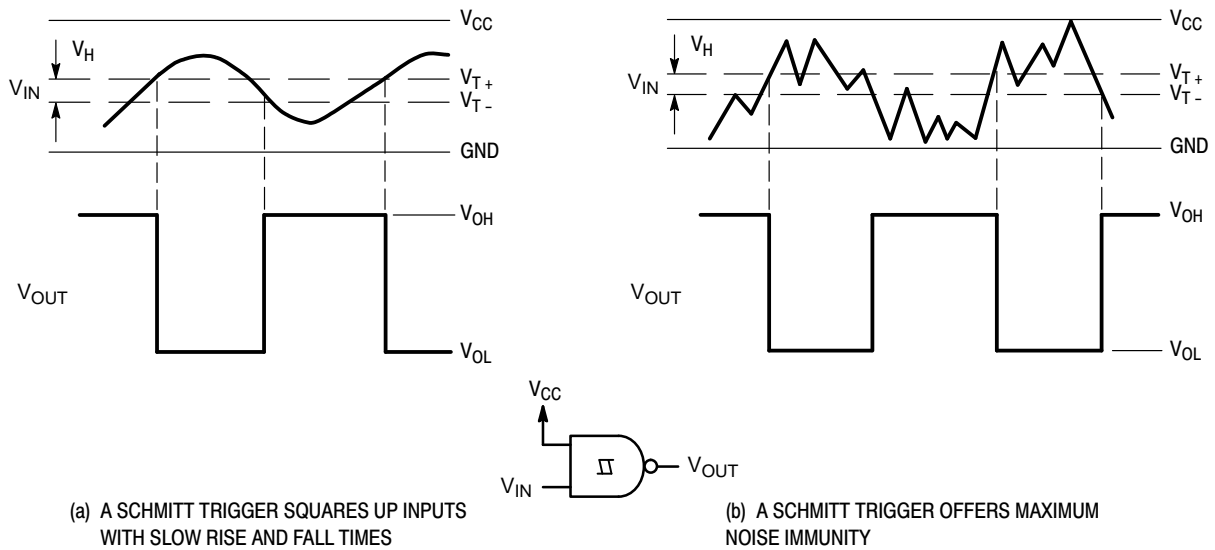
Figure 5. Typical Schmitt−Trigger Applications

ADDITIONAL INFORMATION

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