PCN Number:	20240405000.2	**PCN Date:**	April 08, 2024
Title:	Qualification of a new Die Revision, Data sheet and additional Assembly BOM options for select devices		
Customer Contact:	Change Management team	**Dept:**	Quality Services
Proposed 1st Ship Date:	October 05, 2024	**Sample requests accepted until:**	May 08, 2024*

*Sample requests received after May 08, 2024 will not be supported.

Change Type:

☐	Assembly Site	☒	Design	☐	Wafer Bump Material
☒	Assembly Process	☒	Data Sheet	☐	Wafer Bump Process
☒	Assembly Materials	☐	Part number change	☐	Wafer Fab Site
☐	Mechanical Specification	☐	Test Site	☐	Wafer Fab Material
☐	Packing/Shipping/Labeling	☐	Test Process	☐	Wafer Fab Process

PCN Details

Description of Change:

Texas Instruments is pleased to announce the qualification of a new die revision, data sheet in addition to an Assembly BOM option for the devices listed below.

Construction differences are as follows:

	Current - TITL	**Current - MLA**	**Proposed**
Wire diam/type	0.96mil Au (Die to Die) 1.0mil Cu (Die to Lead)	0.96milAu (Die to Die) 1.0mil Cu (Die to Lead)	0.80mil Cu (Die to Die & Die to Lead)
Mold compound	4221499	4211880	4211880

This particular PCN is related to TI's transition of dual-channel isolated gate drivers in narrow body package (16D) to a newly-designed circuit and to TI's most efficient manufacturing processes and technology. The newly-designed circuit includes improvements to robustness in common automotive and industrial applications. Changes in the datasheet are summarized in the table below and the new datasheet is available at www.ti.com/product/UCC21222-Q1. TI additionally offers a transition guide to ensure complete understanding of system considerations which is available upon request in the SDP (supporting data package). The changes to the manufacturing processes and technology underscore our commitment to product longevity and supply continuity.

Qual details are provided in the Qual Data Section.

The datasheets will be changing as a result of the above mentioned changes. The datasheet change details can be reviewed in the datasheet revision history. The links to the revised datasheets are available in the table below.

Changes from Revision A (February 2024) to Revision B (April 2024) **Page**

Product Folder	Current Datasheet Number	New Datasheet Number	Link to full datasheet
UCC21222-Q1	SLUSDA5A	**SLUSDA5B**	http://www.ti.com/product/UCC21222-Q1

Reason for Change:

Continuity of Supply
These changes are to transition TI's dual-channel isolated gate drivers in narrow body package (16D) to TI's most efficient manufacturing processes and technology, underscoring our commitment to product longevity and supply continuity. Additionally, the newly-designed circuit includes improvements to robustness in common automotive and industrial applications, underscoring our commitment to continuous improvements in both product quality and end system robustness.

Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):

None

Impact on Environmental Ratings

Checked boxes indicate the status of environmental ratings following implementation of this change. If below boxes are checked, there are no changes to the associated environmental ratings.

RoHS	REACH	Green Status	IEC 62474
☒ No Change	☒ No Change	☒ No Change	☒ No Change

Changes to product identification resulting from this PCN:

Die Rev:

Current **New**

Die Rev [2P]	**Die Rev [2P]**
B, C	**A**

Product Affected:

UCC21222QDRQ1

Qualification Report

Automotive Qualification Summary
(As per AEC-Q100 Rev. H and JEDEC Guidelines)
Approve Date 21-December-2023

Product Attributes

Attributes	Qual Device: UCC21330BQDRQ1	QBS Package Reference: ISO6721BQDRQ1	QBS Package Reference: TLV9022QDRQ1	QBS Process Reference: UCC23513QDWYQ1	QBS Product Reference: UCC21551CQDWKRQ1
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Power Management	Interface	Signal Chain	Power Management	Power Management
Wafer Fab Supplier	RFAB, RFAB, RFAB	MH8, MH8	RFAB	RFAB, RFAB	RFAB, RFAB, RFAB
Assembly Site	MLA	MLA	MLA	TAI	MLA
Package Group	SOIC	SOIC	-	SOIC	SOIC
Package Designator	D	D	D	DWY	DWK
Pin Count	16	8	8	6	14

QBS: Qual By Similarity
Qual Device UCC21330BQDRQ1 is qualified at MSL2 260C

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: UCC21330BQDRQ1	QBS Package Reference: ISO6721BQDRQ1	QBS Package Reference: TLV9022QDRQ1	QBS Process Reference: UCC23513QDWYQ1	QBS Product Reference: UCC21551CQDWKRQ1
Test Group A - Accelerated Environment Stress Tests												
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	-	No Fails	No Fails	-	-
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL2 260C	-	No Fails	-	-	-	-
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	-	3/231/0	3/231/0	-	-
AC/UHAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Autoclave	121C/15psig	96 Hours	-	3/231/0	-	-	-
AC/UHAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Unbiased HAST	130C/85%RH	96 Hours	-	-	3/231/0	-	-
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	3/231/0	3/231/0	3/231/0	-	-

HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	150C	1000 Hours	-	-	3/135/0	-	-
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	175C	500 Hours	-	3/135/0	-	-	-
Test Group B - Accelerated Lifetime Simulation Tests												
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	125C	1000 Hours	-	-	-	3/231/0	1/77/0
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate	125C	48 Hours	-	-	-	3/2400/0	-
Test Group C - Package Assembly Integrity Tests												
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	3/228/0	3/90/0	-	-
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	3/228/0	3/90/0	-	-
SD	C3	JEDEC J-STD-002	1	15	PB Solderability	>95% Lead Coverage	-	-	1/15/0	-	-	-
SD	C3	JEDEC J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	-	1/15/0	-	-	-
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	3/30/0	3/30/0	3/30/0	-	-
Test Group D - Die Fabrication Reliability Tests												
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDDB	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
BTI	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group E - Electrical Verification Tests												
ESD	E2	AEC Q100-002	1	3	ESD HBM	-	2000 Volts	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0
ESD	E3	AEC Q100-011	1	3	ESD CDM	-	500 Volts	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0
LU	E4	AEC Q100-004	1	6	Latch-Up	Per AEC Q100-004	-	1/6/0	1/6/0	1/6/0	1/6/0	1/6/0
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	1/30/0	3/90/0	3/90/0	3/90/0	3/90/0

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Ambient Operating Temperature by Automotive Grade Level:

Grade 0 (or E): -40C to +150C
Grade 1 (or Q): -40C to +125C
Grade 2 (or T): -40C to +105C
Grade 3 (or I) : -40C to +85C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

Room/Hot/Cold : HTOL, ED
Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
Room : AC/uHAST
Quality and Environmental data is available at TI's external Web site: http://www.ti.com/

Qualification Report

Automotive New Product Qualification Summary
(As per AEC-Q100, AEC-Q006, and JEDEC Guidelines)

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: ISO6763QDWRQ1
Test Group A - Accelerated Environment Stress Tests								
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL2 260C	-	No Fails
PC	A1.1	-	3	22	SAM Precon Pre	Review for delamination	-	3/66/0
PC	A1.2	-	3	22	SAM Precon Post	Review for delamination	-	3/66/0
HAST	A2.1	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	3/231/0
HAST	A2.1.2	-	3	1	Cross Section, post bHAST, 1X	Post stress cross section	Completed	-
HAST	A2.1.3	-	3	30	Wire Bond Shear, post bHAST, 1X	Post stress	Wires	-
HAST	A2.1.4	-	3	30	Bond Pull over Stitch, post bHAST, 1X	Post stress	Wires	-
HAST	A2.1.5	-	3	30	Bond Pull over Ball, post bHAST, 1X	Post stress	Wires	-
HAST	A2.2	JEDEC JESD22-A110	3	70	Biased HAST	130C/85%RH	192 Hours	3/210/0
HAST	A2.2.1	-	3	22	SAM Analysis, post bHAST 2X	Review for delamination	Completed	3/66/0
HAST	A2.2.2	-	3	1	Cross Section, post bHAST, 2X	Post stress cross section	Completed	3/3/0
HAST	A2.2.3	-	3	30	Wire Bond Shear, post bHAST, 2X	Post stress	Wires	3/9/0
HAST	A2.2.4	-	3	30	Bond Pull over Stitch, post bHAST, 2X	Post stress	Wires	3/9/0
HAST	A2.2.5	-	3	30	Bond Pull over Ball, post bHAST, 2X	Post stress	Wires	3/9/0
TC	A4.1	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	3/231/0
TC	A4.1.1	-	3	22	SAM Analysis, post TC 1X	Review for delamination	Completed	-
TC	A4.1.2	-	3	1	Cross Section, post TC, 1X	Post stress cross section	Completed	-
TC	A4.1.3	-	3	30	Wire Bond Shear, post TC, 1X	Post stress	Wires	-
TC	A4.1.4	-	3	30	Bond Pull over Stitch, post TC, 1X	Post stress	Wires	-
TC	A4.1.5	-	3	30	Bond Pull over Ball, post TC, 1X	Post stress	Wires	-
TC	A4.2	JEDEC JESD22-A104 and Appendix 3	3	70	Temperature Cycle	-65C/150C	1000 Cycles	3/210/0
TC	A4.2.1	-	3	22	SAM Analysis, post TC, 2X	Review for delamination	Completed	3/66/0
TC	A4.2.2	-	3	1	Cross Section, post TC, 2X	Post stress cross section	Completed	3/3/0
TC	A4.2.3	-	3	30	Wire Bond Shear, post TC, 2X	Post stress	Wires	3/9/0
TC	A4.2.4	-	3	30	Bond Pull over Stitch, post TC, 2X	Post stress	Wires	3/9/0
TC	A4.2.5	-	3	30	Bond Pull over Ball, post TC, 2X	Post stress	Wires	3/9/0

HTSL	A6.1	JEDEC JESD22-A103	3	45	High Temperature Storage Life	150C	1000 Hours	3/135/0
HTSL	A6.1.1	-	3	1	Cross Section, post HTSL, 1X	Post stress cross section	Completed	-
HTSL	A6.2	JEDEC JESD22-A103	3	44	High Temperature Storage Life	150C	2000 Hours	3/132/0
HTSL	A6.2.1	-	3	1	Cross Section, post HTSL, 2X	Post stress cross section	Completed	3/3/0
Test Group B - Accelerated Lifetime Simulation Tests								
Test Group C - Package Assembly Integrity Tests								
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0
SD	C3	JEDEC J-STD-002	1	15	PB Solderability	>95% Lead Coverage	-	-
SD	C3	JEDEC J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	-
PD	C4	JEDEC JESD22-B100 and B108	1	10	Physical Dimensions	Cpk>1.67	-	-
Test Group D - Die Fabrication Reliability Tests								
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements
TDDB	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements
NBTI	D4	-	-	-	Negative Bias Temperature Instability	-	-	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements
Test Group E - Electrical Verification Tests								

QBS: Qual By Similarity
Qual Device ISO6763QDWRQ1 is qualified at MSL2 260C
Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
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E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):
Room/Hot/Cold : HTOL, ED
Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
Room : AC/uHAST
Quality and Environmental data is available at TI's external Web site: http://www.ti.com/

ZVEI ID reference: SEM-PA-11, SEM-PA-08, SEM-DE-02, SEM-DE-03, SEM-DS-01

For questions regarding this notice, e-mails can be sent to Change Management team or your local Field Sales Representative.

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