

Dual J-K Flip-Flop with Set and Reset

High-Performance Silicon-Gate CMOS

MC74HC112A

The MC74HC112A is identical in pinout to the LS112. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Each flip-flop is negative-edge clocked and has active-low asynchronous Set and Reset inputs.

The HC112A is identical in function to the HC76, but has a different pinout.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Similar in Function to the LS112 Except When Set and Reset are Low Simultaneously
- Chip Complexity: 100 FETs or 25 Equivalent Gates
- These are Pb-Free Devices



CASE 751B

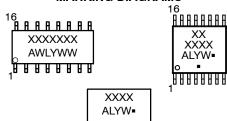






QFN16 MN SUFFIX CASE 485AW

MARKING DIAGRAMS



A = Assembly Location

WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or • = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

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^{*}For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

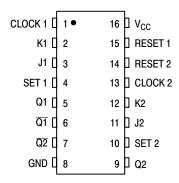
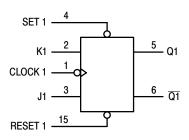


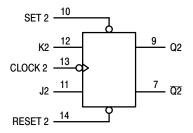
Figure 1. Pin Assignment

FUNCTION TABLE

		Inputs			Out	puts
Set	Reset	Clock	J	K	Q	Ø
L	Н	Х	Х	Х	Н	Г
Н	L	X	Χ	X	L	Н
L	L	Χ	Χ	X	L*	L*
Н	Н	~	L	L	No Ch	ange
Н	Н	~	L	н	L	Н
Н	Н	$\overline{}$	Н	L	Н	L
Н	Н	~	Н	н	Tog	gle
Н	Н	L	Χ	X	No Ch	ange
Н	Н	Н	Χ	X	No Ch	ange
Н	Н		Χ	Х	No Ch	ange

^{*}Both outputs will remain low as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.





PIN 16 = V_{CC} PIN 8 = GND

Figure 2. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V _{CC}	DC Supply Voltage		-0.5 to +6.5	V
V _{IN}	DC Input Voltage		–0.5 to V _{CC} + 0.5	V
V _{OUT}	DC Output Voltage		-0.5 to V _{CC} + 0.5	V
I _{IN}	DC Input Current, per Pin		±20	mA
I _{OUT}	DC Output Current, per Pin		±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins		±50	mA
I _{IK}	Input Clamp Current (V _{IN} < 0 or V _{IN} > V _{CC})		±20	mA
I _{OK}	Output Clamp Current (V _{OUT} < 0 or V _{OUT} > V _{CC})		±20	mA
T _{STG}	Storage Temperature		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
TJ	Junction Temperature Under Bias		±150	°C
$\theta_{\sf JA}$	Thermal Resistance (Note 1)	SOIC-16 QFN16 TSSOP-16	126 118 159	°C/W
P _D	Power Dissipation in Still Air at 25°C	SOIC-16 QFN16 TSSOP-16	995 1062 787	mW
MSL	Moisture Sensitivity		Level 1	-
F _R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	-
V _{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	> 2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V _{CC}	DC Supply Voltage		2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage		0	V _{CC}	V
T _A	Operating Temperature		– 55	+ 125	°C
t _r , t _f	Vcc	= 2.0 V = 4.5 V = 6.0 V	0 0 0	1000 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
 HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

DC ELECTRICAL CHARACTERISTICS

				Gu	aranteed Li	mit	
Symbol	Parameter	Test Conditions	V _{CC} V	–55 to 25°C	≤ 85 °C	≤125°C	Unit
V _{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\left I_{out}\right $ \leq 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\left I_{out}\right $ \leq 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V _{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \le 20 \ \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL} \qquad \begin{vmatrix} I_{out} \end{vmatrix} \le 4.0 \text{ mA} \\ I_{out} \le 5.2 \text{ mA} \end{vmatrix}$	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V _{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \le 20 \ \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\left I_{out}\right \le 4.0$ mA $\left I_{out}\right \le 5.2$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
l _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±[0.1	±[1.0	± <u>∏</u> 1.0	μΑ
Icc	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$	6.0	4	40	80	μΑ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS

			Guaranteed Limit			
Symbol	Parameter	V _{CC} V	–55 to 25°C	≤85°C	≤125°C	Unit
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 3 and 4)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q or Q (Figures 3 and 4)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Reset to Q or Q (Figures 3 and 5)	2.0 4.5 6.0	155 31 26	195 39 33	235 47 40	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Set to Q or Q (Figures 3 and 5)	2.0 4.5 6.0	165 33 28	205 41 35	250 50 43	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 4)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{in}	Maximum Input Capacitance	-	10	10	10	pF

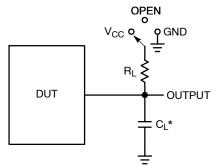
		Typical @ 25°C, V _{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Flip-Flop)*	35	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. *Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

TIMING REQUIREMENTS

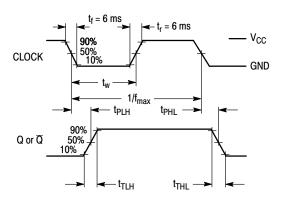
			Guaranteed Limit			
Symbol	Parameter	V _{CC} V	–55 to 25°C	≤85°C	≤125°C	Unit
t _{su}	Minimum Setup Time, J or K to Clock (Figure 6)	2 0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t _h	Minimum Hold Time, Clock to J or K (Figure 6)	2.0 4.5 6.0	3 3 3	3 3 3	3 3 3	ns
t _{rec}	Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 5)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t _w	Minimum Pulse Width, Clock (Figure 4)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t _w	Minimum Pulse Width, Set or Reset (Figure 5)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t _r , t _f	Maximum Input Rise and Fall Times (Figure 4)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

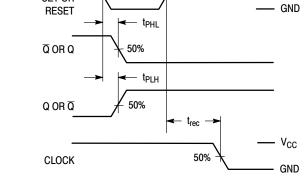
SWITCHING WAVEFORMS



Test	Switch Position	CL	R _L
t _{PLH} / t _{PHL}	Open	50 pF	1 kΩ
t _{PLZ} / t _{PZL}	V _{CC}		
t _{PHZ} / t _{PZH}	GND		

Figure 3. Test Circuit





50%

SET OR

 V_{CC}

Figure 4.

Figure 5.

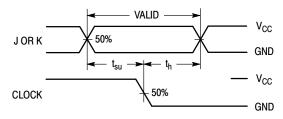


Figure 6.

^{*}C_L Includes probe and jig capacitance

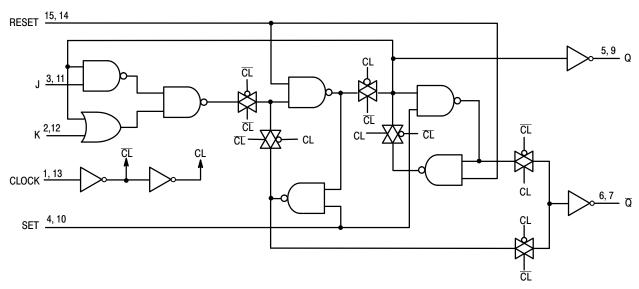


Figure 7. Expanded Logic Diagram

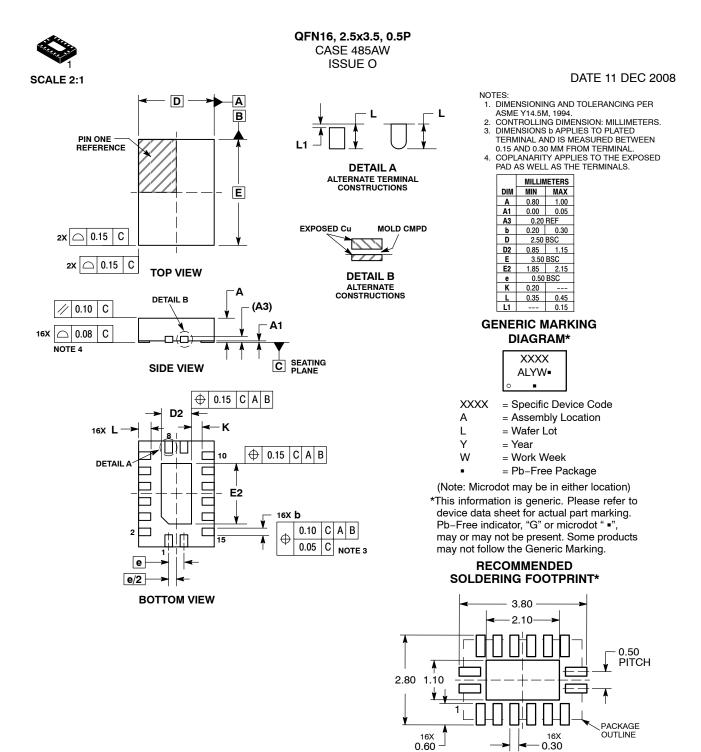
ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
MC74HC112ADR2G	HC112AG	SOIC-16	2500 / Tape & Reel
MC74HC112ADTG	HC 112A	TSSOP-16	96 Units / Rail
MC74HC112ADTR2G	HC 112A	TSSOP-16	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

^{*-}Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

PACKAGE DIMENSIONS



*For additional information on our Pb–Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DIMENSIONS: MILLIMETERS



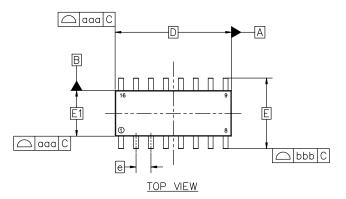


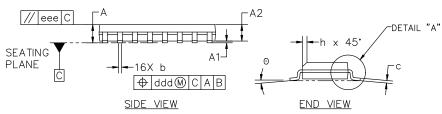
SOIC-16 9.90x3.90x1.50 1.27P CASE 751B ISSUE L

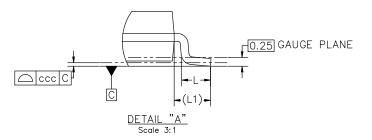
DATE 29 MAY 2024

NOTES:

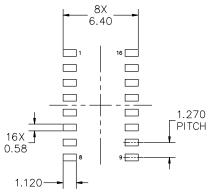
- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
- 2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
- 3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
- 4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
- DIMENSION 6 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE 6 DIMENSION AT MAXIMUM MATERIAL CONDITION.







	MILLIMETERS					
DIM	MIN	NOM	MAX			
А	1.35	1.55	1.75			
A1	0.00	0.05	0.10			
A2	1.35	1.50	1.65			
b	0.35	0.42	0.49			
С	0.19	0.22	0.25			
D	9.90 BSC					
Е	6.00 BSC					
E1	3.90 BSC					
е		1.27 BSC				
h	0.25		0.50			
L	0.40	0.83	1.25			
L1		1.05 REF				
Θ	0.		7°			
TOLERAN	CE OF FO	RM AND	POSITION			
aaa		0.10				
bbb		0.20				
ссс		0.10				
ddd		0.25				
eee		0.10				



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR
PB-FREE STRATEGY AND SOLDERING DETAILS,
PLEASE DOWNLOAD THE onsemi SOLDERING
AND MOUNTING TECHNIQUES REFERENCE
MANUAL, SOLDERRM/D

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DESCRIPTION:	SOIC-16 9.90X3.90X1.50 1	.27P	PAGE 1 OF 2		

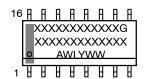
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SOIC-16 9.90x3.90x1.50 1.27P CASE 751B ISSUE L

DATE 29 MAY 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code

A = Assembly Location

WL = Wafer Lot
 Y = Year
 WW = Work Week
 G = Pb-Free Package

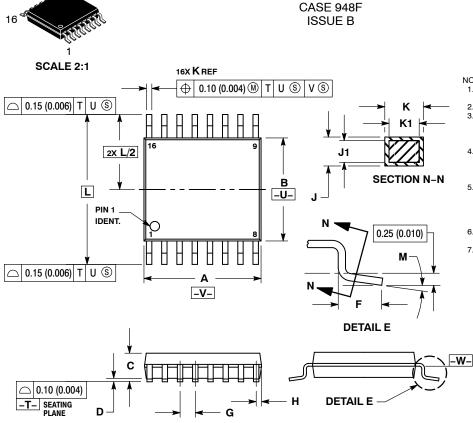
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

077/15/		077450		077/15.0		T/15 4	
STYLE 1: PIN 1.	COLLECTOR	STYLE 2:	CATHODE	STYLE 3: PIN 1.		TYLE 4: PIN 1.	COLLECTOR DVF #1
PIN 1. 2.		PIN 1. 2.		PIN 1. 2.	COLLECTOR, DYE #1 BASE, #1	PIN 1. 2.	
2. 3.	EMITTER	2. 3.	NO CONNECTION	2. 3.		2. 3.	
	NO CONNECTION	3. 4.					
4.	EMITTER	4. 5.		4.		4.	
5.	BASE	5. 6.	NO CONNECTION	5.	,	5.	
6. 7.		o. 7.		6.	EMITTER, #2	6.	
7. 8.		7. 8.	CATHODE	7. 8.			COLLECTOR, #4 COLLECTOR, #4
8. 9.		8. 9.			COLLECTOR, #2		BASE, #4
9. 10.			ANODE		BASE. #3		EMITTER, #4
	NO CONNECTION						
	EMITTER	11.	CATHODE		EMITTER, #3 COLLECTOR, #3		BASE, #3
							EMITTER, #3
	BASE		CATHODE		COLLECTOR, #4		BASE, #2
	COLLECTOR	14.			BASE, #4		EMITTER, #2
15.			ANODE		EMITTER, #4		BASE, #1
16.	COLLECTOR	16.	CATHODE	16.	COLLECTOR, #4	16.	EMITTER, #1
STYLE 5:		STYLE 6:		STYLE 7:			
PIN 1.	,	PIN 1.		PIN 1.			
PIN 1. 2.	DRAIN, #1	PIN 1. 2.	CATHODE	PIN 1. 2.	COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3.	DRAIN, #1 DRAIN, #2	PIN 1. 2. 3.	CATHODE CATHODE	PIN 1. 2. 3.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4.	DRAIN, #1 DRAIN, #2 DRAIN, #2	PIN 1. 2. 3. 4.	CATHODE CATHODE CATHODE	PIN 1. 2. 3. 4.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH		
PIN 1. 2. 3. 4. 5.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3	PIN 1. 2. 3. 4. 5.	CATHODE CATHODE CATHODE CATHODE	PIN 1. 2. 3. 4. 5.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4. 5. 6.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3	PIN 1. 2. 3. 4. 5. 6.	CATHODE CATHODE CATHODE CATHODE CATHODE	PIN 1. 2. 3. 4. 5.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4. 5. 6.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4	PIN 1. 2. 3. 4. 5. 6.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE	PIN 1. 2. 3. 4. 5. 6. 7.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4. 5. 6.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4	PIN 1. 2. 3. 4. 5. 6.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE	PIN 1. 2. 3. 4. 5.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH		
PIN 1. 2. 3. 4. 5. 6.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4 GATE, #4	PIN 1. 2. 3. 4. 5. 6.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE	PIN 1. 2. 3. 4. 5. 6. 7.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH		
PIN 1. 2. 3. 4. 5. 6. 7.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4 SOURCE, #4	PIN 1. 2. 3. 4. 5. 6. 7.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE ANODE	PIN 1. 2. 3. 4. 5. 6. 7.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4 GATE, #4 SOURCE, #4 GATE, #3	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE ANODE ANODE ANODE	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #3 DRAIN, #4 GATE, #4 GATE, #4 SOURCE, #4 SOURCE, #3	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE ANODE ANODE ANODE ANODE ANODE	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 GATE, #4 SOURCE, #4 GATE, #3 SOURCE, #3 GATE, #2	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE ANODE ANODE ANODE ANODE ANODE ANODE ANODE	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GOMMON DRAIN (OUTPUT) GATE N-CH		
PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4 DRAIN, #4 GATE, #4 SOURCE, #4 GATE, #3 SOURCE, #3 GATE, #2 SOURCE, #2 SOURCE, #2	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT) CATE N-CH COMMON DRAIN (OUTPUT)		
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TSSOP-16 WB

DATE 19 OCT 2006

NOTES

- DIMENSIONING AND TOLERANCING PER
- ANSI Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT
- EXCEED 0.15 (0.006) PER SIDE.
 DIMENSION B DOES NOT INCLUDE
 INTERLEAD FLASH OR PROTRUSION.
- INTERLEAD FLASH OR PROTRUSION.
 INTERLEAD FLASH OR PROTRUSION SHALL
 NOT EXCEED 0.25 (0.010) PER SIDE.
 DIMENSION K DOES NOT INCLUDE DAMBAR
 PROTRUSION. ALLOWABILE DAMBAR
 PROTRUSION SHALL BE 0.08 (0.003) TOTAL
 IN EXCESS OF THE K DIMENSION AT
 MAXIMUM MATERIAL CONDITION.
 TERMINIAL NILMBERS ADE SUCUMI ECD
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	4.90	5.10	0.193	0.200
В	4.30	4.50	0.169	0.177
С		1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
Н	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
М	0 °	8°	0°	8 °

RECOMMENDED SOLDERING FOOTPRINT*

7.06 ٦ 1 0.65 **PITCH** 16X 0.36 1.26 **DIMENSIONS: MILLIMETERS**

GENERIC MARKING DIAGRAM*



= Specific Device Code XXXX Α = Assembly Location

= Wafer Lot L = Year W = Work Week G or • = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present. Some products may not follow the Generic Marking.

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