74LVT16374A; 74LVTH16374A

3.3 V 16-bit edge-triggered D-type flip-flop; 3-state

Rev. 13 — 21 March 2024 Product data sheet

1. General description

The 74LVT16374A; 74LVTH16374A is a 16-bit edge-triggered D-type flip-flop with 3-state outputs. The device can be used as two 8-bit flip-flops or one 16-bit flip-flop. The device features two clocks (1CP and 2CP) and two output enables (1$\overline{OE}$ and 2$\overline{OE}$), each controlling 8-bits. The flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (nCP) transition. A HIGH on n$\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the n$\overline{OE}$ input does not affect the state of the flip-flops.

2. Features and benefits

- 16-bit edge-triggered flip-flop
- 3-state buffers
- Output capability: +64 mA and -32 mA
- Wide supply voltage range from 2.7 to 3.6 V
- Overvoltage tolerant inputs to 5.5 V
- BiCMOS high speed and output drive
- Direct interface with TTL levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs. (74LVTH16374A only)
- Live insertion and extraction permitted
- Power-up reset
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 500 mA per JESD 78 Class II Level B
- Complies with JEDEC standard JESD8C (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to 85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVT16374ADGG 74LVTH16374ADGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

4. Functional diagram

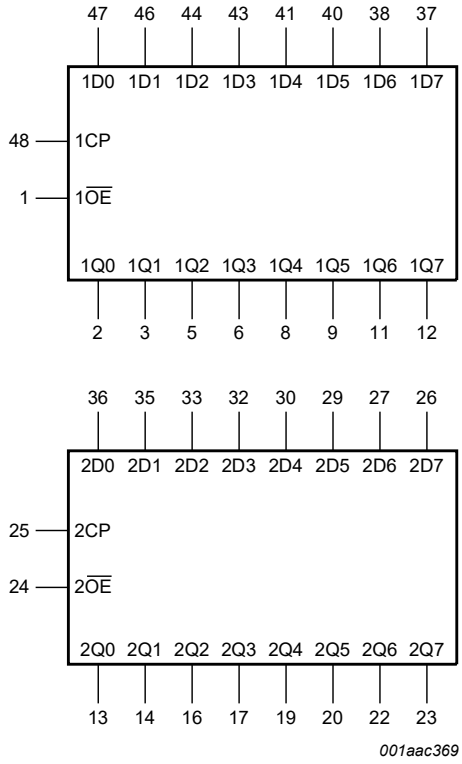


Fig. 1. Logic symbol

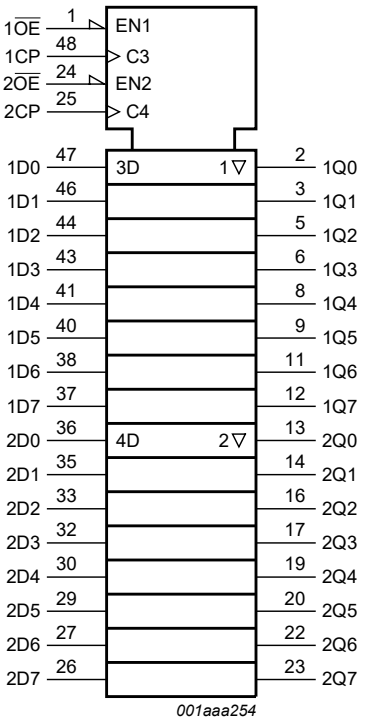


Fig. 2. IEC logic symbol

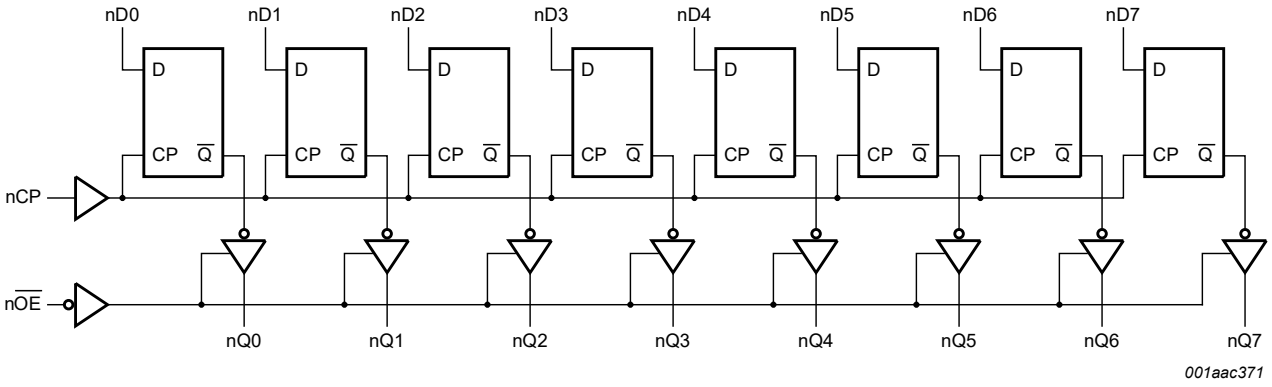
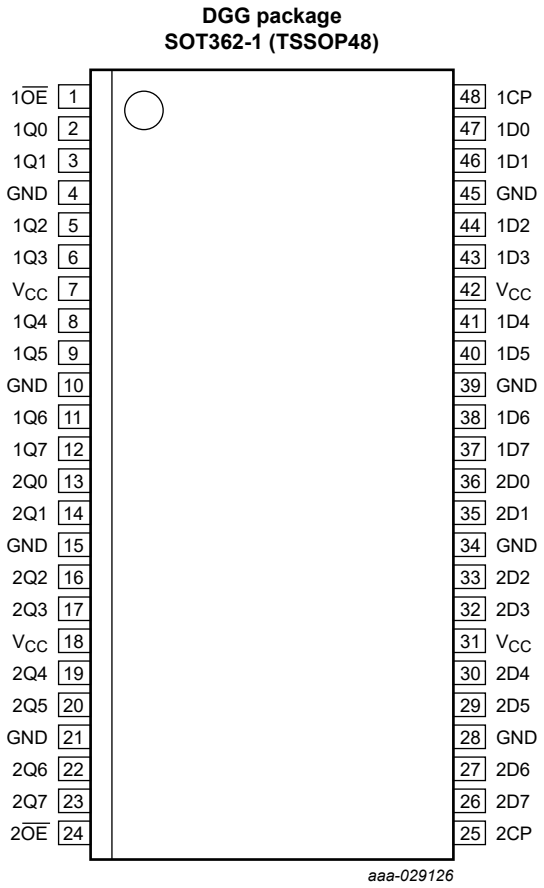


Fig. 3. Logic diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1$\overline{OE}$, 2$\overline{OE}$	1, 24	output enable input (active LOW)
1CP, 2CP	48, 25	clock input
1Q0, 1Q1, 1Q2, 1Q3, 1Q4, 1Q5, 1Q6, 1Q7	2, 3, 5, 6, 8, 9, 11, 12	data output
2Q0, 2Q1, 2Q2, 2Q3, 2Q4, 2Q5, 2Q6, 2Q7	13, 14, 16, 17, 19, 20, 22, 23	data output
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V_{CC}	7, 18, 31, 42	supply voltage
1D0, 1D1, 1D2, 1D3, 1D4, 1D5, 1D6, 1D7	47, 46, 44, 43, 41, 40, 38, 37	data input
2D0, 2D1, 2D2, 2D3, 2D4, 2D5, 2D6, 2D7	36, 35, 33, 32, 30, 29, 27, 26	data input

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the HIGH-to-LOW clock transition;
L = LOW voltage level; l = LOW voltage level one set-up time prior to the HIGH-to-LOW clock transition;
NC = no change; X = don't care;
Z = high-impedance OFF-state; ↑ = LOW-to-HIGH clock transition.

Operating mode	Input			Internal register	Output
	$n\overline{OE}$	nCP	nDn		nQ0 to nQ7
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Hold	L	NC	X	NC	NC
Disable outputs	H	NC	X	NC	Z
	H	↑	nDn	nDn	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage	[1]	-0.5	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state [1]	-0.5	+7.0	V
I_{IK}	input clamping current	V_I < 0 V	-50	-	mA
I_{OK}	output clamping current	V_O < 0 V	-50	-	mA
I_O	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-64	-	mA
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature	[2]	-	150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +85 °C	-	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.7	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		-32	-	-	mA
I_{OL}	LOW-level output current	none	-	-	32	mA
		current duty cycle ≤ 50 %; f_i ≥ 1 kHz	-	-	64	mA
T_{amb}	ambient temperature	in free-air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
V_{IK}	input clamping voltage	V_{CC} = 2.7 V; I_{IK} = -18 mA	-1.2	-0.85	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = -100 µA; V_{CC} = 2.7 V to 3.6 V	V_{CC} - 0.2	V_{CC}	-	V
		I_{OH} = -8 mA; V_{CC} = 2.7 V	2.4	2.5	-	V
		I_{OH} = -32 mA; V_{CC} = 3.0 V	2.0	2.3	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 2.7 V				
		I_{OL} = 100 µA	-	0.07	0.2	V
		I_{OL} = 24 mA	-	0.3	0.5	V
		V_{CC} = 3.0 V				
		I_{OL} = 16 mA	-	0.25	0.4	V
		I_{OL} = 32 mA	-	0.3	0.5	V
		I_{OL} = 64 mA	-	0.4	0.55	V
$V_{OL(pu)}$	power-up LOW-level output voltage	V_{CC} = 3.6 V; I_O = 1 mA; V_I = V_{CC} or GND [2]	-	0.1	0.55	V
I_I	input leakage current	control pins				
		V_{CC} = 3.6 V; V_I = V_{CC} or GND	-	0.1	±1	µA
		V_{CC} = 0 V or 3.6 V; V_I = 5.5 V	-	0.4	10	µA
		input data pins [3]				
		V_{CC} = 0 V or 3.6 V; V_I = 5.5 V	-	0.4	10	µA
		V_{CC} = 3.6 V; V_I = V_{CC}	-	0.1	1	µA
		V_{CC} = 3.6 V; V_I = 0 V	-5	-0.4	-	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 0 V to 4.5 V	-	0.1	±100	µA
I_{BHL}	bus hold LOW current	V_{CC} = 3 V; V_I = 0.8 V	75	135	-	µA
I_{BHH}	bus hold HIGH current	V_{CC} = 3 V; V_I = 2.0 V	-	-135	-75	µA
I_{BHLO}	bus hold LOW overdrive current	input data pins; V_I = 0 V to 3.6 V; V_{CC} = 3.6 V [4]	500	-	-	µA

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
I_{BHHO}	bus hold HIGH overdrive current	input data pins; V_I = 0 V to 3.6 V; V_{CC} = 3.6 V [4]	-	-	-500	µA
I_{LO}	output leakage current	output in HIGH-state when $V_O > V_{CC}$; V_O = 5.5 V; V_{CC} = 3.0 V	-	50	125	µA
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} \leq$ 1.2 V; V_O = 0.5 V to V_{CC}; V_I = GND or V_{CC}; n$\overline{OE}$ = don't care [5]	-	1	±100	µA
I_{OZ}	OFF-state output current	V_{CC} = 3.6 V; $V_I = V_{IH}$ or V_{IL}				
		output HIGH: V_O = 3.0 V	-	0.5	5	µA
		output LOW: V_O = 0.5 V	-5	0.5	-	µA
I_{CC}	supply current	V_{CC} = 3.6 V; V_I = GND or V_{CC}; I_O = 0 A				
		outputs HIGH	-	0.07	0.12	mA
		outputs LOW	-	4.0	6.0	mA
		outputs disabled [6]	-	0.07	0.12	mA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 3.0 V to 3.6 V; one input at V_{CC} - 0.6 V, other inputs at V_{CC} or GND [7]	-	0.1	0.2	mA
C_I	input capacitance	input pins; V_I = 0 V or 3.0 V	-	3	-	pF
C_O	output capacitance	output pins nQn; outputs disabled; V_O = 0 V or V_{CC}	-	9	-	pF

[1] Typical values are measured at V_{CC} = 3.3 V and at T_{amb} = 25 °C.
[2] For valid test results, data must not be loaded into the flips-flops (or latches) after applying power.
[3] Unused pins at V_{CC} or GND.
[4] This is the bus hold overdrive current required to force the input to the opposite logic state.
[5] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 µs is permitted. This parameter is valid for T_{amb} = 25 °C only.
[6] I_{CC} is measured with outputs pulled to V_{CC} or GND.
[7] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

Table 7. Dynamic characteristics

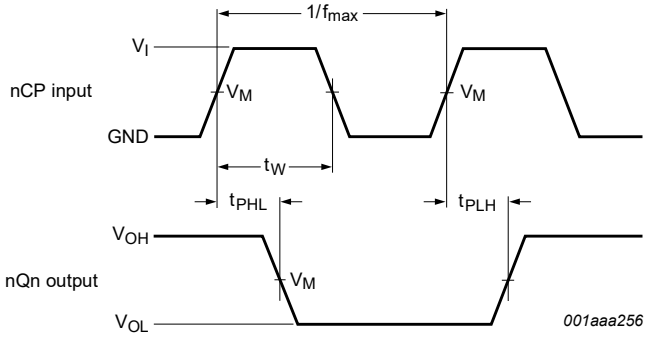
Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
f_{max}	maximum frequency	nCP; V_{CC} = 3.3 V ± 0.3 V; see Fig. 4	150	-	-	MHz
t_{PLH}	LOW to HIGH propagation delay	nCP to nQn; see Fig. 4				
		V_{CC} = 3.3 V ± 0.3 V	1.5	2.9	5.0	ns
		V_{CC} = 2.7 V	-	-	5.6	ns
t_{PHL}	HIGH to LOW propagation delay	nCP to nQn; see Fig. 4				
		V_{CC} = 3.3 V ± 0.3 V	1.5	3.0	5.0	ns
		V_{CC} = 2.7 V	-	-	5.6	ns
t_{PZH}	OFF-state to HIGH propagation delay	n$\overline{OE}$ to nQn; see Fig. 5				
		V_{CC} = 3.3 V ± 0.3 V	1.5	3.2	4.8	ns
		V_{CC} = 2.7 V	-	-	6.0	ns
t_{PZL}	OFF-state to LOW propagation delay	n$\overline{OE}$ to nQn; see Fig. 5				
		V_{CC} = 3.3 V ± 0.3 V	1.5	3.0	4.6	ns
		V_{CC} = 2.7 V	-	-	5.2	ns

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
t_{PHZ}	HIGH to OFF-state propagation delay	$n\overline{OE}$ to nQn; see Fig. 5				
		V_{CC} = 3.3 V ± 0.3 V	1.5	3.9	5.4	ns
		V_{CC} = 2.7 V	-	-	6.0	ns
t_{PLZ}	LOW to OFF-state propagation delay	$n\overline{OE}$ to nQn; see Fig. 5				
		V_{CC} = 3.3 V ± 0.3 V	1.5	3.4	4.6	ns
		V_{CC} = 2.7 V	-	-	5.0	ns
t_{su}	set-up time	nDn to nCP; HIGH or LOW; see Fig. 6				
		V_{CC} = 3.3 V ± 0.3 V	2.0	0.7	-	ns
		V_{CC} = 2.7 V	2.0	-	-	ns
t_h	hold time	nDn to nCP; HIGH or LOW; see Fig. 6				
		V_{CC} = 3.3 V ± 0.3 V	0.8	0	-	ns
		V_{CC} = 2.7 V	0.1	-	-	ns
t_W	pulse width	nCP HIGH; see Fig. 4				
		V_{CC} = 3.3 V ± 0.3 V	1.5	0.6	-	ns
		V_{CC} = 2.7 V	1.5	-	-	ns
		nCP LOW; see Fig. 4				
		V_{CC} = 3.3 V ± 0.3 V	3.0	1.6	-	ns
		V_{CC} = 2.7 V	3.0	-	-	ns

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

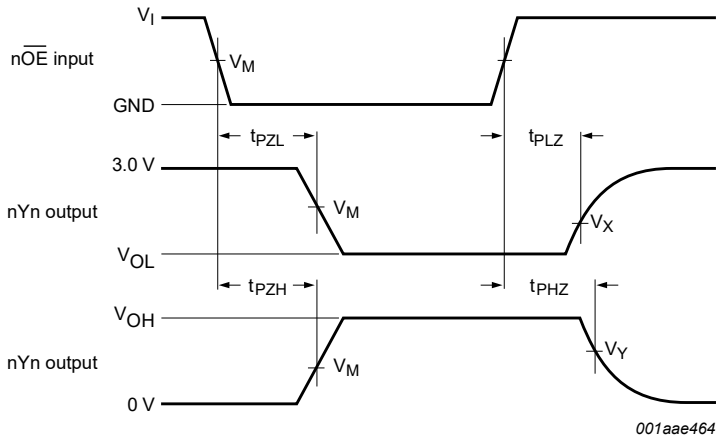
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

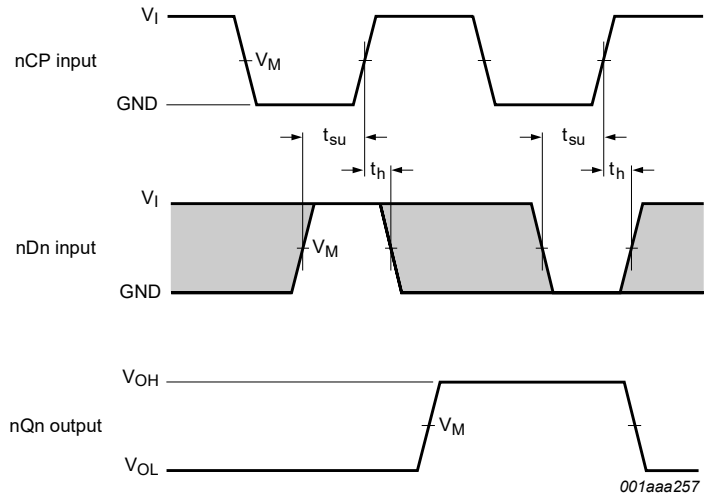
Fig. 4. Propagation delay clock input to output, clock pulse width and maximum clock frequency



Measurements points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. Enable and disable times



Measurement points are given in Table 8.

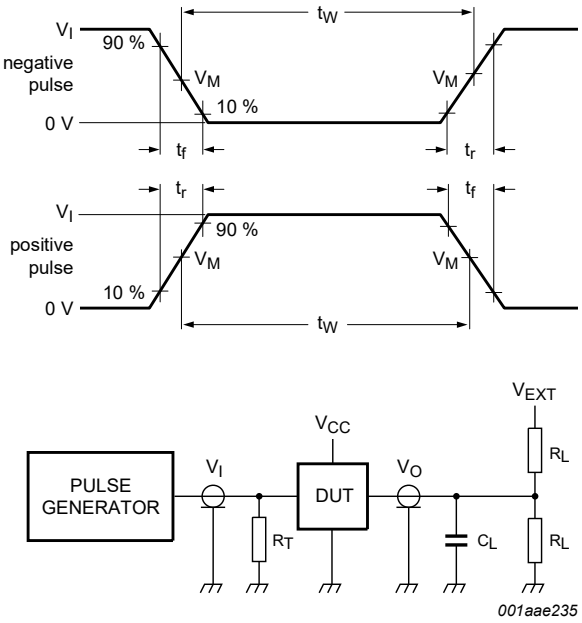
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 6. Data set-up and hold times

Table 8. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 9.

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

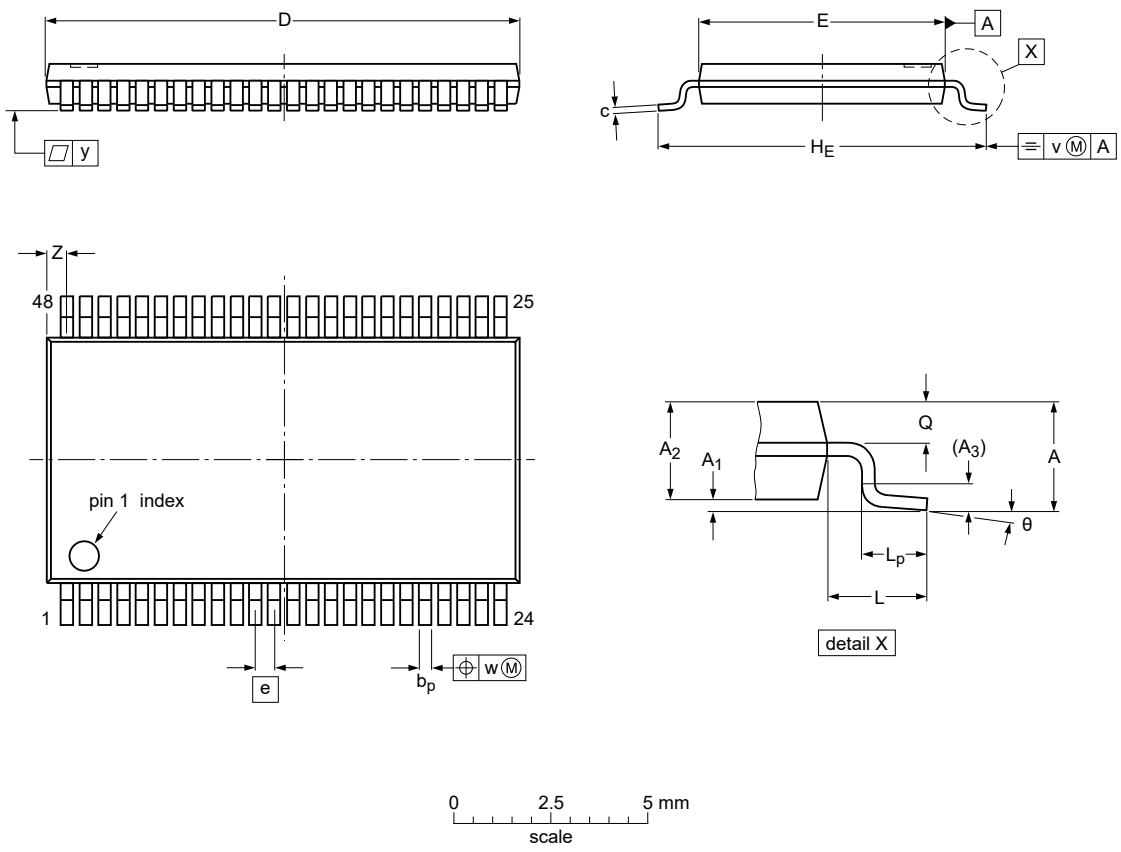
Fig. 7. Test circuit for measuring switching times

Table 9. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	GND	6 V	open

11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	max	1.2	0.15	1.05		0.28	0.2	12.6	6.2		8.3		0.8	0.50				0.8	8°
	nom				0.25					0.5		1			0.25	0.08	0.1		
	min		0.05	0.85		0.17	0.1	12.4	6.0		7.9		0.4	0.35				0.4	0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot362-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~13-08-05~~ 24-01-05

Fig. 8. Package outline SOT362-1 (TSSOP48)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT_LVTH16374A v.13	20240321	Product data sheet	-	74LVT_LVTH16374A v.12
Modifications:	• Fig. 8: Updated package outline drawing SOT362-1 (TSSOP48).			
74LVT_LVTH16374A v.12	20210806	Product data sheet	-	74LVT_LVTH16374A v.11
Modifications:	• Type number 74LVT16374ADL (SOT370-1/SSOP48) removed. • Section 1 and Section 2 updated. • Section 7: Derating value for P_{tot} total power dissipation removed.			
74LVT_LVTH16374A v.11	20190205	Product data sheet	-	74LVT_LVTH16374A v.10
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type numbers 74LVT16374AEV (SOT702-1) and 74LVTH16374ABX (SOT1134-2) removed. • Package outline drawing SOT362-1 (TSSOP48) updated.			
74LVT_LVTH16374A v.10	20120402	Product data sheet	-	74LVT_LVTH16374A v.9
Modifications:	• For type number 74LVTH16374ABX the sot code has changed to SOT1134-2.			
74LVT_LVTH16374A v.9	20111122	Product data sheet	-	74LVT_LVTH16374A v.8
Modifications:	• Legal pages updated.			
74LVT_LVTH16374A v.8	20110620	Product data sheet	-	74LVT_LVTH16374A v.7
74LVT_LVTH16374A v.7	20100322	Product data sheet	-	74LVT_LVTH16374A v.6
74LVT_LVTH16374A v.6	20100118	product data sheet	-	74LVT16374A v.5
74LVT16374A v.5	20040916	product data sheet	-	74LVT16374A v.4
74LVT16374A v.4	20021101	product specification	-	74LVT16374A v.3
74LVT16374A v.3	19991018	product specification	-	74LVT16374A v.2
74LVT16374A v.2	19980219	product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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