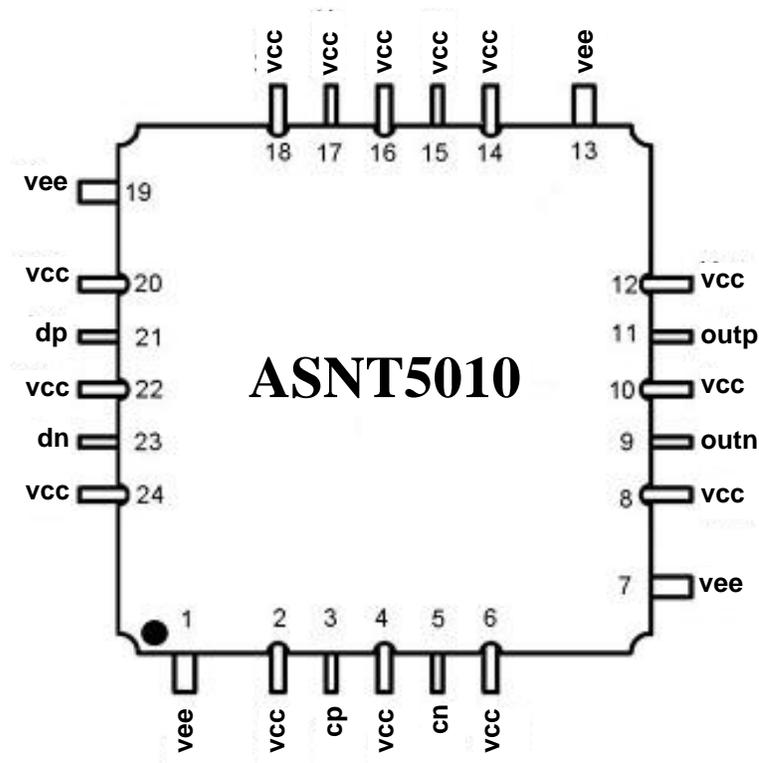




## ASNT5010-KMC DC-32Gbps D-Type Flip-Flop

- High speed broadband D-Type Flip-Flop for data retiming with full rate clock
- Exhibits low jitter and limited temperature variation over industrial temperature range
- 6.5ps set-up/hold time capability
- 87% clock phase margin for retiming of data input eye
- Fully differential CML input interfaces
- Fully differential CML output interface with 400mV single-ended swing
- Single +3.3V or -3.3V power supply
- Power consumption: 415mW
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 24-pin package



## DESCRIPTION

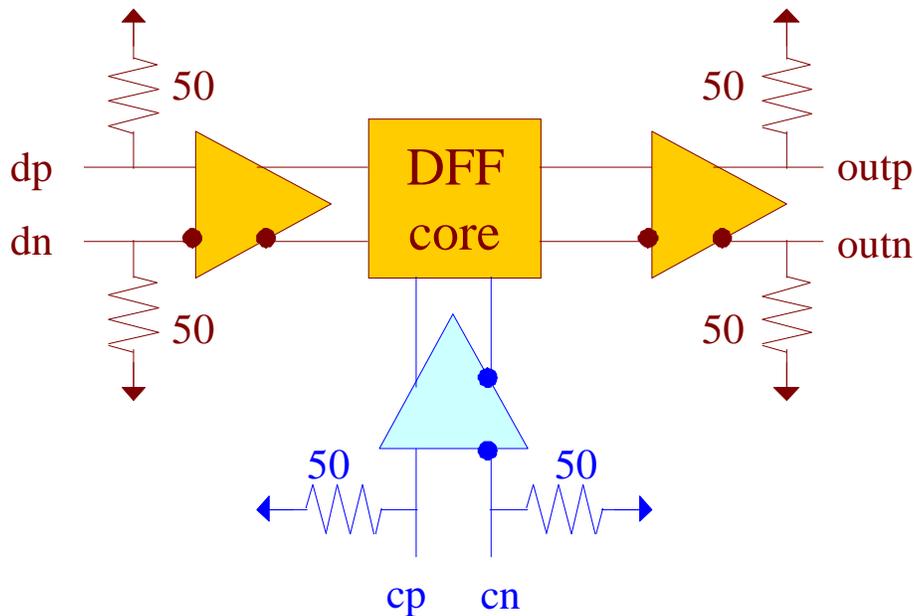


Fig. 1. Functional Block Diagram

The temperature stable ASNT5010-KMC SiGe IC provides broadband data retiming functionality and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can sample a high-speed data signal  $dp/dn$  with a full-rate external clock  $cp/cn$  to create a full-rate retimed NRZ data output  $outp/outn$ .

The part's I/O's support the CML logic interface with on chip  $50\Omega$  termination to  $vcc$  and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

## POWER SUPPLY CONFIGURATION

The part can operate with either negative supply ( $vcc = 0.0V = \text{ground}$  and  $vee = -3.3V$ ), or positive supply ( $vcc = +3.3V$  and  $vee = 0.0V = \text{ground}$ ). In case of the positive supply, all I/Os need AC termination when connected to any devices with  $50\Omega$  termination to ground. Different PCB layouts will be needed for each different power supply combination.



All the characteristics detailed below assume  $v_{cc} = 0.0V$  and  $v_{ee} = -3.3V$ .

## ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

| Parameter                   | Min | Max  | Units       |
|-----------------------------|-----|------|-------------|
| Supply Voltage ( $v_{ee}$ ) |     | -3.6 | V           |
| Power Consumption           |     | 0.46 | W           |
| RF Input Voltage Swing (SE) |     | 1.0  | V           |
| Case Temperature            |     | +90  | $^{\circ}C$ |
| Storage Temperature         | -40 | +100 | $^{\circ}C$ |
| Operational Humidity        | 10  | 98   | %           |
| Storage Humidity            | 10  | 98   | %           |

## TERMINAL FUNCTIONS

| TERMINAL                               |  |               | DESCRIPTION  |
|--|--|---------------|--|
| Name                                   | No.                                    | Type          |  |
| <b>High-Speed I/Os</b>                 |  |               |  |
| dp                                     | 21                                     | CML<br>input  | Differential data inputs with internal SE 50 $\Omega$ termination to $v_{cc}$  |
| dn                                     | 23                                     |               |  |
| cp                                     | 3                                      | CML<br>input  | Differential clock inputs with internal SE 50 $\Omega$ termination to $v_{cc}$   |
| cp                                     | 5                                      |               |  |
| outp                                   | 11                                     | CML<br>output | Differential data outputs with internal SE 50 $\Omega$ termination to $v_{cc}$ . Require external SE 50 $\Omega$ termination to $v_{cc}$ |
| outn                                   | 9                                      |               |  |
| <b>Supply and Termination Voltages</b> |  |               |  |
| Name                                   | Description                            |               | Pin Number   |
| vcc                                    | Positive power supply<br>(+3.3V or 0)  |               | 2, 4, 6, 8, 10, 12, 14, 15, 16, 17, 18, 20, 22, 24   |
| vee                                    | Negative power supply<br>(0V or -3.3V) |               | 1, 7, 13, 19   |



## ELECTRICAL CHARACTERISTICS

| PARAMETER                         | MIN                  | TYP                  | MAX             | UNIT | COMMENTS                          |
|-----------------------------------|----------------------|----------------------|-----------------|------|-----------------------------------|
| <b>General Parameters</b>         |                      |                      |                 |      |                                   |
| v <sub>ee</sub>                   | -3.1                 | -3.3                 | -3.5            | V    | ±6%                               |
| v <sub>cc</sub>                   |                      | 0.0                  |                 | V    | External ground                   |
| I <sub>vee</sub>                  |                      | 125                  |                 | mA   |                                   |
| Power consumption                 |                      | 415                  |                 | mW   |                                   |
| Junction temperature              | -40                  | 25                   | 125             | °C   |                                   |
| <b>HS Input Data (dp/dn)</b>      |                      |                      |                 |      |                                   |
| Data rate                         | DC                   |                      | 32              | Gbps |                                   |
| Swing                             | 0.05                 |                      | 0.8             | V    | Differential or SE, p-p           |
| CM Voltage Level                  | v <sub>cc</sub> -0.8 |                      | v <sub>cc</sub> | V    | Must match for both inputs        |
| Setup/Hold time                   |                      | 6.5                  |                 | ps   |                                   |
| <b>HS Input Clock (cp/cn)</b>     |                      |                      |                 |      |                                   |
| Frequency                         | DC                   |                      | 32              | GHz  |                                   |
| Swing                             | 0.05                 |                      | 0.8             | V    | Differential or SE, p-p           |
| CM Voltage Level                  | v <sub>cc</sub> -0.8 |                      | v <sub>cc</sub> | V    | Must match for both inputs        |
| Clock Phase Margin                | 85                   | 87                   | 89              | %    |                                   |
| <b>HS Output Data (outp/outn)</b> |                      |                      |                 |      |                                   |
| Data rate                         | DC                   |                      | 32              | Gbps |                                   |
| Latency                           |                      | 67                   |                 | ps   | From Clock input to Data output   |
| Logic "1" level                   |                      | v <sub>cc</sub>      |                 | V    |                                   |
| Logic "0" level                   |                      | v <sub>cc</sub> -0.4 |                 | V    | With external 50Ωm DC termination |
| Clock-to-output delay             | 55                   | 65                   | 75              | ps   |                                   |
| Rise/Fall times                   |                      |                      | 13              | ps   | 20%-80%                           |
| Output Jitter                     |                      |                      | 4               | ps   | Peak-to-peak                      |

## PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFP package shown in Fig. 2. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the v<sub>cc</sub> plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT5010-KMC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

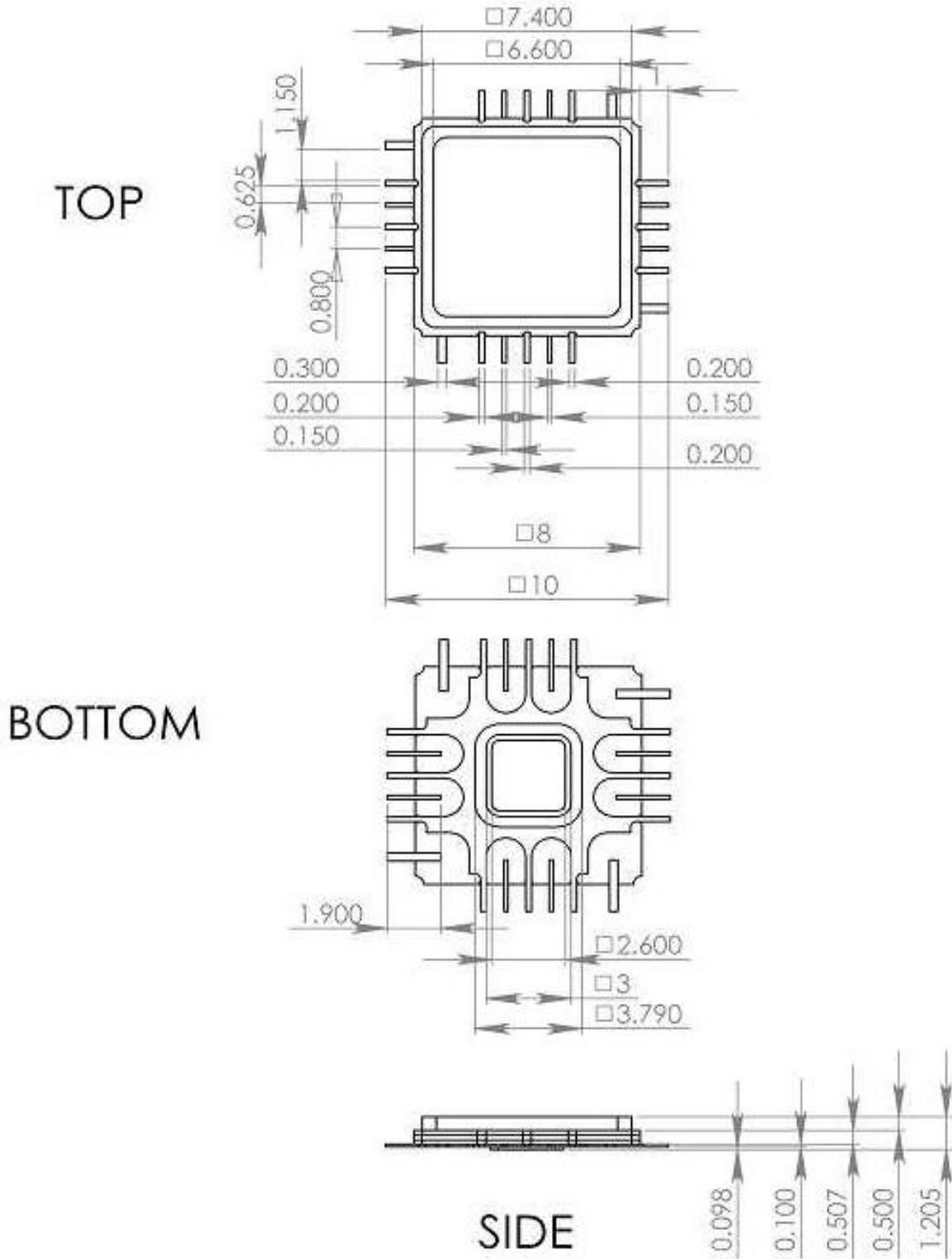


Fig. 2. CQFP 24-Pin Package Drawing (All Dimensions in mm)



## REVISION HISTORY

| Revision | Date    | Changes   |
|----------|---------|---|
| 2.7.2    | 02-2020 | Updated Package Information   |
| 2.6.2    | 07-2019 | Updated Letterhead  |
| 2.6.1    | 02-2019 | Added setup/hold time to Electrical Characteristics table   |
| 2.5.1    | 08-2018 | Corrected latency specifications  |
| 2.4.1    | 08-2018 | Added latency specifications  |
| 2.3.1    | 06-2018 | Updated electrical characteristics  |
| 2.2.1    | 06-2018 | Updated electrical characteristics<br>Updated package information   |
| 2.1.1    | 02-2013 | Revised title<br>Revised package information  |
| 2.0.1    | 01-2013 | Revised title<br>Added package pin out drawing<br>Revised functional block diagram<br>Added power supply configuration<br>Added absolute maximum ratings<br>Revised terminal functions<br>Revised electrical characteristics<br>Added package information and mechanical drawing<br>Format correction |
| 1.0      | 02-2008 | First release   |