15.1 GHz to 32 GHz, Tunable Band-Pass Filter

Data Sheet

ADMV8432

FEATURES

Amplitude settling time: 200 ns typical
Wideband rejection: ≥30 dB
Single chip implementation
40-lead, 6 mm × 6 mm, RoHS compliant LFCSP

APPLICATIONS

Test and measurement equipment
Military radar and electronic warfare (EW) systems
Video satellite (VSAT) communications

FUNCTIONAL BLOCK DIAGRAM

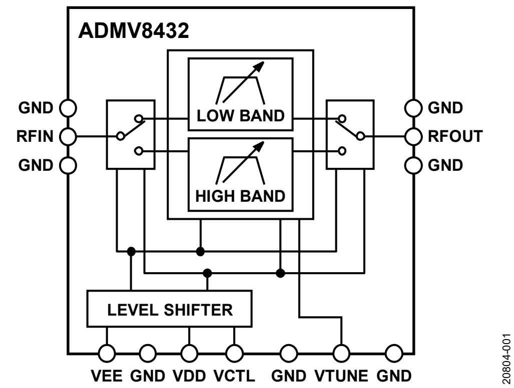

Figure 1.

GENERAL DESCRIPTION

The ADMV8432 is a monolithic microwave integrated circuit (MMIC), tunable band-pass filter that features a user selectable pass-band frequency. The 3 dB filter bandwidth is >17% of the center frequency (f_{CENTER}). Additionally, f_{CENTER} can be varied between 16.6 GHz to 30.1 GHz by applying an analog tuning voltage between 0 V to 15 V. The usable pass band corner frequencies (f_{CORNER}) span from 15.1 GHz to 32 GHz. This tunable filter can be used as a much smaller alternative to physically large switched filter banks and cavity tuned filters. This tunable filter has excellent microphonics due to the monolithic design and provides a dynamically adjustable solution in advanced communications applications.

Rev. A **Document Feedback**

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Tel: 781.329.4700

Technical Support **www.analog.com**

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REVISION HISTORY

3/2021—Rev. 0 to Rev. A

7/2019—Revision 0: Initial Version

SPECIFICATIONS

HIGH BAND SPECIFICATIONS

T_A = 25°C, VDD = 5 V, VEE = −5 V, and VCTL = 0 V, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE					
f_{CENTER}	25.7		30.1	GHz	
3 dB f_{CORNER}	23.7		32	GHz	
3 dB Filter Bandwidth		17		%	
REJECTION					
Low-Side		0.75 × f_{CENTER}		GHz	≥30 dB
High-Side		1.25 × f_{CENTER}		GHz	≥30 dB
Re-Entry		>40		GHz	≤30 dB
LOSS					
Insertion Loss		9		dB	
Return Loss		15		dB	
DYNAMIC PERFORMANCE					
Input Third-Order Intercept (IP3)		37		dBm	
Input Power at 5° Shift in Insertion Phase		19		dBm	VTUNE = 0 V
Group Delay Flatness		0.1		ns	VTUNE = 0 V
Phase Sensitivity		0.6		Rad/V	
Amplitude Settling		200		ns	Time to settle to minimum insertion loss, within ≤0.5 dB of static insertion loss
Drift Rate		−2.7		MHz/°C	
Tuning Sensitivity		580		MHz/V	
RESIDUAL PHASE NOISE					
1 MHz Offset		−162		dBc/Hz	

LOW BAND SPECIFICATIONS

T_A = 25°C, VDD = 5 V, VEE = −5 V, and VCTL = 2.5 V, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE					
f_{CENTER}	16.6		22.5	GHz	
3 dB f_{CORNER}	15.1		24.5	GHz	
3 dB Filter Bandwidth		18		%	
REJECTION					
Low-Side		0.72 × f_{CENTER}		GHz	≥30 dB
High-Side		1.21 × f_{CENTER}		GHz	≥30 dB
Re-Entry		>40		GHz	≤30 dB
LOSS					
Insertion Loss		8		dB	
Return Loss		10		dB	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					
Input IP3		34		dBm	
Input Power at 5° Shift in Insertion Phase		20		dBm	VTUNE = 0 V
Group Delay Flatness		0.15		ns	VTUNE = 0 V
Phase Sensitivity		0.8		Rad/V	
Amplitude Settling		200		ns	Time to settle to minimum insertion loss, within ≤0.5 dB of static insertion loss
Drift Rate		−1.4		MHz/°C	
Tuning Sensitivity		530		MHz/V	
RESIDUAL PHASE NOISE					
1 MHz Offset		−163		dBc/Hz	

DC CHARACTERISTICS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
f_{CENTER} TUNING					
Voltage (VTUNE)	0		15	V	
Current (I_{TUNE})			±1	μA	
BAND CONTROL VOLTAGE (VCTL)					
Input Voltage					
Low	0		0.8	V	0 V for high band select
High	2	2.5	3	V	2.5 V for low band select
Current			1	μA	
SUPPLY VOLTAGES					
Negative (VEE)	−5.5	−5		V	
Positive (VDD)		5	5.5	V	
SUPPLY CURRENTS					
Negative (I_{EE})		0.7		mA	
Positive (I_{DD})			1	mA	

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Tuning	
VTUNE	−0.5 V to +15.5 V
I_{TUNE}	±1 µA
Supply Voltages	
VEE	−5.6 V
VDD	5.6 V
VCTL	−0.5 V to VDD + 0.5 V
RF Input Power	
2 GHz to 50 GHz	27 dBm
0.5 GHz to 2 GHz	19 dBm
0.1 GHz to 0.5 GHz	6 dBm
Hot Switch Input Power	
2 GHz to 50 GHz	24 dBm
0.5 GHz to 2 GHz	16 dBm
0.1 GHz to 0.5 GHz	3 dBm
Temperature	
Operating	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Junction for 1 Million Mean Times Between Failures (MTTF)	150°C
Nominal Junction (T_{PADDLE} = 85°C, Input Power (P_{IN}) = 23 dBm)	150°C
Electrostatic Discharge (ESD) Rating	
Human Body Model (HBM)	250 V
Field Induced Charged Device Model (FICDM)	1250 V
Moisture Sensitivity Level (MSL) Rating	MSL3

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

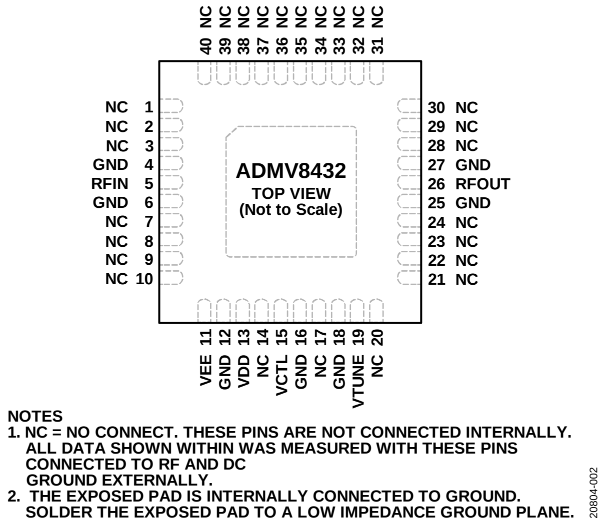

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 3, 7 to 10, 14, 17, 20 to 24, 28 to 40	NC	No Connect. These pins are not connected internally. All data shown within was measured with these pins connected to RF and dc ground externally.
4, 6, 12, 16, 18, 25, 27	GND	Ground. These pins must be connected to RF and dc ground.
5	RFIN	RF Input. This pin is dc-coupled and matched to 50 Ω. Blocking capacitors are required if the RF line potential is not equal to 0 V.
11	VEE	Negative Supply Voltage. VEE is −5 V.
13	VDD	Positive Supply Voltage. VDD is 5 V.
15	VCTL	Control Voltage for Band Selection. The device is in the high band when the voltage is 0 V and in the low band when the voltage is 2.5 V.
19	VTUNE	Center Frequency Control Voltage of the Band-Pass Filter. VTUNE can be varied from 0 V to 15 V.
26	RFOUT	RF Output. This pin is dc-coupled and matched to 50 Ω. Blocking capacitors are required if the RF line potential is not equal to 0 V.
	EPAD	Exposed Pad. The exposed pad is internally connected to ground. Solder the exposed pad to a low impedance ground plane.

INTERFACE SCHEMATICS

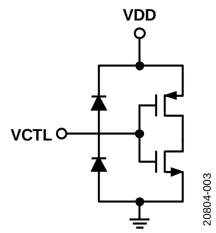

Figure 3. VCTL and VDD Interface Schematic

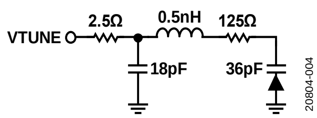

Figure 4. VTUNE Interface Schematic

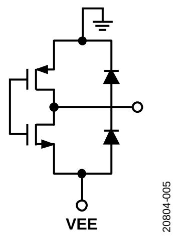

Figure 5. VEE Interface Schematic

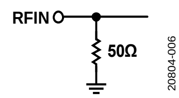

Figure 6. RFIN Interface Schematic

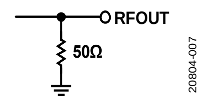

Figure 7. RFOUT Interface Schematic

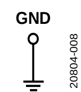

Figure 8. GND Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

HIGH BAND

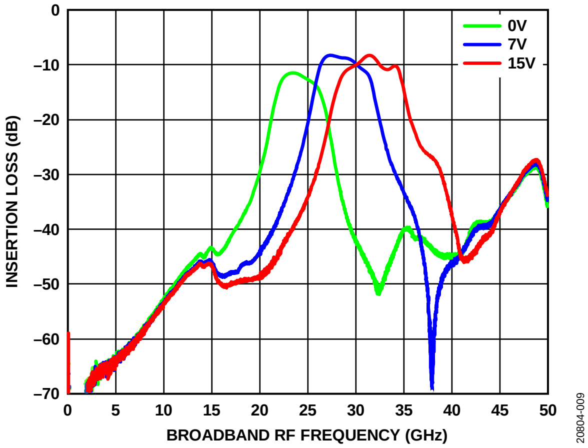

Figure 9. Insertion Loss vs. Broadband RF Frequency at Various VTUNE Voltages

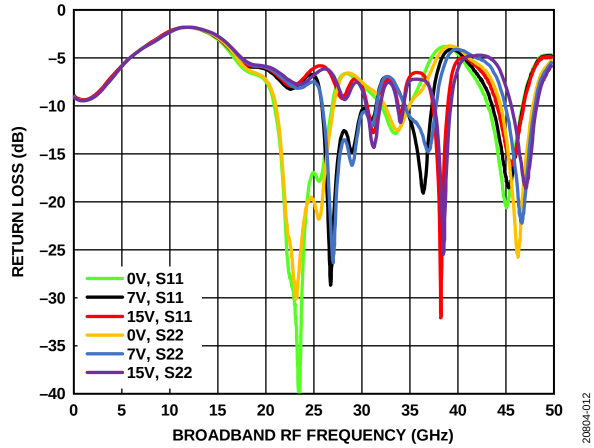

Figure 12. Return Loss vs. Broadband RF Frequency at Various Voltages

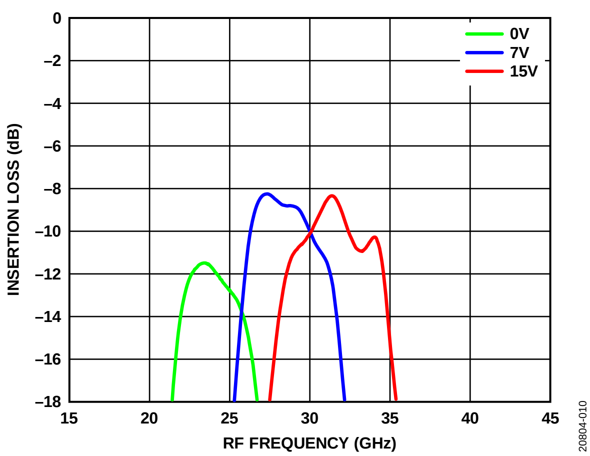

Figure 10. Insertion Loss vs. RF Frequency at Various Voltages

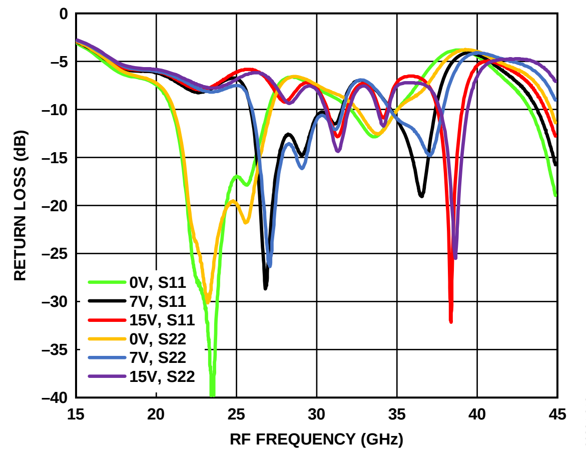

Figure 13. Return Loss vs. RF Frequency at Various Voltages

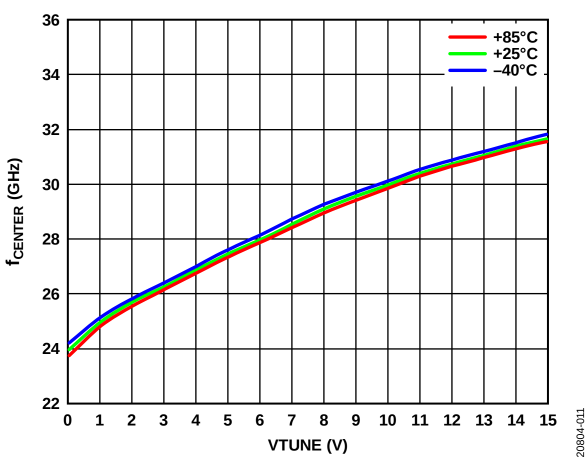

Figure 11. f_{CENTER} vs. VTUNE at Various Temperatures

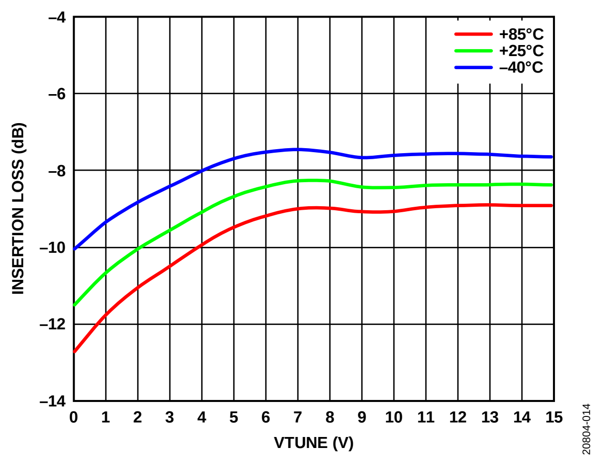

Figure 14. Insertion Loss vs. VTUNE at Various Temperatures

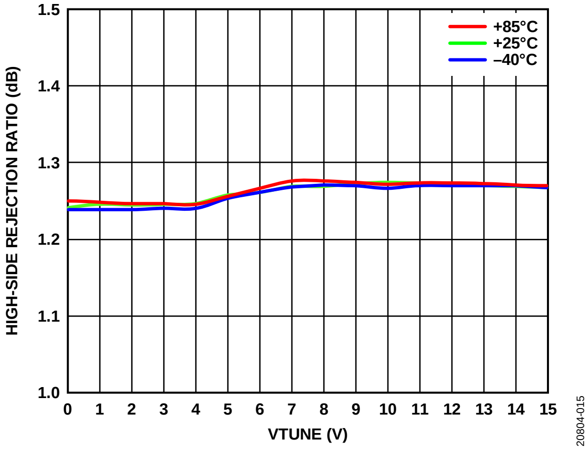

Figure 15. High-Side Rejection vs. VTUNE at Various Temperatures

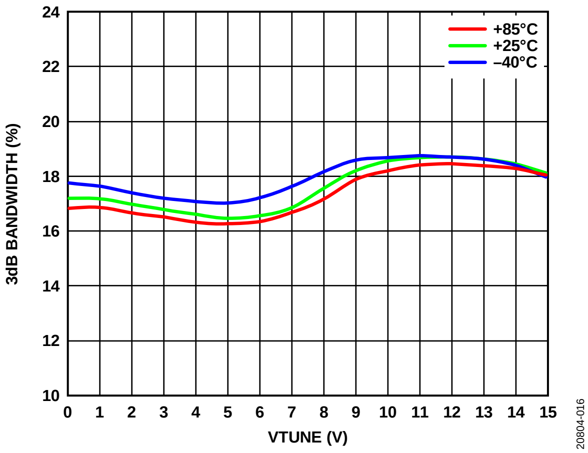

Figure 16. 3 dB Bandwidth vs. VTUNE at Various Temperatures

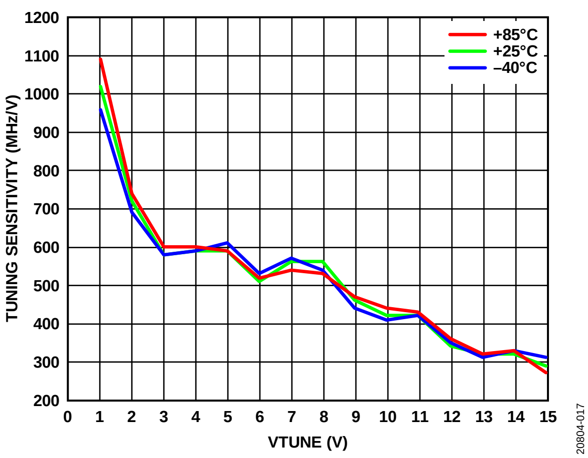

Figure 17. Tuning Sensitivity vs. VTUNE at Various Temperatures

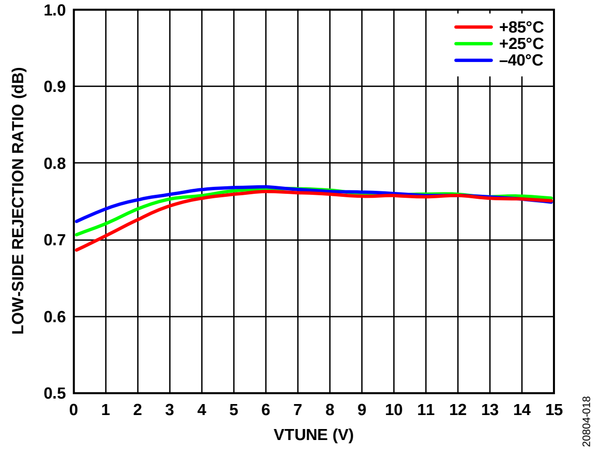

Figure 18. Low-Side Rejection vs. VTUNE at Various Temperatures

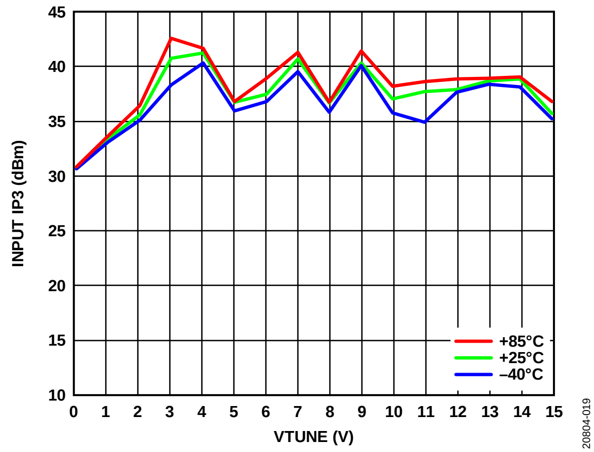

Figure 19. Input IP3 vs. VTUNE at Various Temperatures

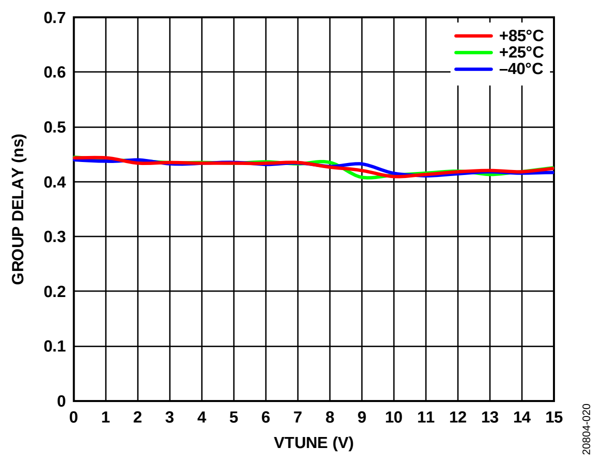

Figure 20. Group Delay vs. VTUNE at Various Temperatures

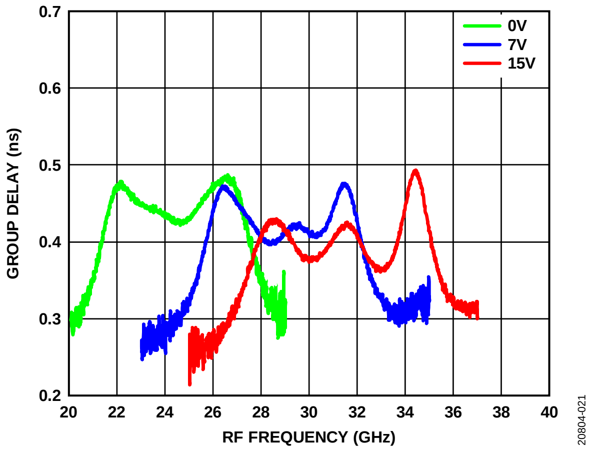

Figure 21. Group Delay vs. RF Frequency at Various VTUNE Voltages

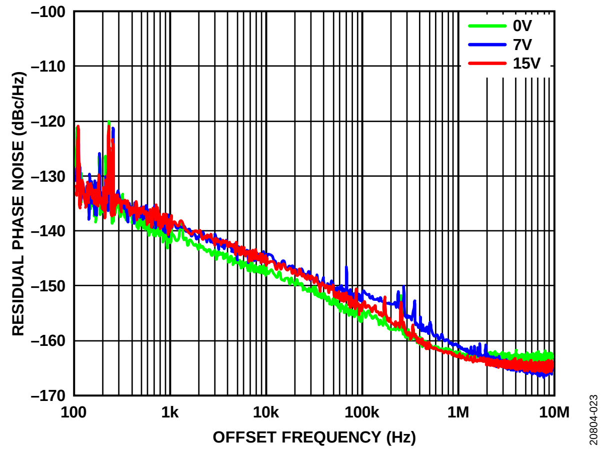

Figure 23. Residual Phase Noise vs. Offset Frequency at Various VTUNE Voltages

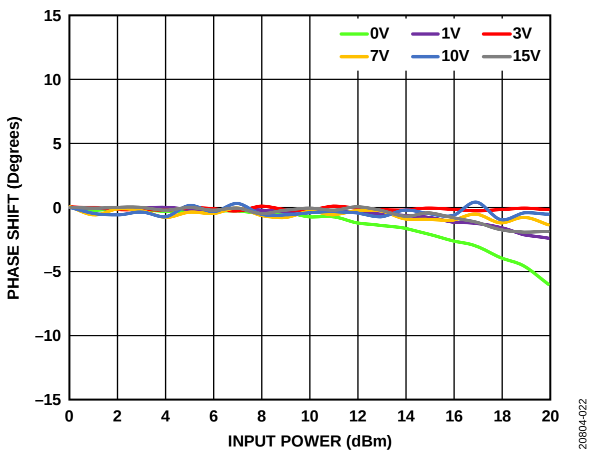

Figure 22. Phase Shift vs. Input Power at Various VTUNE Voltages

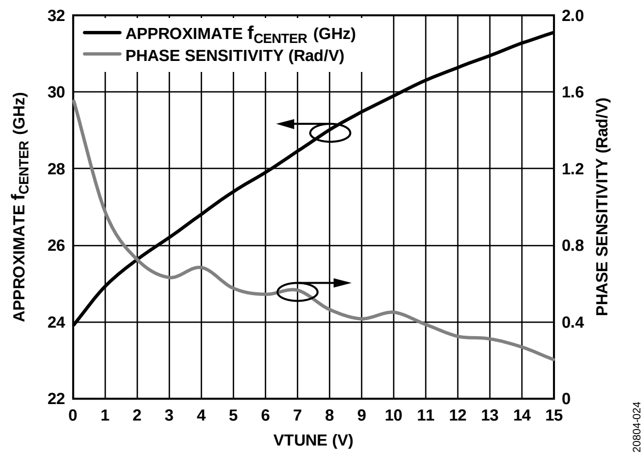

Figure 24. Approximate f_{CENTER} and Phase Sensitivity vs. VTUNE

LOW BAND

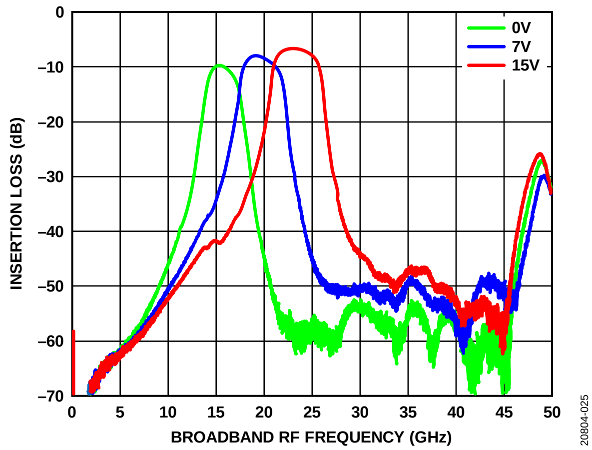

Figure 25. Insertion Loss vs. Broadband RF Frequency for Various VTUNE Voltages

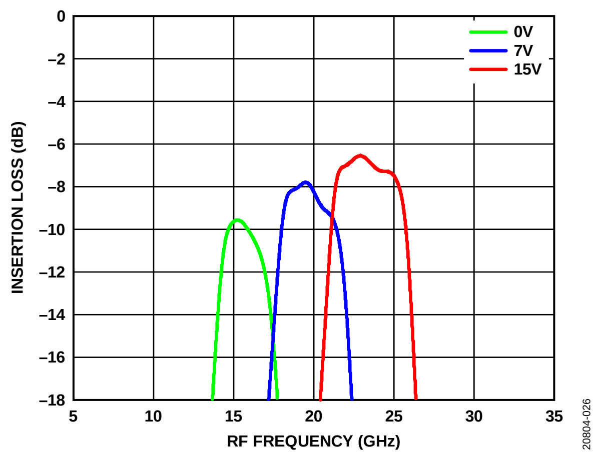

Figure 26. Insertion Loss vs. RF Frequency for Various VTUNE Voltages

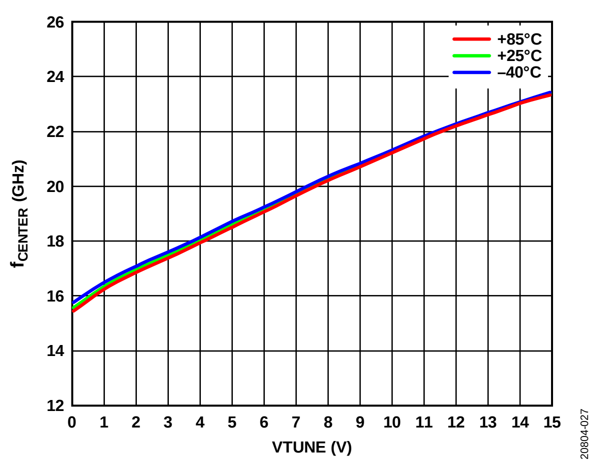

Figure 27. f_{CENTER} vs. VTUNE at Various Temperatures

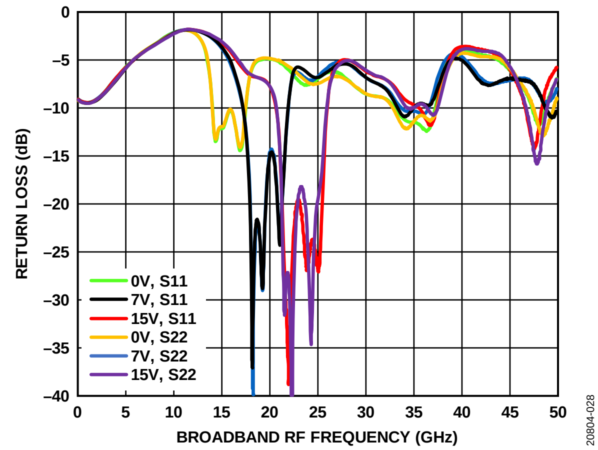

Figure 28. Return Loss vs. Broadband RF Frequency for Various VTUNE Voltages

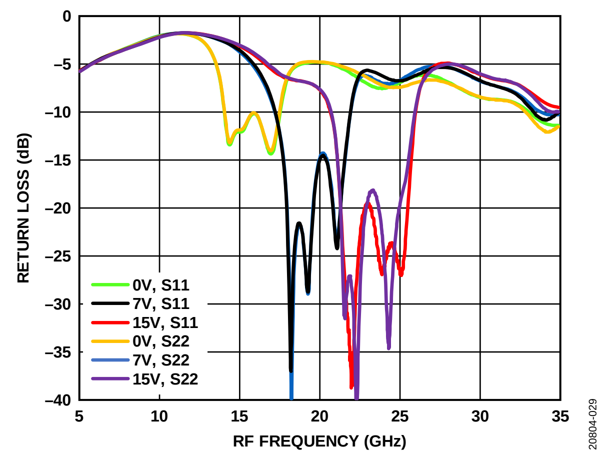

Figure 29. Return Loss vs. RF Frequency for Various VTUNE Voltages

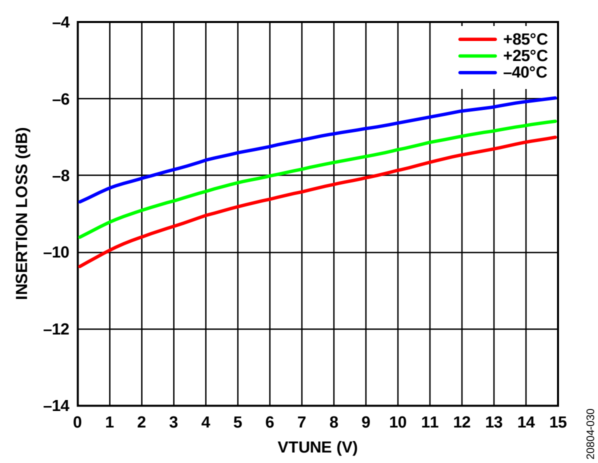

Figure 30. Insertion Loss vs. VTUNE at Various Temperatures

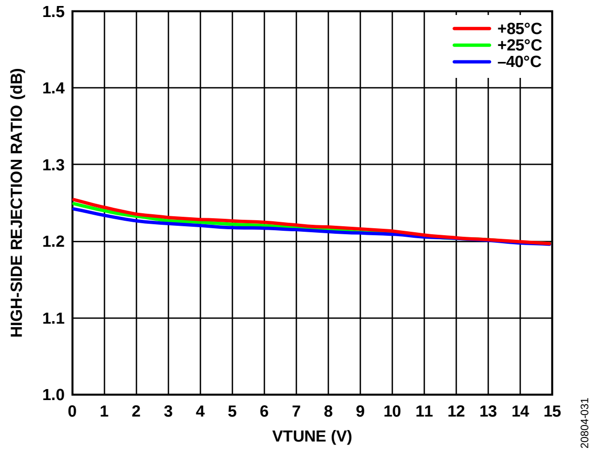

Figure 31. High-Side Rejection vs. VTUNE at Various Temperatures

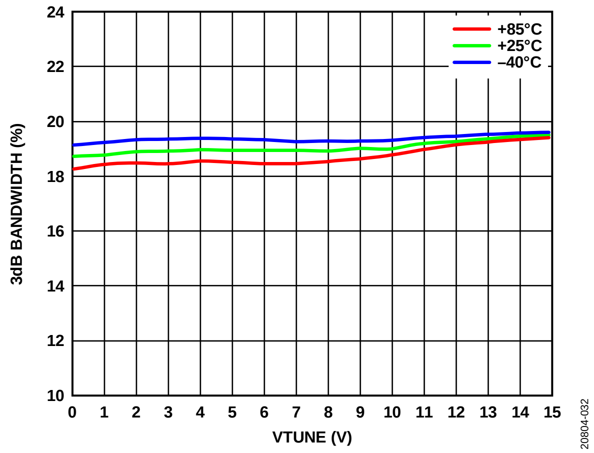

Figure 32. 3 dB Bandwidth vs. VTUNE at Various Temperatures

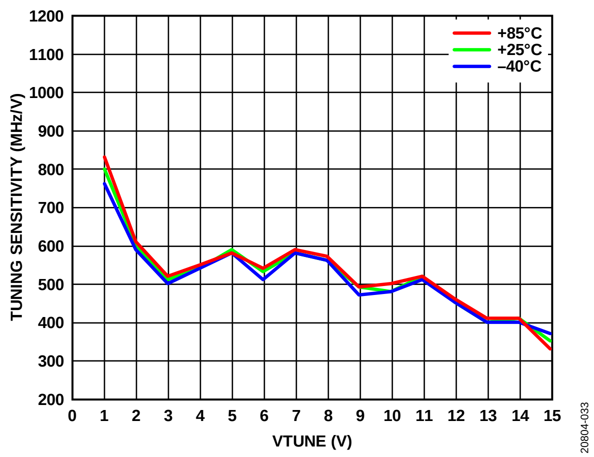

Figure 33. Tuning Sensitivity vs. VTUNE at Various Temperatures

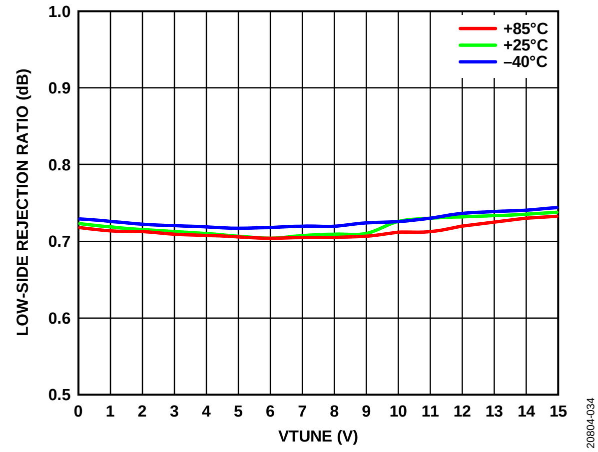

Figure 34. Low-Side Rejection vs. VTUNE at Various Temperatures

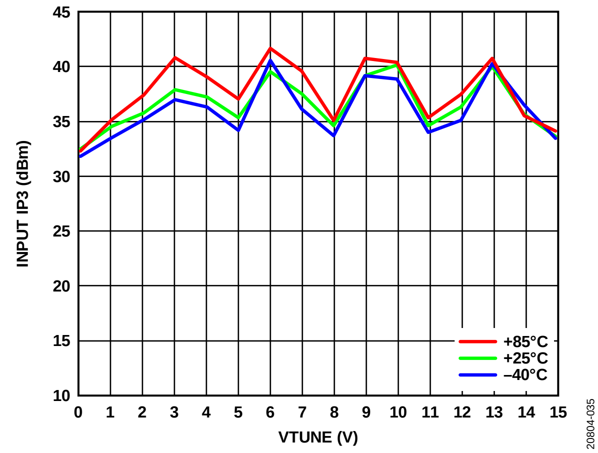

Figure 35. Input IP3 vs. VTUNE at Various Temperatures

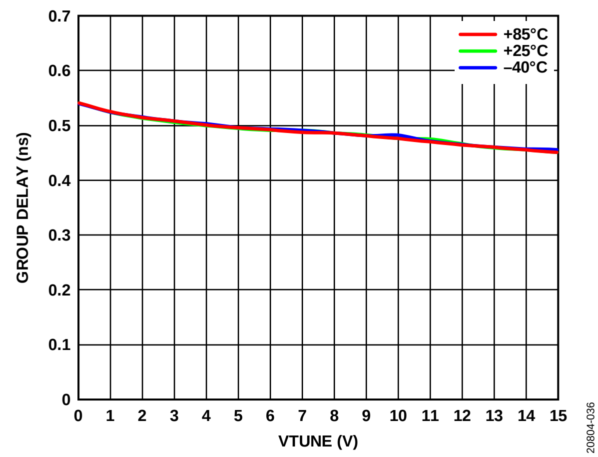

Figure 36. Group Delay vs. VTUNE at Various Temperatures

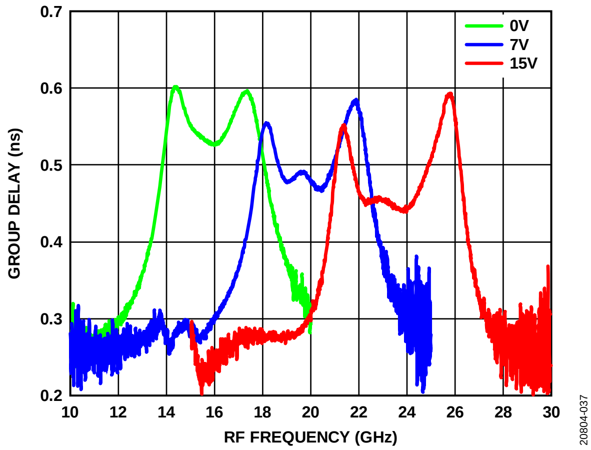

Figure 37. Group Delay vs. RF Frequency at Various VTUNE Voltages

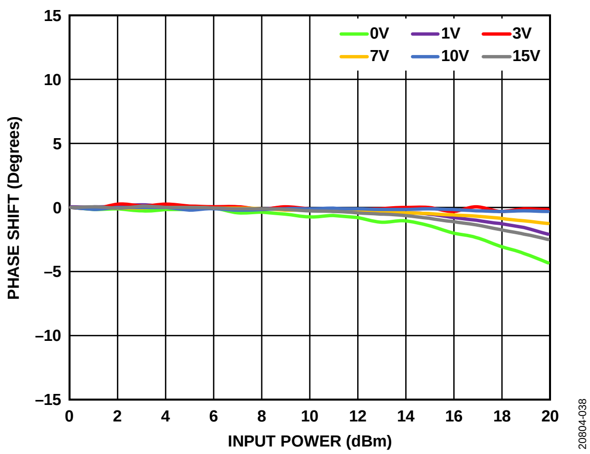

Figure 38. Phase Shift vs. Input Power at Various VTUNE Voltages

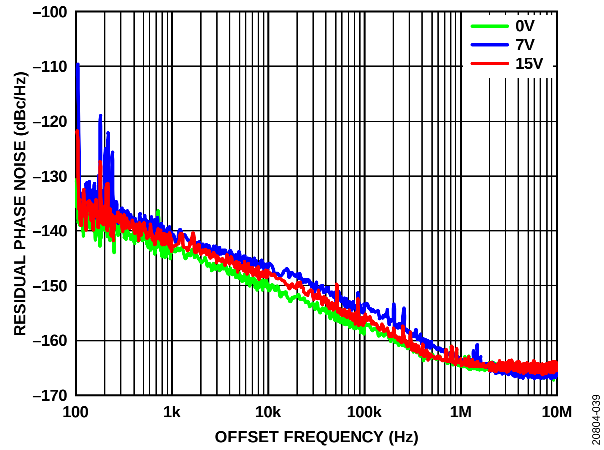

Figure 39. Residual Phase Noise vs. Offset Frequency at Various VTUNE Voltages

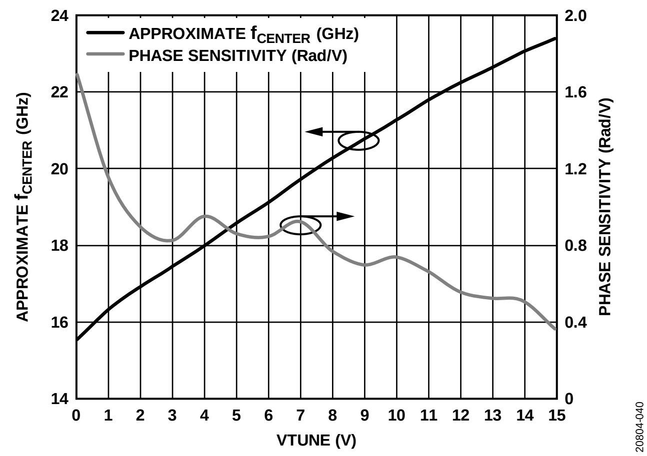

Figure 40. Approximate f_{CENTER} and Phase Sensitivity vs. VTUNE

HIGH BAND AND LOW BAND

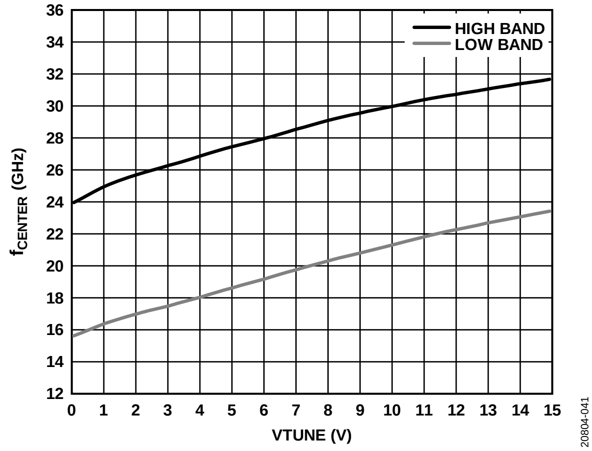

Figure 41. f_{CENTER} vs. VTUNE

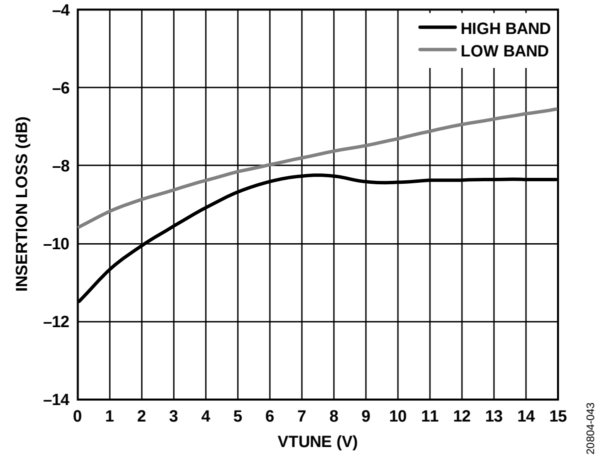

Figure 43. Insertion Loss vs. VTUNE

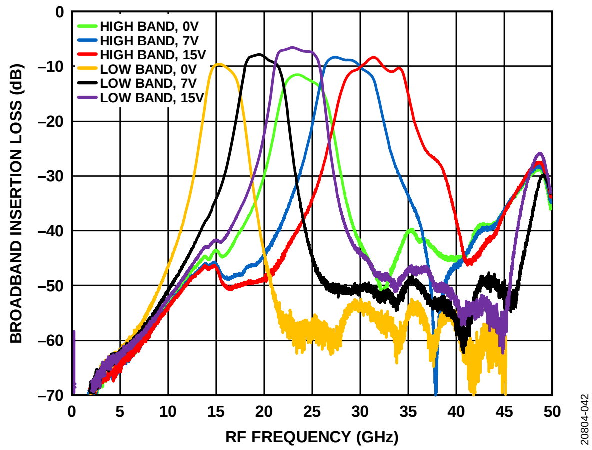

Figure 42. Broadband Insertion Loss vs. RF Frequency

THEORY OF OPERATION

The ADMV8432 is a MMIC, band-pass filter that features a user selectable pass-band frequency. To select the high band, apply 0 V at VCTL, and to select the low band, apply 2.5 V at VCTL. Varying the applied analog tuning voltage between 0 V and 15 V at VTUNE varies the f_{CENTER} from 16.6 GHz to 22.5 GHz for the low band and from 25.7 GHz to 30.1 GHz for the high band.

APPLICATIONS INFORMATION

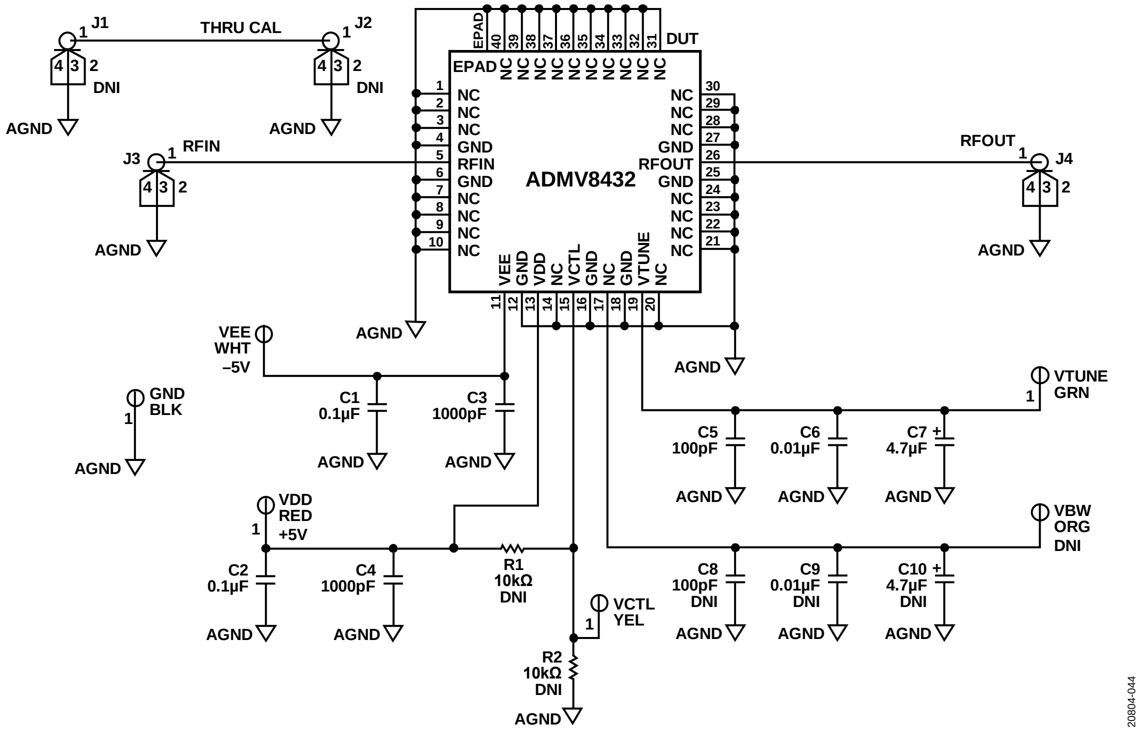

Figure 44. Typical Application Circuit

TYPICAL APPLICATION CIRCUIT

Figure 44 shows the typical application circuit for the ADMV8432.

POWER SUPPLY SEQUENCE

The required power-up sequence is GND, VDD, VEE, VCTL, and VTUNE. Deviations from this sequence may forward bias the ESD protection structures and damage them.

OUTLINE DIMENSIONS

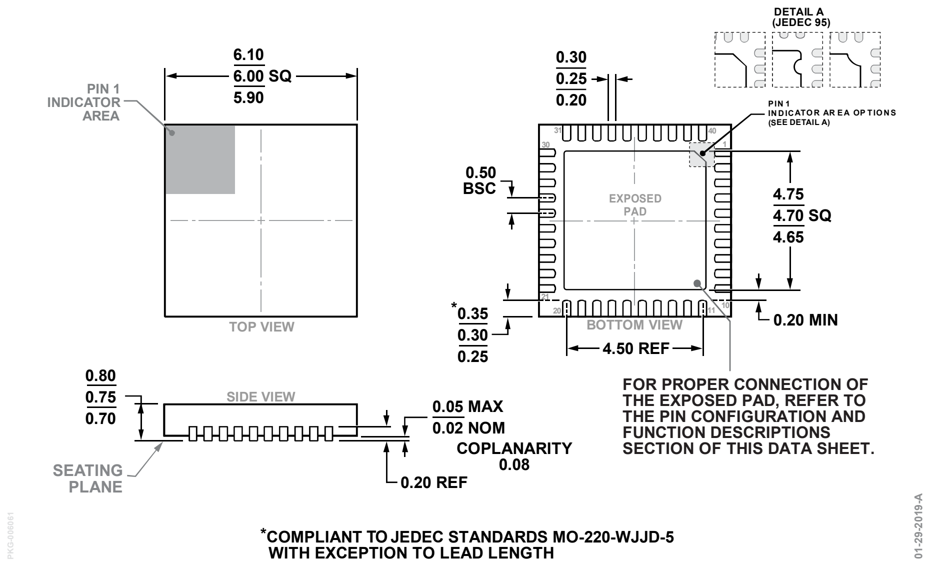

Figure 45. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.75 mm Package Height
(CP-40-27)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADMV8432ACPZ	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-27
ADMV8432ACPZ-R5	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-27
ADMV8432-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.