OSFP 800G Closed Top ELB Module (Straight-mapping)

0-Watt

30-Watt

Features

- OSFP Comply to OSFP Type2 Flat Top style
- Industry's highest rated mating cycles for 2000 and above
- Built-in surge current mitigation technology
- Adjustable total power consumption up to 30W distributed to the 4 regions, each region is individually
- Operating temperature: 0℃ to 85℃
- +3.3V power supply
- Supports 8*10G/25G/56G PAM4/112G PAM4 data rates
- 2-wire interface for integrated Digital Diagnostic Monitoring
- Signal integrity performance meets IEEE 802.3ba, 802.3bj, 802.3cd , 802.3ck standards respectively
- Enhanced heat dissipation technology for high power testing
- Custom EEPROM available
- A multi-color LED indicator for module states
- Hot-pluggable
- RoHS 2.0 compliant

Application

- OSFP port/system testing
- Ethernet IEEE 802.3 (Gigabit, 10~800 Gigabit Ethernet)
- SONET, SDH, GBE, Fiber Channel Support

Standard

- Common Management Interface Specification, Rev 4.0
- SFF-8024, SFF Cross Reference to Industry Products, Rev 4.7
- OSFP Octal Small Form Factor Pluggable Module, Rev 4.09
- EIA 364 Series
- IEEE 803.2bm
- IEEE 803.2bj
- IEEE 802.3cd
- IEEE802.3bs
- IEEE 802.3ck

Description

Designed and engineered to accommodate customers high usage 2000 cycles at 0°C to 85°C, the loopback module series are the most reliable products in the market to enable the quickest customers systems production and deployment. Software defined multiple power consumption may emulate the optical module power, and the embedded insertion loss characteristics emulates the real-world cabling for 100G/400G/800G Ethernet/Infiniband/FC. The built-in surge current mitigation technology mitigates the DUT risks from being damaged. The broad operating temperature range accommodates the enterprise, datacom and telecom applications. The loopback module may be used for ports testing, field deployment testing and equipment troubleshooting.

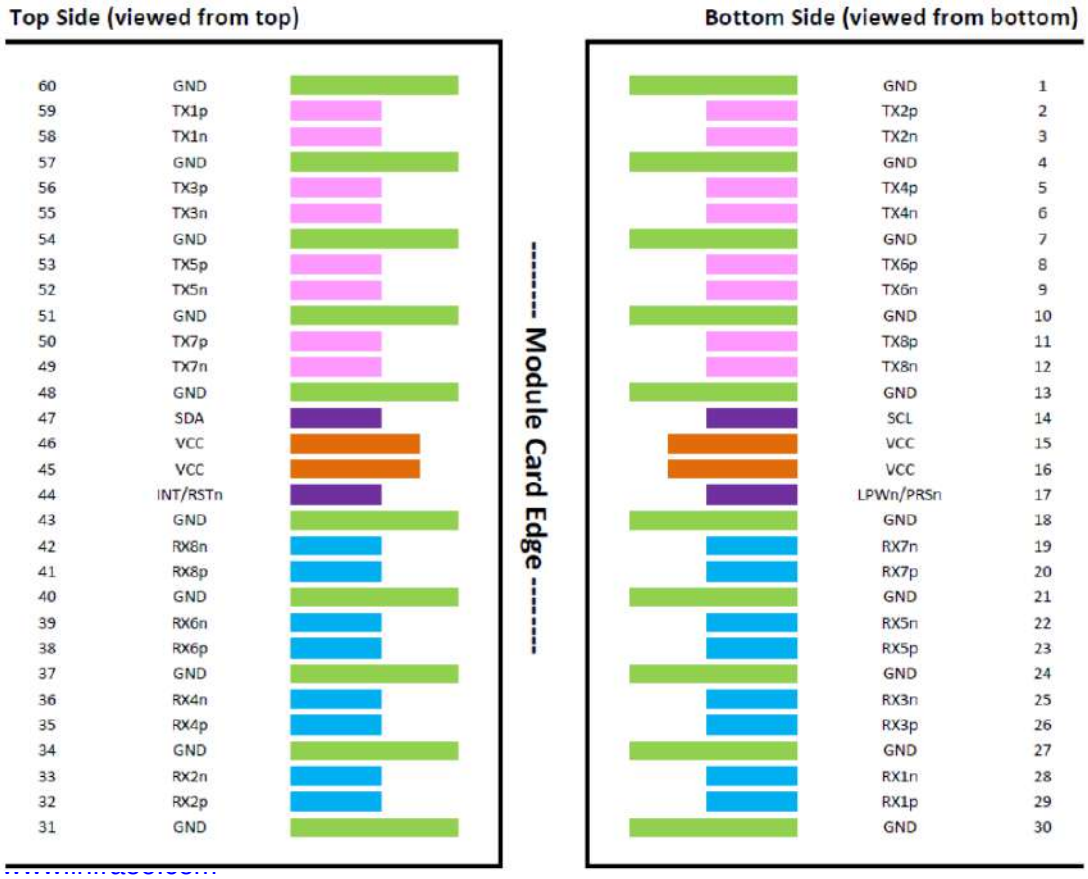
Specification

Absolute Maximum Ratings				
Parameter	**Symbol**	**Min**	**Max**	**Unit**
Storage Temperature	Ts	-40	+85	℃
Ambient Operating Temperature	Ta	0	+85	℃
Storage Relative Humidity	RH_S	0	95	%
Operating Relative Humidity	RH_O	0	85	%
Power Supply Voltage	Vcc	2.97	+3.63	V

Recommended Operating Conditions					
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**
Ambient Operating Temperature	Ta	0	-	+85	℃
Power Supply Voltage	V_{CC}	2.97	3.3	3.63	V
Data Rate	BRate	0.1	-	800	Gbps
Durability Cycles		-	2000	2250	Cycles

High Speed Characteristics						
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**	**Notes**
Input/Output Impedance	Zdiff	85	95	115	Ohm	Differential Impedance
Return Loss	SDD11/22	<-10 <-5	0.01GHz ≤ f < 10GHz 10GHz≤ f < 40GHz		dB	
Insertion Loss @26.56GHz	SDD21	-	-	7 (Include Trace&Via&Mating& Connectors， Without MCB insertion loss) 11.75 (Include MCB insertion loss&Trace&Via& Mating&Connectors)	dB	The insertion loss for TX to RX, including the AC Caps, as measured with MCB,The MCB insertion loss comply with IEEE 802.3ck CL 162B.1.2.1

Pin Definition



Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

Nomenclature on lanes

The 16 lanes are connected as following with match polarity:

- TX1 and RX1
- TX2 and RX2
- TX3 and RX3
- TX4 and RX4
- TX5 and RX5
- TX6 and RX6
- TX7 and RX7
- TX8 and RX8

Status LED

A multi-color LED would be viewed from the front of the module in order to signify module states

Power-up-reset or Soft-reset:

STP1:Illuminate RED LED

STP2:Continuous illuminate Red LED if the voltage on LPWn/PRSn is below 0.3V

STP3: Once the LPWn/PRSn is above 0.3V, illuminate Green LED, and Start the Normal operation.

Normal operation:

Solid green: low-power mode

Solid red: high-power mode

Blinking green: low-power mode with any of the interrupt flag is set

Blinking red: high-power mode with any of the interrupt flag is set

I2C interface

I2C management interface shall conform to the CMIS 4.0.

Upon the completion of the MgmtInit state, the I2C interface on the module must support Fast-mode as defined in the UM10204, I2C-bus specification and user manual, Rev. 6 – 4 April 2014 in order to handle the SCL clock frequency between 0kHz and 400KHz. In addition, the module may only clock stretching the SCL less than 100 μsec in any frequency.

NVRAM

A 128-byte NVRAM be accessed through I2C:
The NVRAM be located at page 0x03 address 127 through address 255.
The NVRAM support Current Address Read Operation, Random Read Operation , Sequential Bytes Read Operation, Byte Write Operation6 and Sequential Bytes Write Operation .
The NVRAM support Fast-mode as defined in the UM10204, I2C-bus specification and user manual, Rev. 6 – 4 April 2014.
The default value in the NVRAM is 00h for the entire 128 bytes.

Identification:

Table 1:Loopback ID registers

Page	Address	Size	Name	Description
N/A	0	1	Identifier	19h: Identifier Type of OSFP
	3	1	Module state	b0000_011x: ModuleLowPwr state.
	85	1	Module Type Encodings	0x03: Passive Cu
	86	1	ApSelCode 1: Host Electrical Interface Code	0x49: 800GBASE-CR8 (Ethernet Technology Consortium)
	87	1	ApSelCode 1: Module Media Interface Code	0xBF: Passive Loopback Module
00h	128	1	Identifier	19h: Identifier Type of OSFP
	129-144	16	Vendor name	Vendor name (ASCII)
	148-163	16	Vendor PN	Part number provided by vendor (ASCII)
	164-165	2	Vendor rev	Revision (ASCII)
	166-181	16	Vendor SN	Vendor Serial Number (ASCII)
	200	1	Maximum Power identifier	bxxxx 01xx: 30-Watt loopback bxxxx_11xx: 0-Watt loopback Refer to address 201
	201	1	Max Power	0x78 (30W/0.25W = 120) 0x00 (0W,Without Power burner. Only EEPROM)

Table 2: Loopback non-ID registers:

Page	Address	Size	Name	Description
N/A	12-15	4	Temperature DOM	
	16-17	2	Voltage DOM	
	26	1	Self-reset	
00h	200	bit 7-4	Power burner control	
	213-216	4	Power burner setting	
03h	127-255	128	NVRAM	
FFh	225	bit 1-0	Low-Speed Signal Status	
		bit 4-3	Low-Speed Signal state transaction	
	226-229	4	Low-Speed Signal voltage DOM	
	250-251	2	Power-cycle counter	
	252-253	2	Contact pads insertion cycle	
	254	bit 7-4	Low-Speed Signal Control	

Case temperature monitor

The Case temperatures(0□~85℃) is monitored on the top of the case

Table 3: temperature DOM

Page	Address	Size	Name	Description
N/A	12	1	Reserved / Temperature 2 MSB	Internally measured temperature, top case: signed 2's complement in 1/256℃ increments NOTE: Temperature can be below 0℃
	13	1	Custom / Temperature 2 LSB	
	14	1	Module Monitor 1: Temperature 1 MSB	Internally measured temperature, top case: signed 2's complement in 1/256℃ increments NOTE: Temperature can be below 0℃
	15	1	Module Monitor 1: Temperature 1 LSB	

Power rail voltage monitor

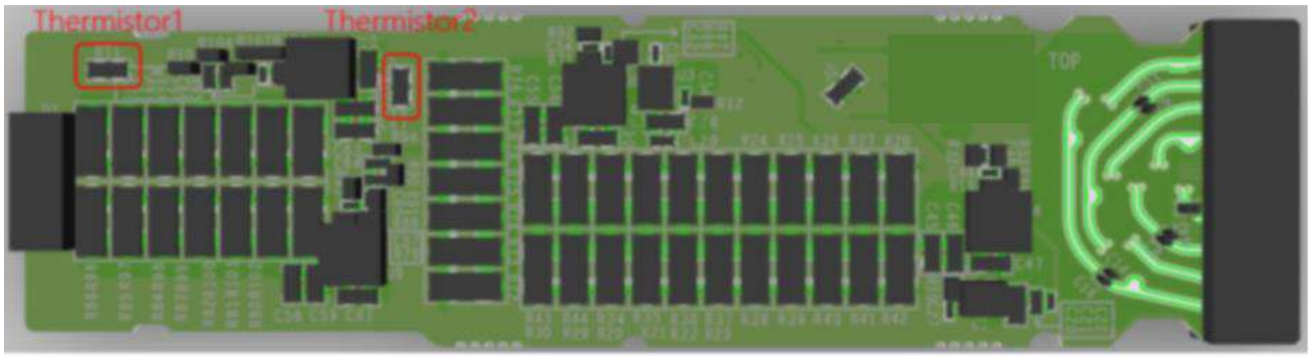
The 4 VCC power pins are tied together to formed a single power rail in order to be monitored..

Table 4: VCC voltage DOM

Page	Address	Size	Name	Description
N/A	16	1	Module Monitor 2: Supply 3.3-volt MSB	Internally measured 3.3volt input supply voltage:in 100μV increments
	17	1	Module Monitor 2: Supply 3.3-volt LSB	

Temperature sensors

The temperature is based on direct measurement and feedback to MCU for built-in algorithms;



Reset requirement

There are 3 different type of reset in the module, power-up-reset, hard-reset and softreset.

Power-up-reset

The power-up-reset should cause all the active components, including the microcontroller, in the module reset to default state and then start the normal operation. It should also reset the power burner in the module to consume the default power.

Falling edge of hard-reset

The soft-reset should cause the microcontroller to reset, and then reset all the other active components and reset the power burner to consume the default power. Afterward, the microcontroller will start the normal operation.

Soft-reset

The soft-reset should cause the microcontroller to reset, and then reset all the other active components and reset the power burner to consume the default power. Afterward, the microcontroller will start the normal operation. The soft-reset is set by host through the I2C register 26 bit 3.

Table 5: Soft-reset register

Page	Address	Size	Name	Description	Type
N/A	26	3	Software Reset	Software reset	RW, Self-Clear

Programmable power consumption/burner

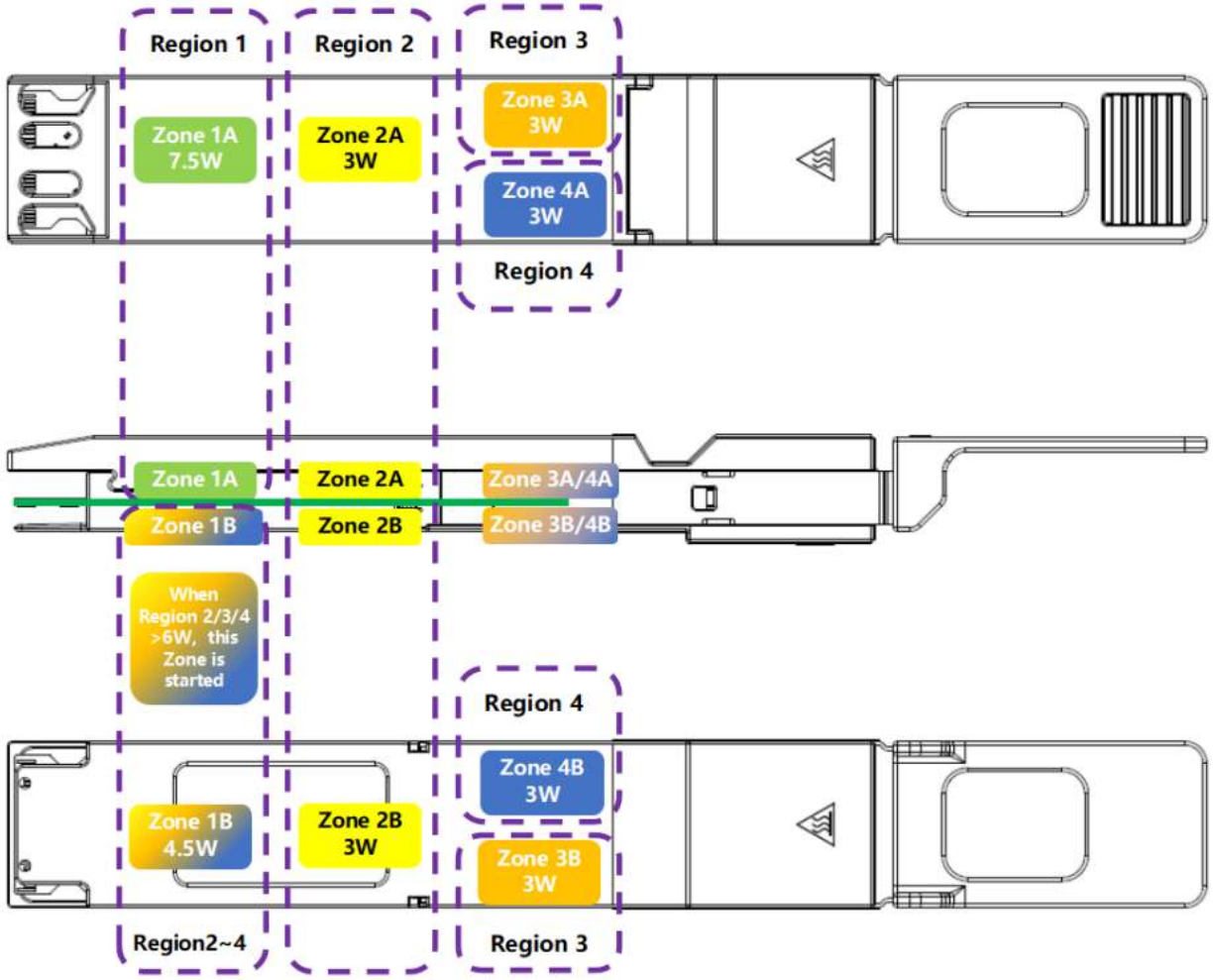
During power-up of the module, the default power consumption in the module should burn less than 0.5W to boot up the MCU and associated control logic/circuitry as default. Afterward, host can set the module to consume higher power by programming the 4 burners in 4 regions through I2C registers 200, 213-216.

Table 6: power burner registers

Page	Address	Bits	Name	Description	Type
00h	200	7	Region 4 burner	The burner in each region is individually enabled by these bits. 0b: Disable (default) 1b: Enable	RW
		6	Region 3 burner		
		5	Region 2 burner		
		4	Region 1 burner		
		3-2	Maximum Power identifier	01b: Refer to address 201	RO
		1-0	Reserved	00b	RO
	213	7-0	Region 4 power consumption	The power in these 4 regions are individually programmed between 1.0W through 7.5W 10h: 1.0W (default) 18h: 1.5W 20h: 2.0W 28h: 2.5W 30h: 3.0W 38h: 3.5W 40h: 4.0W 48h: 4.5W 50h: 5.0W 58h: 5.5W 60h: 6.0W 68h: 6.5W 70h: 7.0W 78h: 7.5W Else: remain the current value. The tolerance of power consumption must meet the following criteria : +/-5% @ VCC = 3.3V +/-2% +/-11% @ VCC = 3.3V +/-5% +/-20% @ VCC = 3.3v +/-10%	RW
	214	7-0	Region 3 power consumption		RW
	215	7-0	Region 2 power consumption		RW
	216	7-0	Region 1 power consumption		RW

Power distribution

The power burner is placed on the top and bottom side of paddle PCB with all the heat be dissipated at the top of the case. The power burner is separated into 4 regions as shown:



Pull-up/down resistor detection of the Low-Speed Signals on host

the module is able to report the logical 1 (Vi > 1.25V) or logical 0 (Vi < 1.25V) of these signals in I2C register Page FFh.

Table 7: Low-Speed Signal status registers

Page	Address	Size	Name	Description	Type
FFh	225	1	LPWn/PRSn signal status	0b: logical 0 (VLPWn/PRSn < 1.25V) 1b: logical 1 (VLPWn/PRSn > 1.25V)	RO

The lag time should be less than 10.0 msec from the corresponding logical value occurred on LPWn/PRSn until the bit 1 and/or 0 in Page FFh 225 is set to correct logical value to be read by I2C operation.

Digital state detection and report on LPWn

The module is able to detect the digital state of the LPWn on LPWn/PRSn signals. A I2C latch register in Page FFh should be latched on the change of the digital state, both 1→ 0 and 0 → 1, on the LPWn. The latch register will be cleared when host write an “1” to it.

Table 8: Low-Speed Signal state transaction registers

Page	Address	Size	Name	Description	Type
FFh	225	4	LPWn state transaction	Read 0b: No edge detected Read 1b: Either rising or falling edges crossing the 1.25V Thresholds is detected Write 0b: No effect Write 1b: Clear the register	RW

The lag time should be less than 10.0 msec from the corresponding transaction edge occurred on LPWn until the bit 4 and/or 3 in Page FFh Address 225 is set to be read by I2C operation.

Detection of the missing 68kΩ pull-down on INT/RSTn signal

The LPWn/PRSn and INT/RSTn signals will be monitored by ADC on the module.
The ADC output will be presented as a 16-bit unsigned integer with the voltage defined as the full 16-bit value with LSB equal to 100μV at I2C registers 226(MSB) and 227(LSB) for LPWn/PRSn signal and 228(MSB) and 229(LSB) for INT/RSTn signal in Page FFh. Voltage accuracy should be +/-1%

Table 9: Low-Speed Signal voltage DOM

Page	Address	Size	Name	Description
FFh	226	1	LPWn/PRSn voltage MSB	Internally measured LPWn/PRSn voltage: in 100μV increments
	227	1	LPWn/PRSn voltage LSB	
	228	1	INT/RSTn voltage MSB	Internally measured INT/RSTn voltage: in 100μV increments
	229	1	INT/RSTn voltage LSB	

PRSn

The PRSn is pulled towards ground in the module.

Power-cycle counter

When the MCU in the module is powered-up, the power-cycle counter must be implemented. The default value of the counter is 00h. The value of the counter must be saved in I2C registers in Page FFh.

Table 10: Power-cycle counter registers

Page	Address	Size	Name	Description	Type
FFh	250	1	Power-cycle counter, MSB	Power-cycle counter.Default to 00_00h from factory.	RO
	251	1	Power-cycle counter, LSB		RO

Contact pads insertion and module reliability

Table 11: Contact pads insertion cycle registers

Page	Address	Size	Name	Description	Type
FFh	252	1	Guaranteed maximum insertion/temperature cycle, MSB	Guaranteed maximum insertion/temperature cycle in hex. The goal is 2000 (07D0h) insertions.	RO
	253	1	Guaranteed maximum insertion/temperature cycle, LSB		RO

Alarm and Warning Thresholds(Page 02H Byte 128~143)

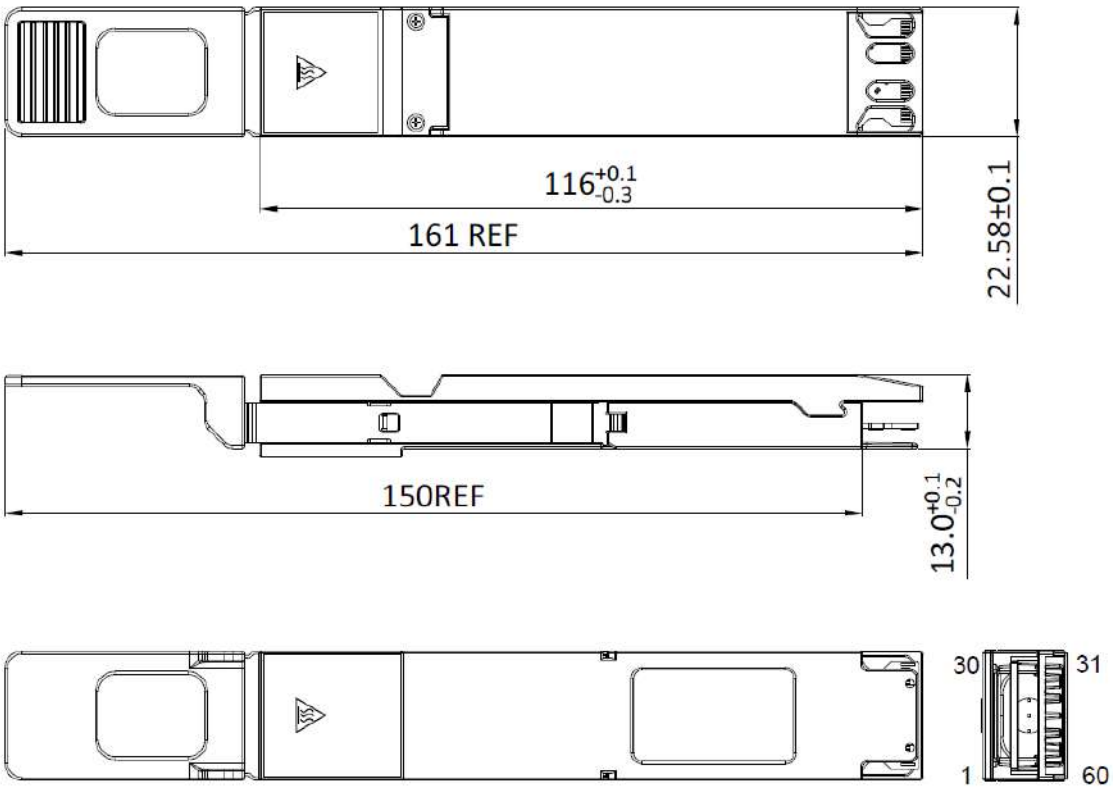
Page	Address	Field Size(Byte)	Name of field	Description
02h	128-129	2	Temp High Alarm	MSB at low address, 95℃
	130-131	2	Temp Low Alarm	MSB at low address, -10℃
	132-133	2	Temp High Warning	MSB at low address, 85℃
	134-135	2	Temp Low Warning	MSB at low address, -5℃
	136-137	2	VCC Voltage High Alarm	MSB at low address, 3.6V
	138-139	2	VCC Voltage Low Alarm	MSB at low address, 3.0V
	140-141	2	VCC Voltage High Warning	MSB at low address, 3.5V
	142-143	2	VCC Voltage Low Warning	MSB at low address, 3.1V

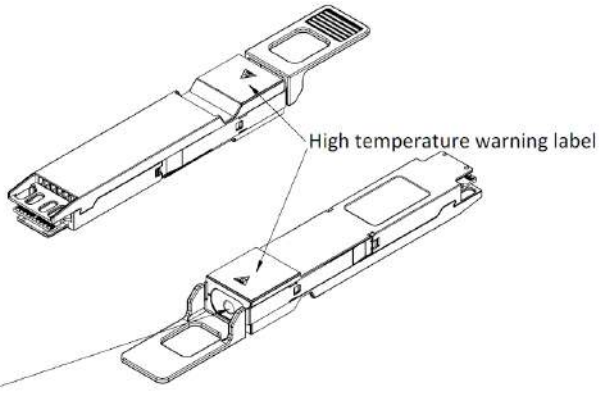
PS: Alarm and Warning Thresholds can be customized according to customer requirements

Package Outline

Dimensions are in millimeters. (Unit: mm)

OSFP Type2 Flat Top style:





LED

Installation: RED LED: When Power-up-reset or Soft-reset
Red LED: When voltage on LPWn/PRSn is below 0.3V
Green LED: Once the LPWn/PRSn is above 0.3V, and Start the Normal operation.

Solid green: low-power mode
Solid red: high-power mode
Blinking green: low-power mode with any of the interrupt flag is set
Blinking red: high-power mode with any of the interrupt flag is set
LED should be below black SR surface