DUAL N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV_{DSS}	$R_{DS(ON)}$ Max	I_D T_C = +25°C
30V	20mΩ @ V_{GS} = 10V	16A
	32mΩ @ V_{GS} = 4.5V	13A

Description

This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- Backlighting
- Power Management Functions
- DC-DC Converters

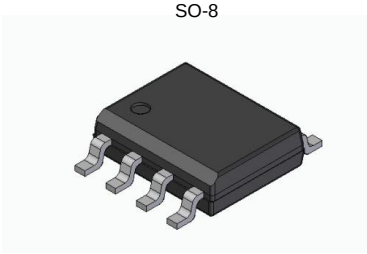
Features

- Dual N-Channel MOSFET
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- 100% Unclamped Inductive Switching (UIS) Test in Production – Ensures More Reliable and Robust End Application
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.**
  https://www.diodes.com/quality/product-definitions/
- **An Automotive-Compliant Part is Available Under Separate Datasheet (DMT3020LSDQ)**

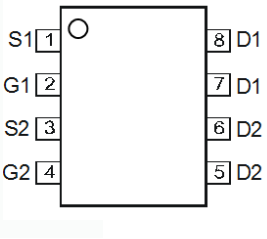
Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals Connections Indicator: See Diagram
- Terminals: Finish - Matte Tin Annealed over Copper Lead Frame. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.072 grams (Approximate)

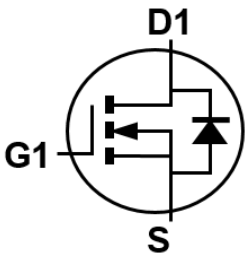
SO-8



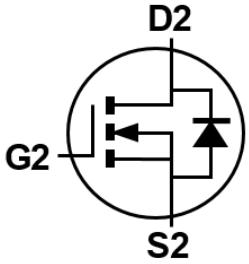
Top View



Internal Schematic



N-Channel MOSFET



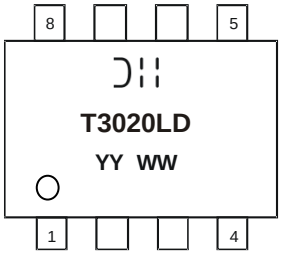
N-Channel MOSFET

Ordering Information (Note 4)

Part Number	Case	Packaging
DMT3020LSD-13	SO-8	2500/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



= Manufacturer's Marking
T3020LD = Product Type Marking Code
YYWW = Date Code Marking
YY or YY= Year (ex: 21 = 2021)
WW = Week (01 to 53)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	30	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current, V_{GS} = 10V (Note 7)	Steady State	T_C = +25°C T_C = +70°C	I_D	16 13	A
Maximum Body Diode Forward Current (Note 7)			I_S	8	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	50	A
Pulsed Drain Body Diode Forward Current (10µs Pulse, Duty Cycle = 1%)			I_{SM}	50	A
Avalanche Current (L = 0.1mH) (Note 8)			I_{AS}	13	A
Avalanche Energy (L = 0.1mH) (Note 8)			E_{AS}	8.5	mJ

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)		P_D	1.0	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	117	°C/W
Total Power Dissipation (Note 6)		P_D	1.5	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	81	°C/W
Thermal Resistance, Junction to Case (Note 7)		$R_{\theta JC}$	20	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV_{DSS}	30.0	—	—	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	1.0	µA	V_{DS} = 24V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	$V_{GS(TH)}$	1.0	—	2.5	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	—	20	mΩ	V_{GS} = 10V, I_D = 9.0A
			—	32		V_{GS} = 4.5V, I_D = 7.0A
Diode Forward Voltage	V_{SD}	—	—	1.2	V	V_{GS} = 0V, I_S = 2A
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	C_{iss}	—	393	—	pF	V_{DS} = 15V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	173	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	27	—	pF	
Gate Resistance	R_g	—	1.1	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz
Total Gate Charge (V_{GS} = 10V)	Q_g	—	7.0	—	nC	V_{DD} = 15V, I_D = 9A
Total Gate Charge (V_{GS} = 4.5V)	Q_g	—	3.6	—	nC	
Gate-Source Charge	Q_{gs}	—	0.9	—	nC	
Gate-Drain Charge	Q_{gd}	—	1.5	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	1.8	—	ns	V_{DD} = 15V, V_{GS} = 10V, R_G = 6Ω, I_D = 9A
Turn-On Rise Time	t_R	—	1.9	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	7.5	—	ns	
Turn-Off Fall Time	t_F	—	2.4	—	ns	
Reverse Recovery Time	t_{RR}	—	10	—	ns	I_F = 9A, dI/dt = 100A/µs
Reverse Recovery Charge	Q_{RR}	—	2.6	—	nC	

Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
7. Thermal resistance from junction to soldering point (on the exposed drain pad).
8. I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep T_J = +25°C.
9. Short duration pulse test used to minimize self-heating effect.
10. Guaranteed by design. Not subject to product testing.

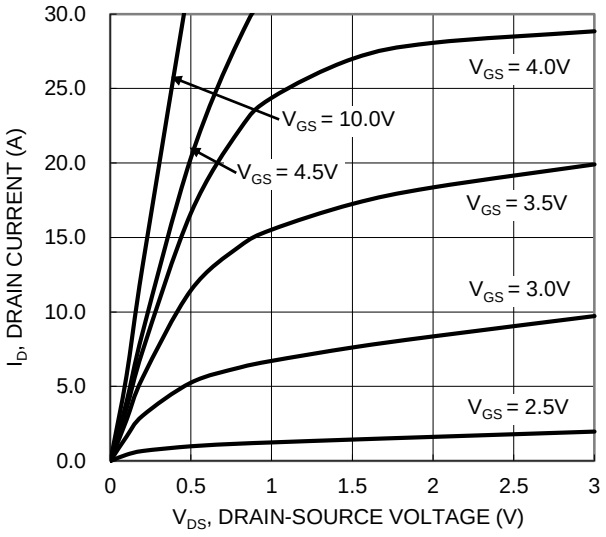


Figure 1.Typical Output Characteristic

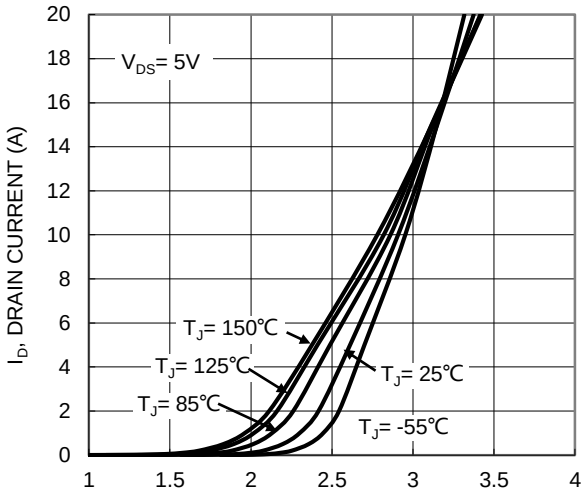


Figure 2. Typical Transfer Characteristic

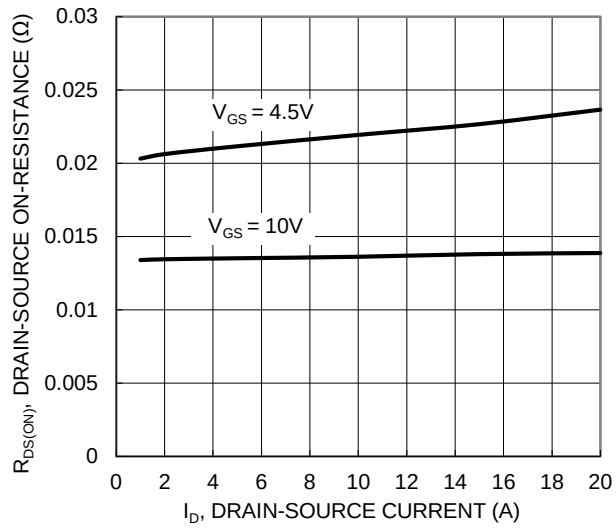


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

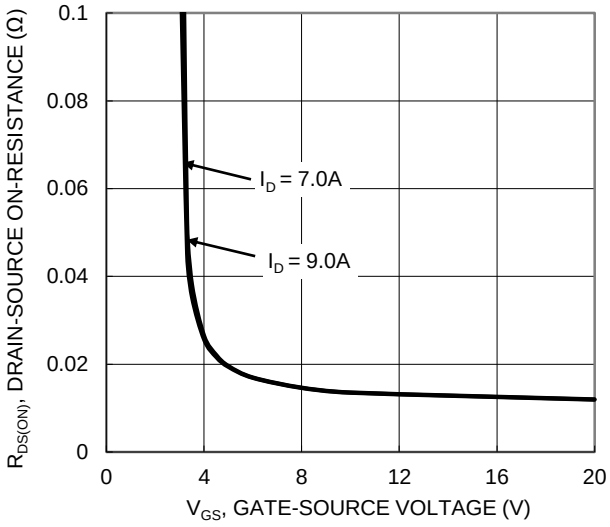


Figure 4. Typical Transfer Characteristic

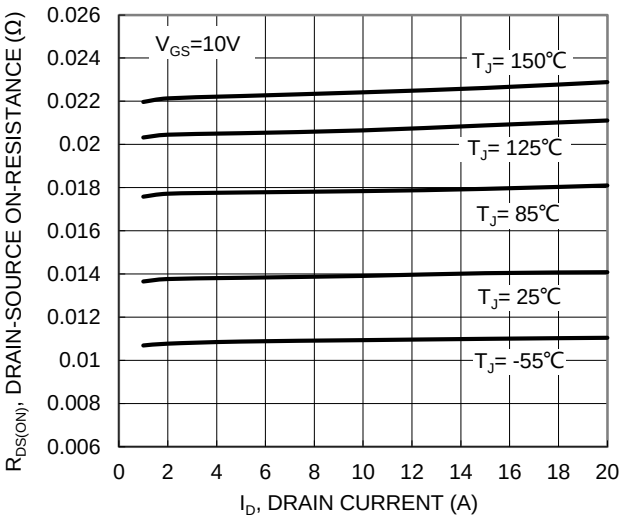


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

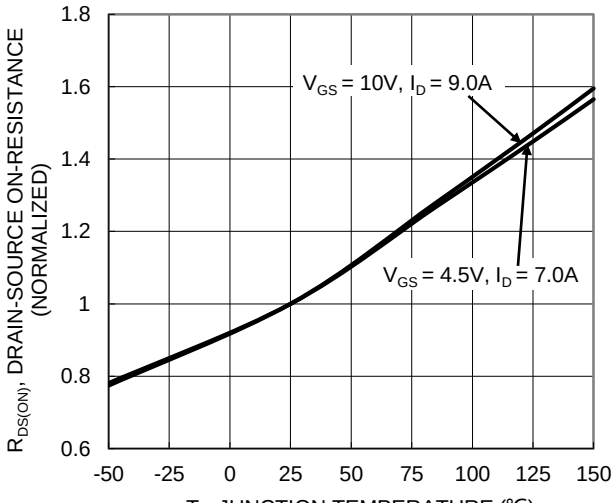


Figure 6. On-Resistance Variation with Temperature

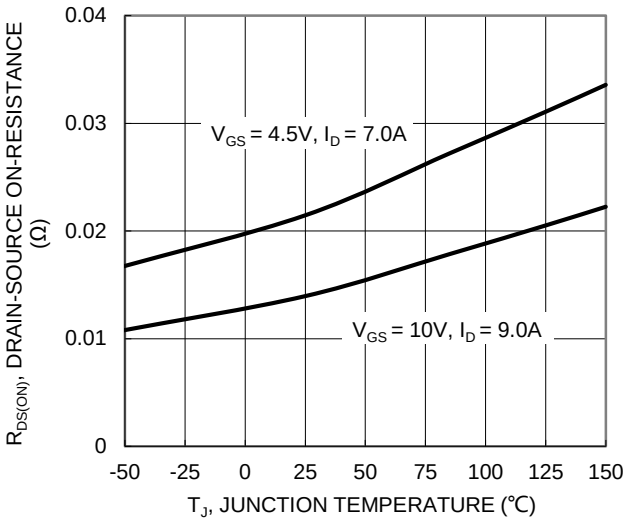


Figure 7. On-Resistance Variation with Temperature

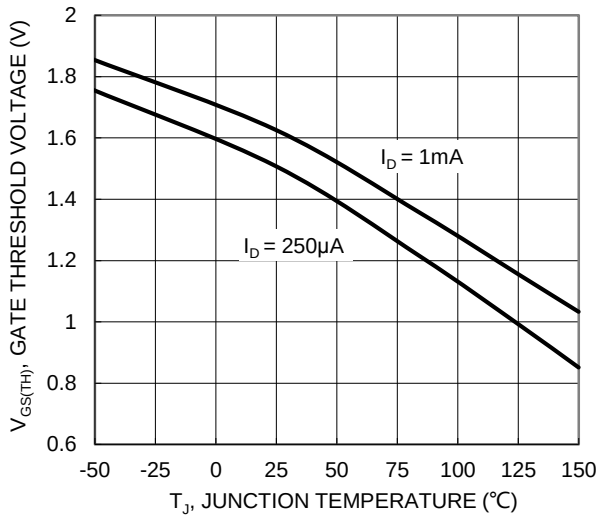


Figure 8. Gate Threshold Variation vs. JunctionTemperature

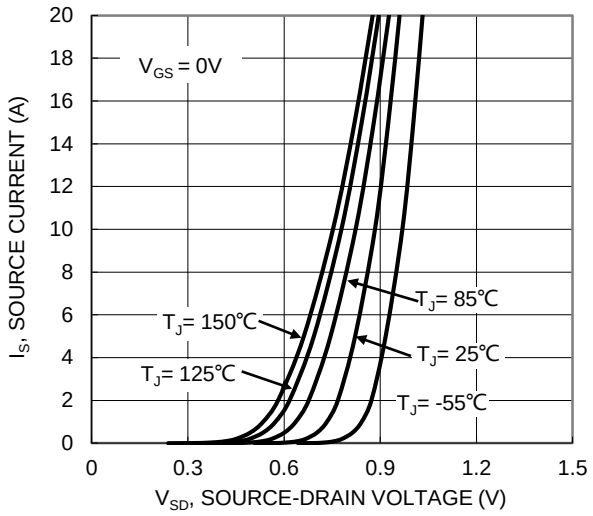


Figure 9. Diode Forward Voltage vs. Current

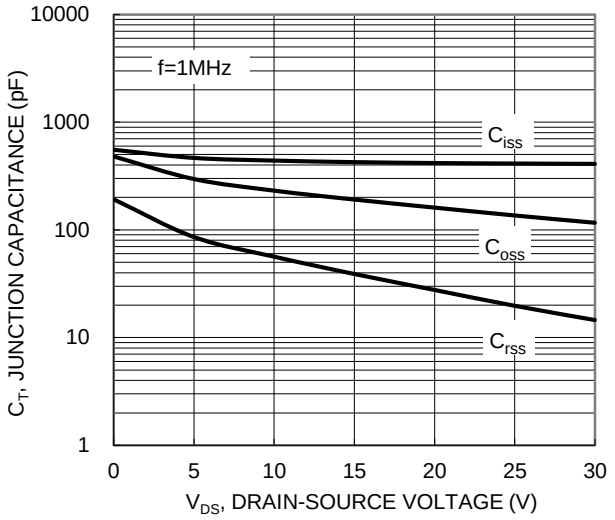


Figure 10. Typical Junction Capacitance

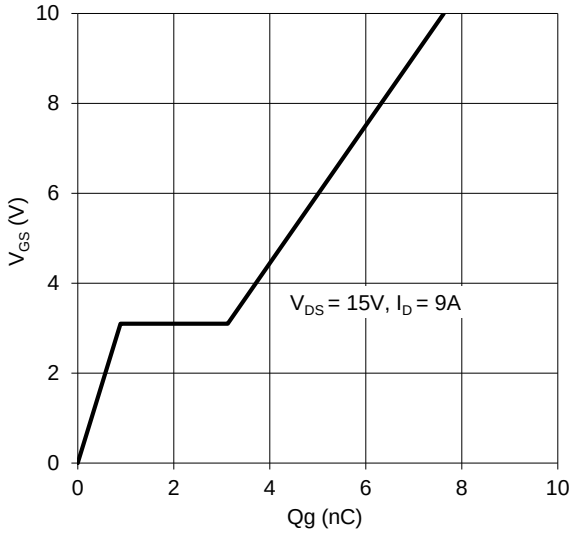


Figure 11. Gate Charge

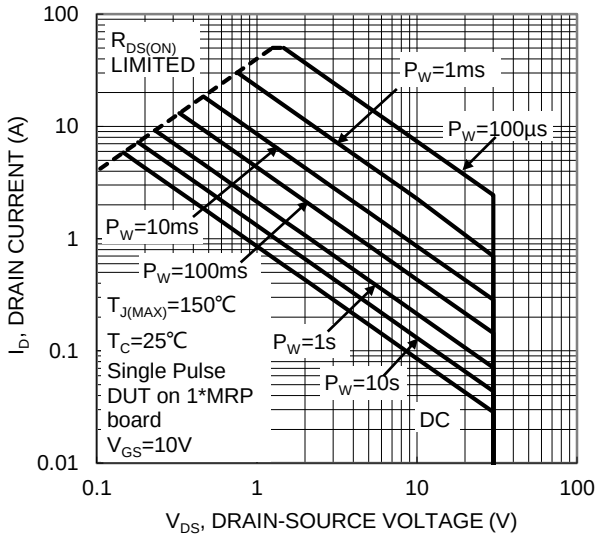


Figure 12. SOA, Safe Operation Area

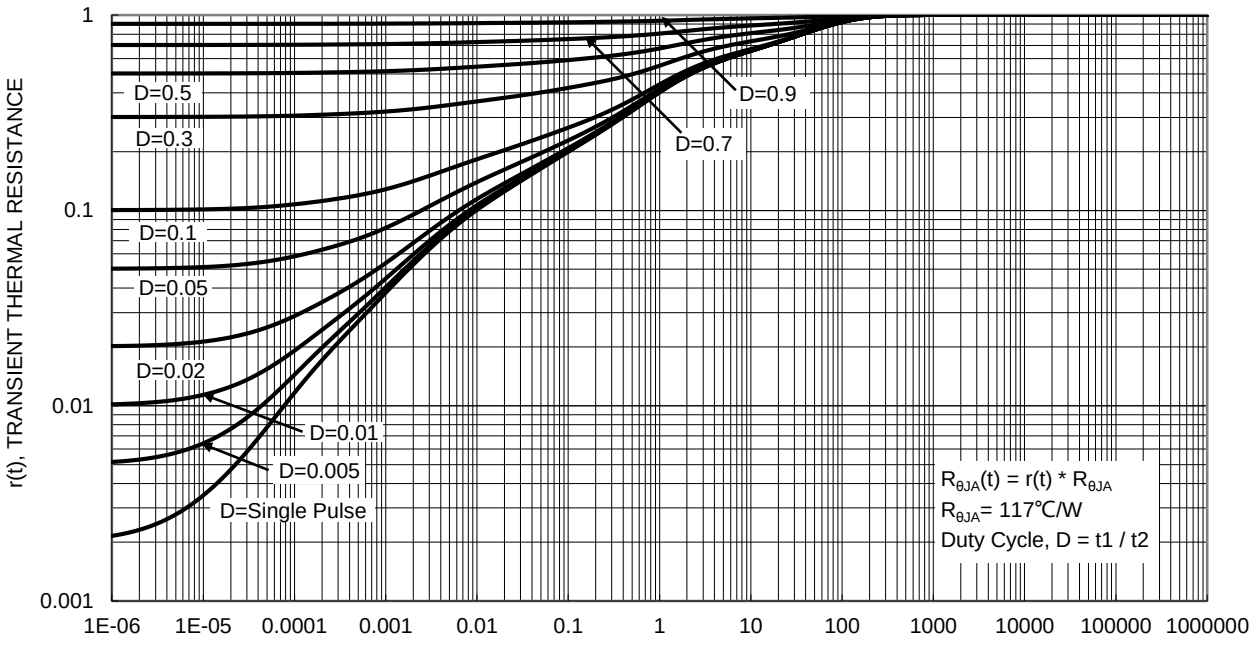


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

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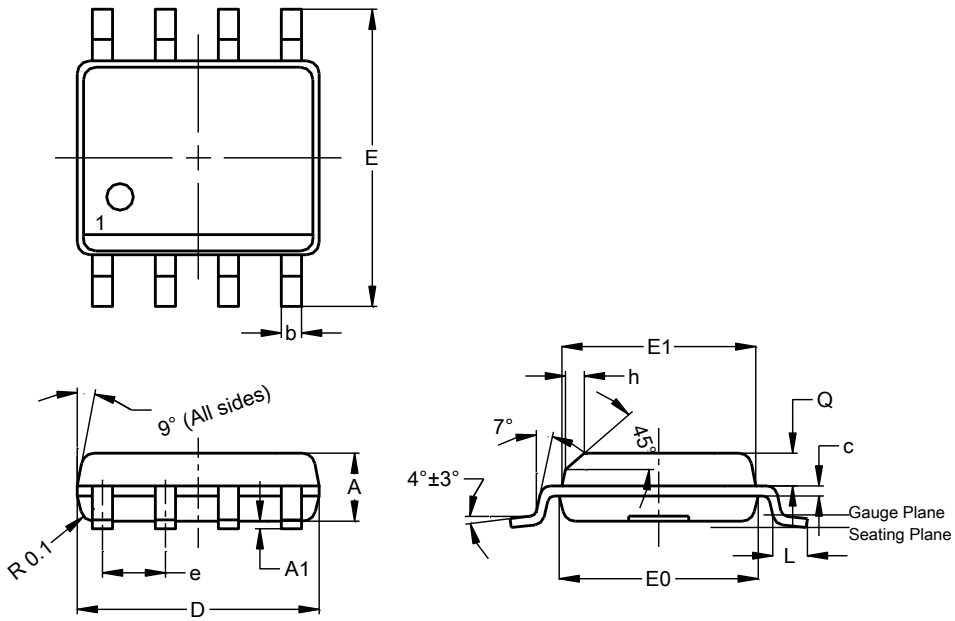
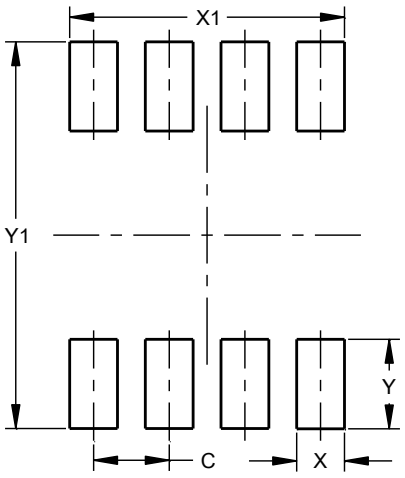


SO-8			
Dim	**Min**	**Max**	**Typ**
A	1.40	1.50	1.45
A1	0.10	0.20	0.15
b	0.30	0.50	0.40
c	0.15	0.25	0.20
D	4.85	4.95	4.90
E	5.90	6.10	6.00
E1	3.80	3.90	3.85
E0	3.85	3.95	3.90
e	--	--	1.27
h	--	--	0.35
L	0.62	0.82	0.72
Q	0.60	0.70	0.65
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8



Dimensions	Value (in mm)
C	1.27
X	0.802
X1	4.612
Y	1.505
Y1	6.50

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