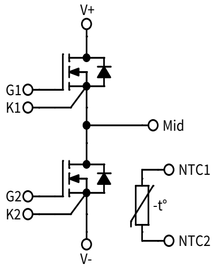
CAB760M12HM3

1200 V, 760 A, Silicon Carbide, Half-Bridge Module

V_{DS}	**1200 V**
I_{DS}	**760 A**

Technical Features

- Low Inductance, Low Profile 62 mm Footprint
- High Junction Temperature (175 °C) Operation
- Implements Switching Optimized Third Generation SiC MOSFET Technology
- Light Weight AlSiC Baseplate
- High Reliability Silicon Nitride Insulator



Applications

- Railway & Traction
- Solar
- EV Chargers
- Industrial Automation & Testing

System Benefits

- Lightweight, Compact Form Factor with 62 mm Compatible Baseplate Enables System Retrofit
- Increased System Efficiency, due to Low Switching & Conduction Losses of SiC
- High Reliability Material Selection

Key Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Note
Drain-Source Voltage	V_{DS}			1200	V	T_C = 25 °C	
Gate-Source Voltage, Maximum Value	$V_{GS(max)}$	-8		+19		Transient	Note 1 Fig. 32
Gate-Source Voltage, Recommended	$V_{GS(op)}$		-4/+15			Static	
DC Continuous Drain Current	I_D		1015		A	V_{GS} = 15 V, T_C = 25 °C, T_{VJ} ≤ 175 °C	Notes 2, 3 Fig. 20
			765			V_{GS} = 15 V, T_C = 90 °C, T_{VJ} ≤ 175 °C	
DC Source-Drain Current (Body Diode)	$I_{SD(BD)}$		515			V_{GS} = -4 V, T_C = 25 °C, T_{VJ} ≤ 175 °C	
Pulsed Drain-Source Current	I_{DM}		1530			t_{Pmax} limited by T_{VJmax} V_{GS} = 15 V, T_C = 25 °C	
Power Dissipation	P_D		2206		W	T_C = 25 °C, T_{VJ} ≤ 175 °C	Note 4 Fig. 20
Virtual Junction Temperature	$T_{VJ(op)}$	-40		175	°C		

Note (1): Recommended turn-on gate voltage is 15 V with ±5 % regulation tolerance
Note (2): Current limit at T_C = 90 °C calculated by $I_{D(max)} = \sqrt{(P_D/R_{DS(typ)}(T_{VJ(max)}, I_{D(max)}))}$
Note (3): Verified by design
Note (4): $P_D = (T_{VJ} - T_C)/R_{TH(JC,typ)}$

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MOSFET Characteristics (Per Position) (T_{VJ} = 25 °C Unless Otherwise Specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1200			V	V_{GS} = 0 V, T_{VJ} = -40 °C	
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.5	3.6		$V_{DS} = V_{GS}$, I_D = 280 mA	
			2.0			$V_{DS} = V_{GS}$, I_D = 280 mA, T_{VJ} = 175 °C	
Zero Gate Voltage Drain Current	I_{DSS}		15	400	µA	V_{GS} = 0 V, V_{DS} = 1200 V	
Gate-Source Leakage Current	I_{GSS}		0.12	3		V_{GS} = 15 V, V_{DS} = 0 V	
Drain-Source On-State Resistance (Devices Only)	$R_{DS(on)}$		1.33	1.73	mΩ	V_{GS} = 15 V, I_D = 760 A	Fig. 2 Fig. 3
			2.13			V_{GS} = 15 V, I_D = 760 A, T_{VJ} = 175 °C	
Transconductance	g_{fs}		548		S	V_{DS} = 20 V, I_{DS} = 760 A	Fig. 4
			585			V_{DS} = 20 V, I_{DS} = 760 A, T_{VJ} = 175 °C	
Turn-On Switching Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 175 °C	E_{ON}		20.3 20.7 23.7		mJ	V_{DS} = 600 V, I_D = 760 A, V_{GS} = -4 V/15 V, $R_{G(ext)}$ = 1.0 Ω, L = 13.7 µH	Fig. 11 Fig. 13
Turn-Off Switching Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 175 °C	E_{OFF}		17.9 17.5 17.8				
Internal Gate Resistance	$R_{G(int)}$		0.47		Ω	V_{AC} = 25 mV, f = 100 kHz	
Input Capacitance	C_{iss}		79.4		nF	V_{GS} = 0 V, V_{DS} = 800 V, V_{AC} = 25 mV, f = 100 kHz	Fig. 9
Output Capacitance	C_{oss}		2.9				
Reverse Transfer Capacitance	C_{rss}		90		pF		
Gate to Source Charge	Q_{GS}		768		nC	V_{DS} = 800 V, V_{GS} = -4 V/15 V I_D = 760 A Per IEC60747-8-4 pg 21	
Gate to Drain Charge	Q_{GD}		924				
Total Gate Charge	Q_G		2724				
FET Thermal Resistance, Junction to Case	$R_{th\ JC}$		0.068	0.073	°C/W		Fig. 17

Diode Characteristics (Per Position) (T_{VJ} = 25 °C Unless Otherwise Specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Note
Body Diode Forward Voltage	V_{SD}		5.4		V	V_{GS} = -4 V, I_{SD} = 760 A	Fig. 7
			4.7			V_{GS} = -4 V, I_{SD} = 760 A, T_{VJ} = 175 °C	
Reverse Recovery Time	t_{RR}		49		ns	V_{GS} = -4 V, I_{SD} = 760 A , V_R = 600 V di/dt = 20 A/ns, T_{VJ} = 175 °C	Fig. 32
Reverse Recovery Charge	Q_{RR}		17.0		µC		
Peak Reverse Recovery Current	I_{RRM}		540		A		
Reverse Recovery Energy T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 175 °C	E_{RR}		1.3 3.5 5.5		mJ	V_{DS} = 600 V, I_D = 760 A, V_{GS} = -4 V/15 V, $R_{G(ext)}$ = 1.0 Ω, L = 13.7 µH	Fig. 14

Module Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Package Resistance, M1	R_{1-2}		106.5		μΩ	T_C = 125 °C, Note 5
Package Resistance, M2	R_{2-3}		126.3		μΩ	T_C = 125 °C, Note 5
Stray Inductance	L_{Stray}		4.9		nH	Between Terminals 1 and 3
Case Temperature	T_C	-40		125	°C	
Weight	W		179		g	
Mounting Torque	M_S	3	4.5	5	N-m	Baseplate, M4 Bolts
		0.9	1.1	1.3		Power Terminals, M6 Bolts
Case Isolation Voltage	V_{isol}	4			kV	AC, 50 Hz, 1 min
Comparative Tracking Index	CTI	600				
Clearance Distance		13.07			mm	Terminal to Terminal
		6.00				Terminal to Baseplate
Creepage Distance		14.27				Terminal to Terminal
		12.34				Terminal to Baseplate

Note (5): Total Effective Resistance (Per Switch Position) = MOSFET $R_{DS(on)}$ + Switch Position Package Resistance

Temperature Sensor (NTC) Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Resistance at 25 °C	R_{25}		4700		Ω	T_{NTC} = 25 °C
Tolerance of R_{25}			±1		%	
Beta Value for 25 °C to 85 °C	$B_{25/85}$		3435		K	
Beta Value for 0 °C to 100 °C	$B_{0/100}$		3399		K	
Tolerance of $B_{25/85}$			±1		%	
Maximum Power Dissipation	P_{25}		50		mW	

Steinhart & Hart Coefficients for NTC Resistance & NTC Temperature Computation (T in K)

$$\ln\left(\frac{R}{R_{25}}\right) = A + \frac{B}{T} + \frac{C}{T^2} + \frac{D}{T^3}$$

A	B	C	D
-1.289E+01	4.245E+03	-8.749E+04	-9.588E+06

$$\frac{1}{T} = A_1 + B_1 \ln\left(\frac{R}{R_{25}}\right) + C_1 \ln^2\left(\frac{R}{R_{25}}\right) + D_1 \ln^3\left(\frac{R}{R_{25}}\right)$$

A_1	B_1	C_1	D_1
3.354E-03	3.001E-04	5.085E-06	2.188E-07

Typical Performance

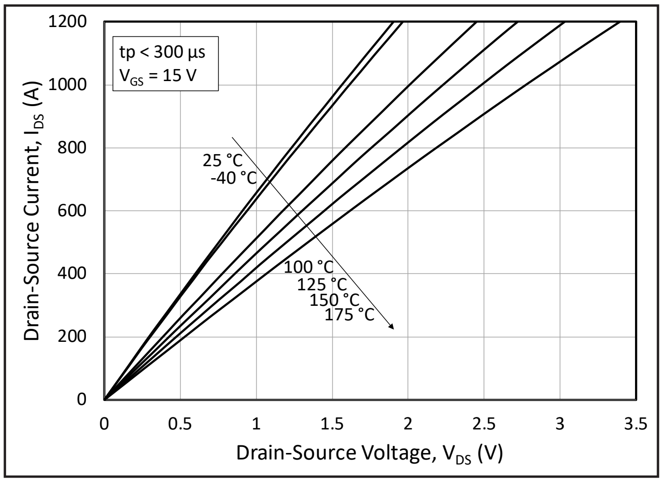


Figure 1. Output Characteristics for Various Junction Temperatures

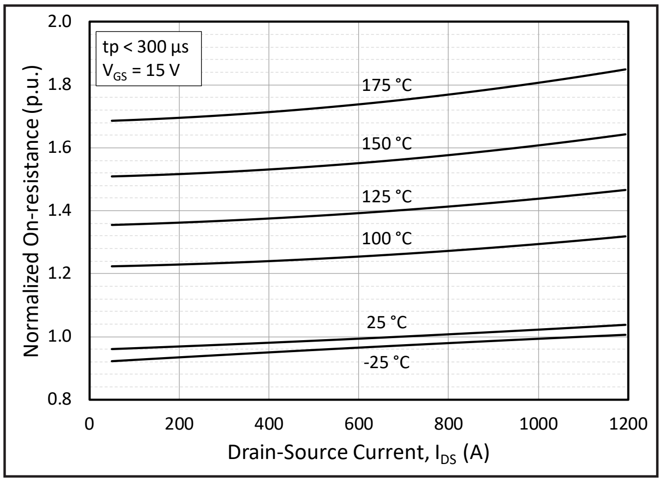


Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures

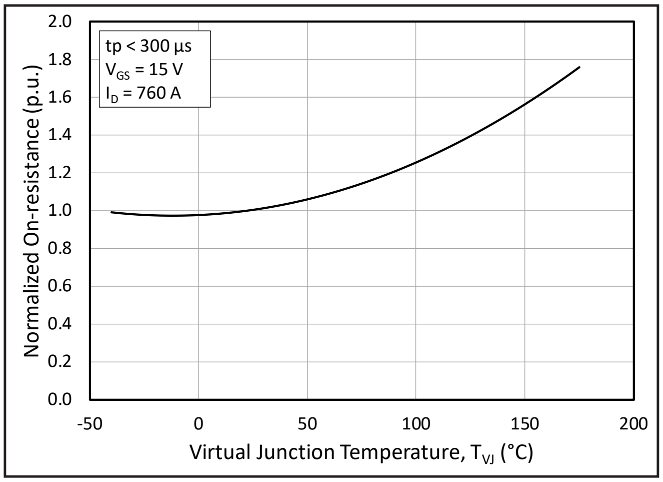


Figure 3. Normalized On-State Resistance vs. Junction Temperature

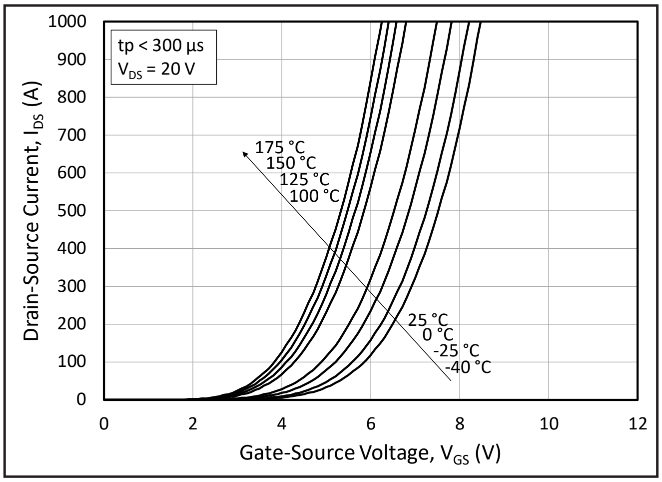


Figure 4. Transfer Characteristic for Various Junction Temperatures

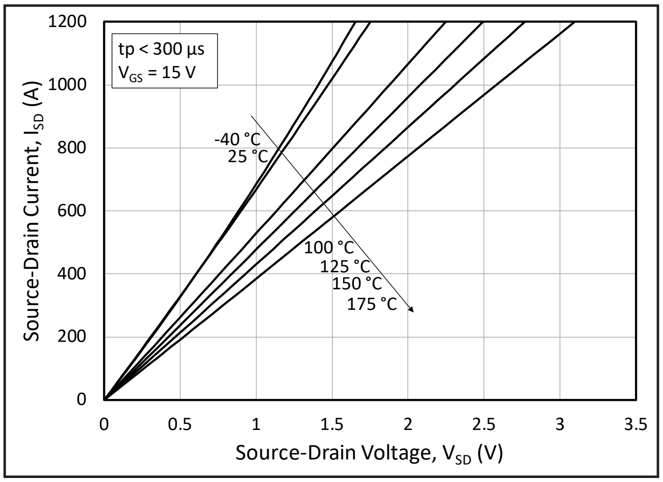


Figure 5. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 15 V

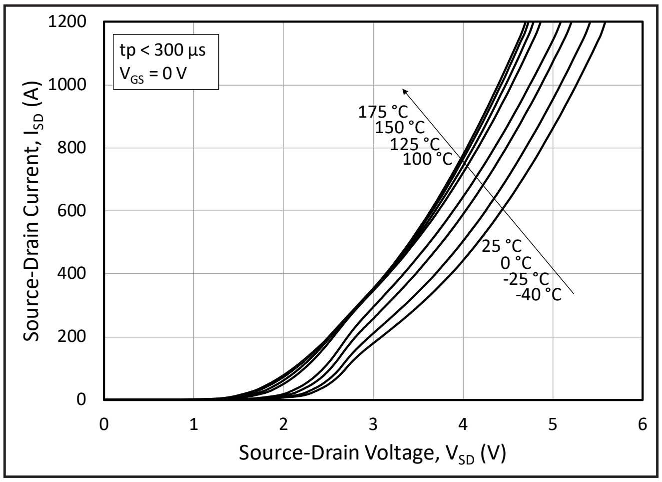


Figure 6. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 0 V (Body Diode)

Typical Performance

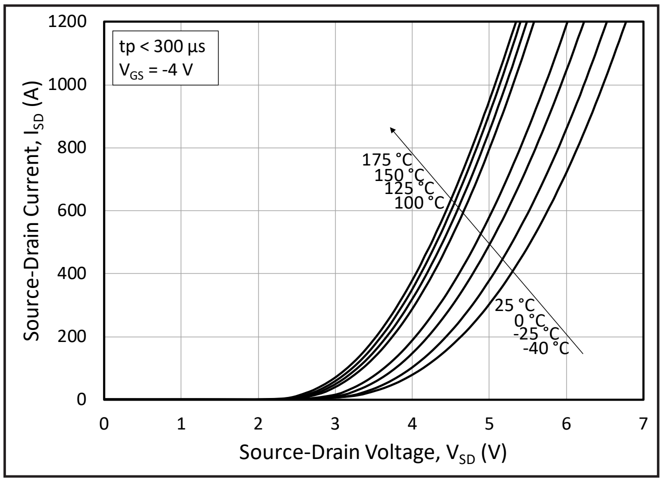


Figure 7. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = -4 V (Body Diode)

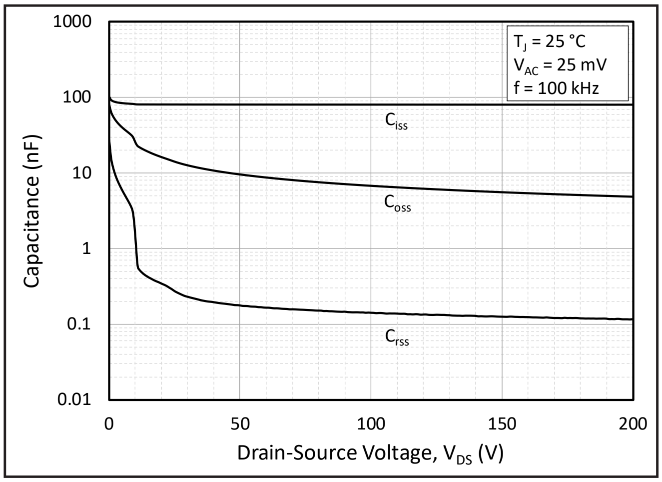


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 - 200 V)

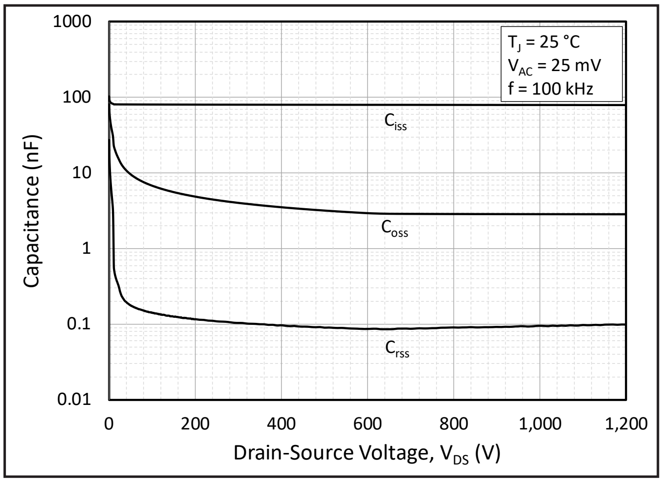


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 - 1200 V)

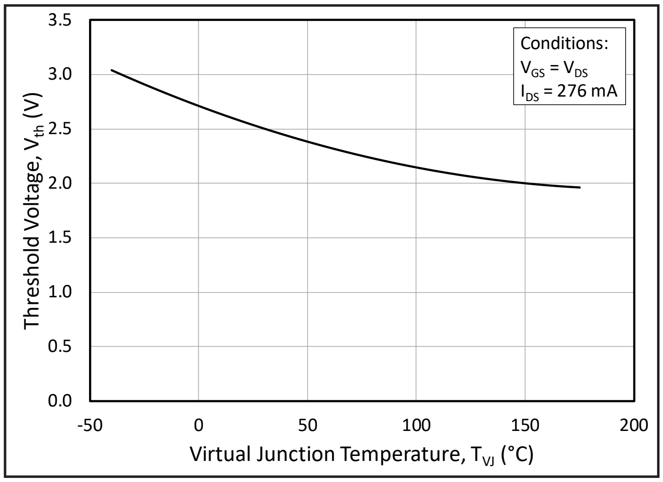


Figure 10. Threshold Voltage vs. Junction Temperature

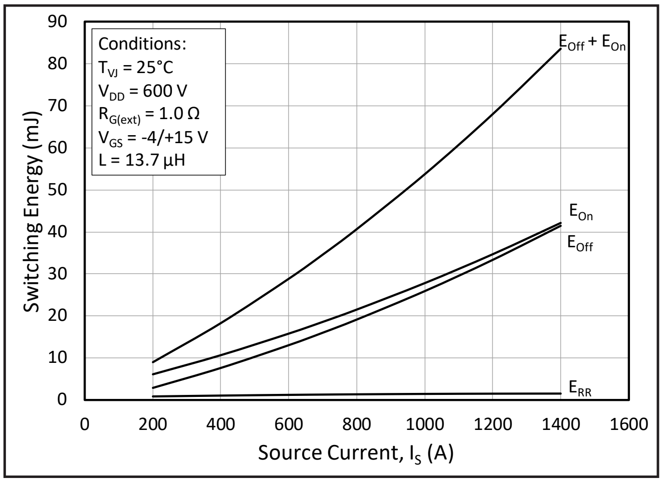


Figure 11. Switching Energy vs. Drain Current (V_{DS} = 600 V)

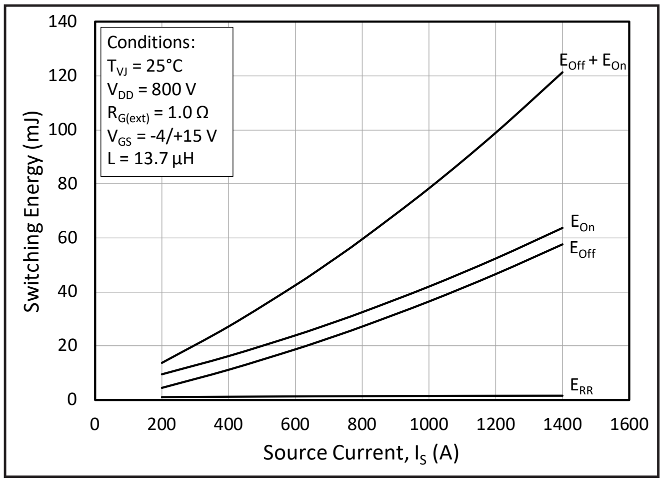


Figure 12. Switching Energy vs. Drain Current (V_{DS} = 800 V)

Typical Performance

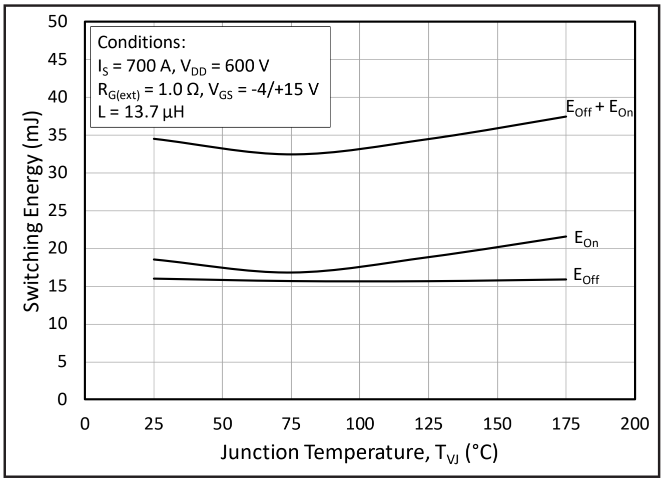


Figure 13. MOSFET Switching Energy vs. Junction Temperature

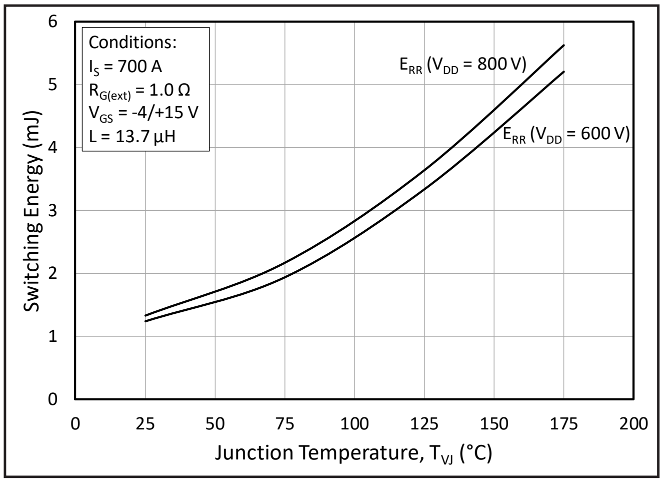


Figure 14. Reverse Recovery Energy vs. Junction Temperature

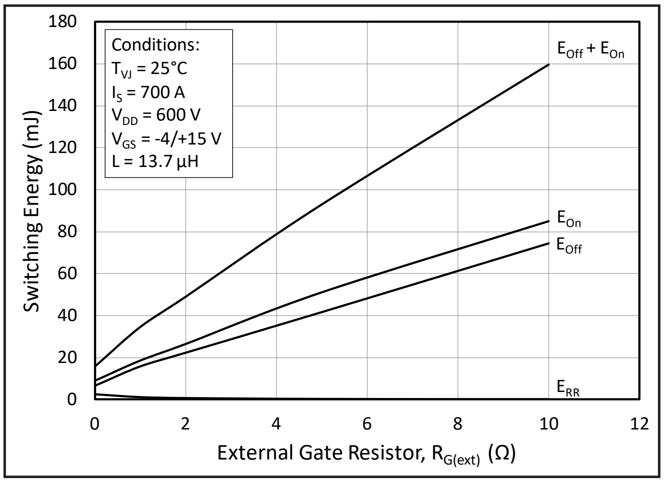


Figure 15. MOSFET Switching Energy vs. External Gate Resistance

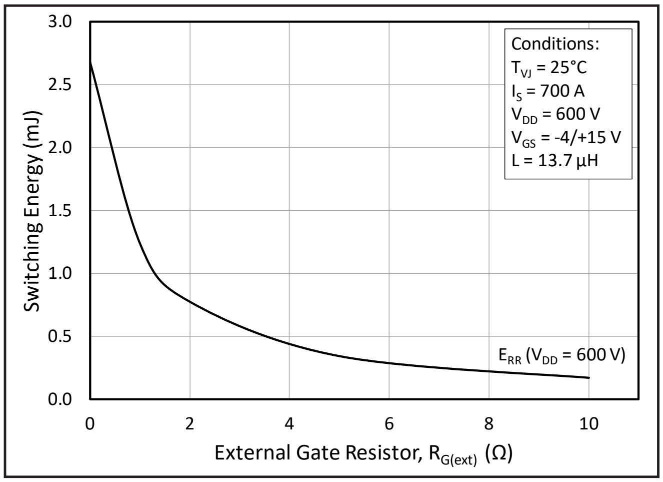


Figure 16. Reverse Recovery Energy vs. External Gate Resistance

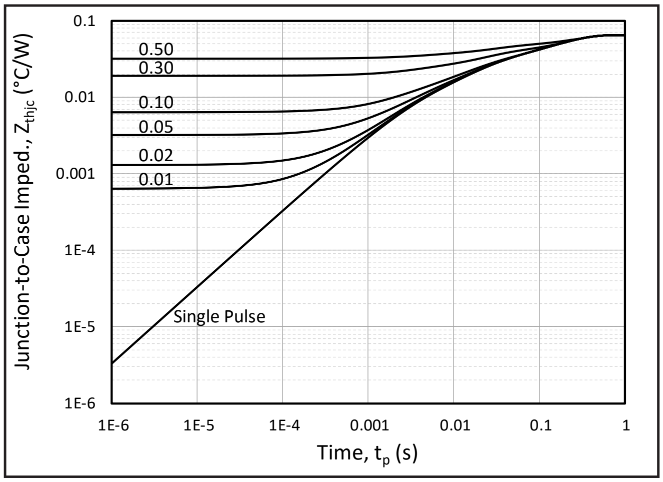


Figure 17. MOSFET Junction to Case Transient Thermal Impedance, $Z_{th\ JC}$ (°C/W)

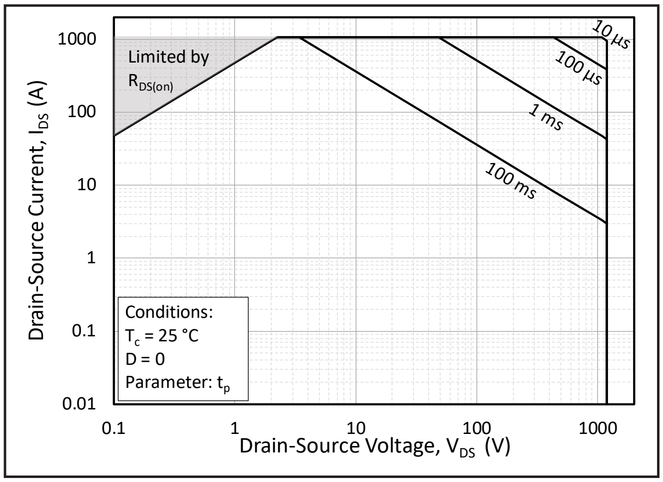


Figure 18. Forward Bias Safe Operating Area (FBSOA)

Typical Performance

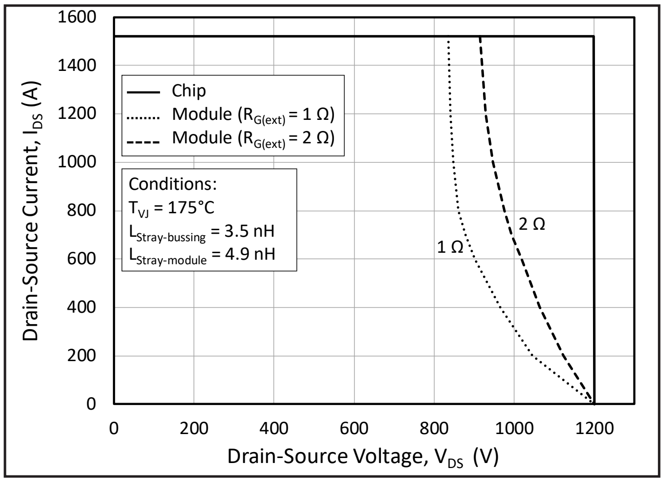


Figure 19. Reverse Bias Safe Operating Area (RBSOA)

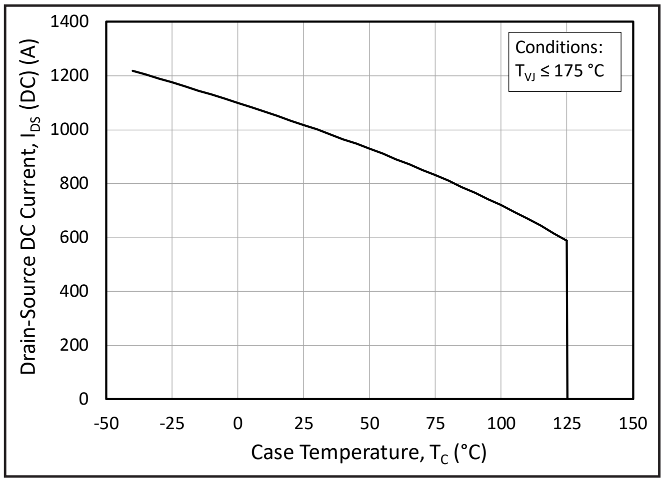


Figure 20. Continuous Drain Current Derating vs. Case Temperature

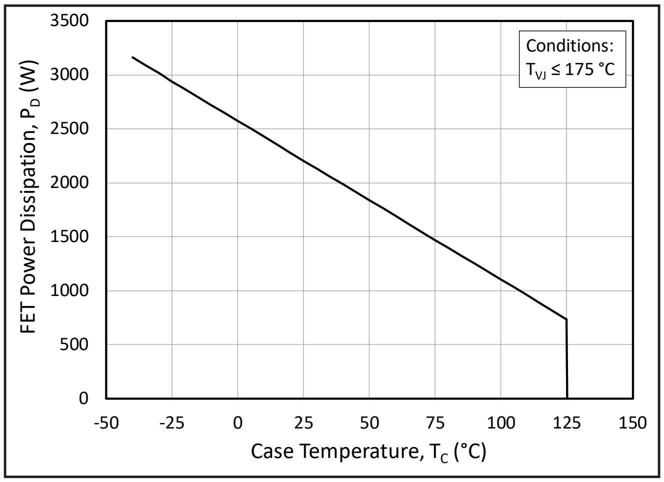


Figure 21. Maximum Power Dissipation Derating vs. Case Temperature

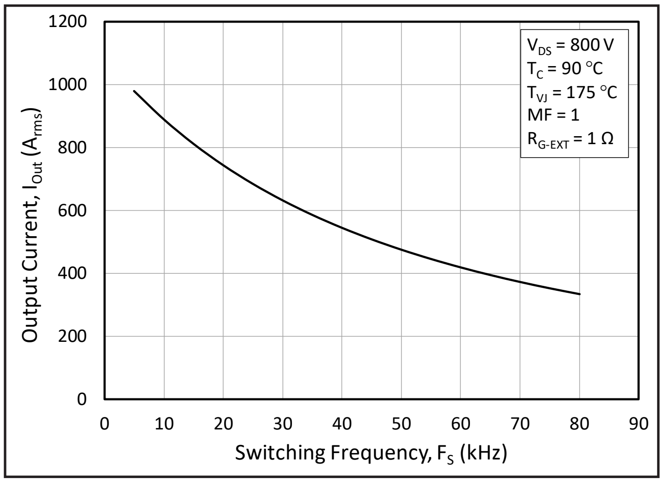


Figure 22. Typical Output Current Capability vs. Switching Frequency (Inverter Application)

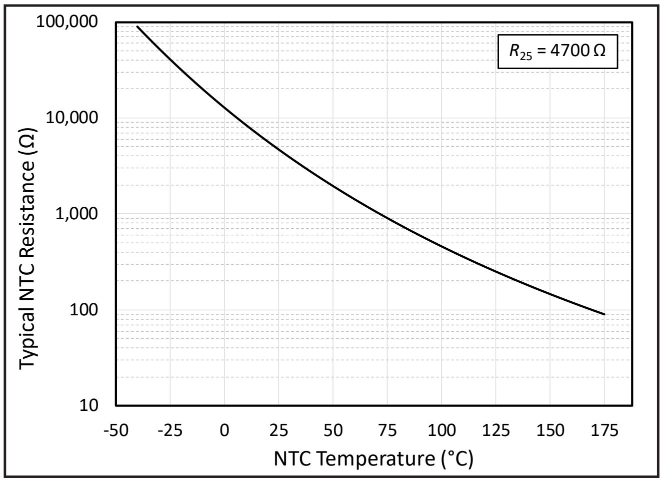


Figure 23. Typical NTC Resistance vs. Temperature

Timing Characteristics

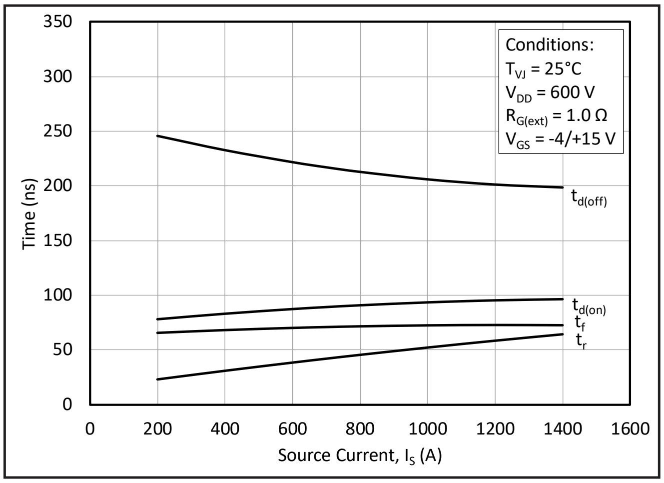


Figure 24. Timing vs. Source Current

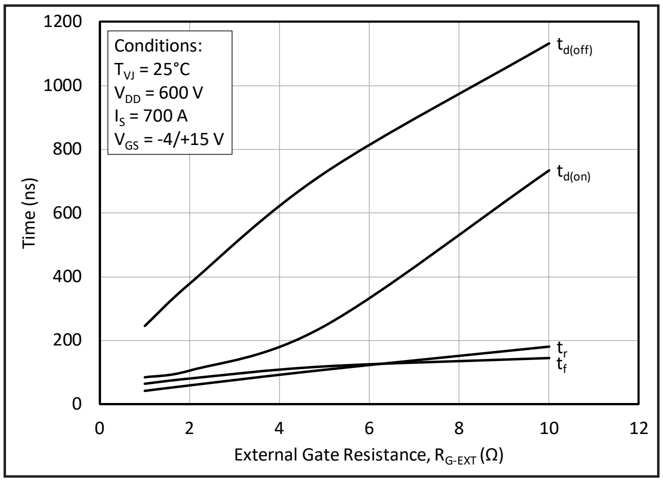


Figure 25. Timing vs. External Gate Resistance

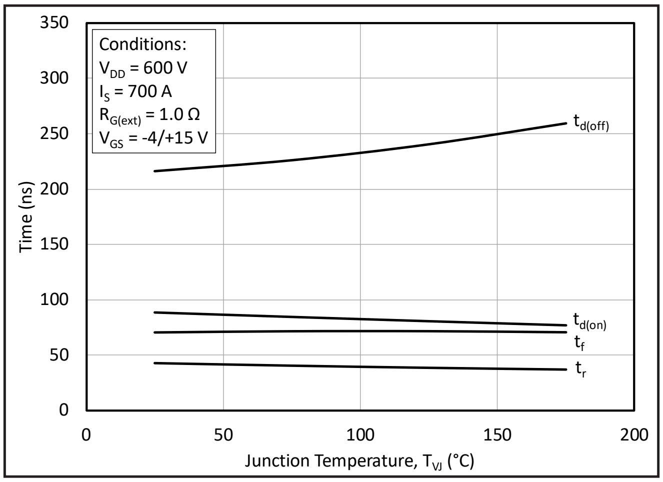


Figure 26. Timing vs. Junction Temperature

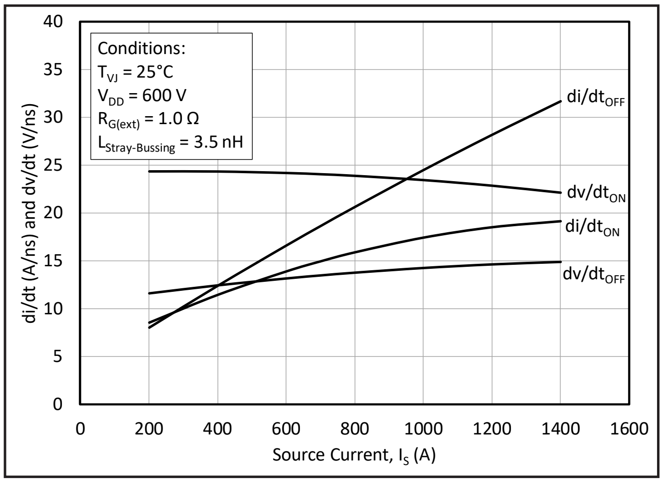


Figure 27. dv/dt and di/dt vs. Source Current

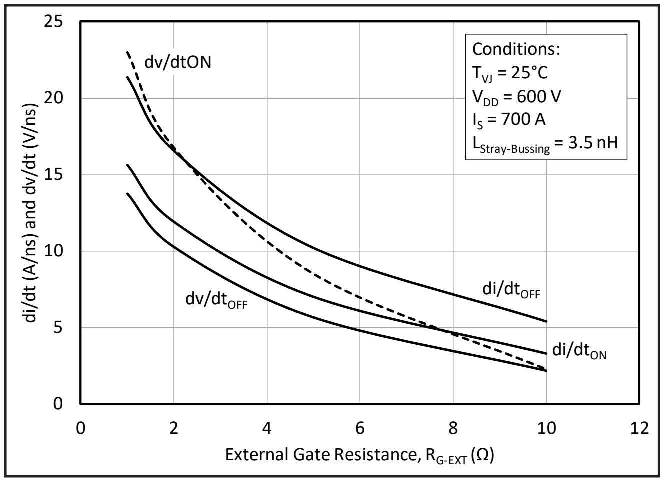


Figure 28. dv/dt and di/dt vs. External Gate Resistance

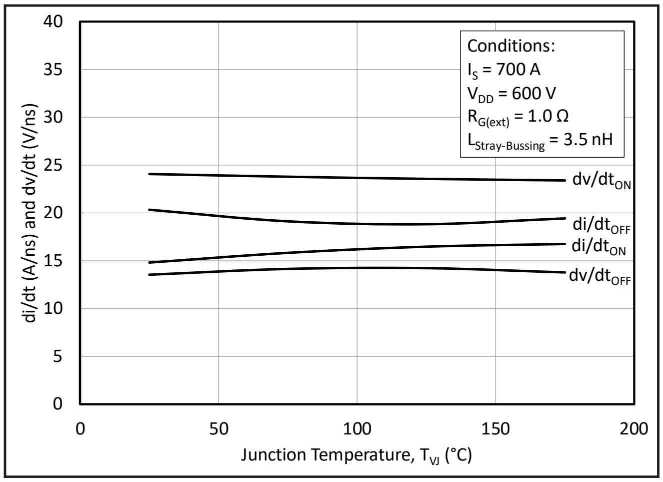


Figure 29. dv/dt and di/dt vs. Junction Temperature

Definitions

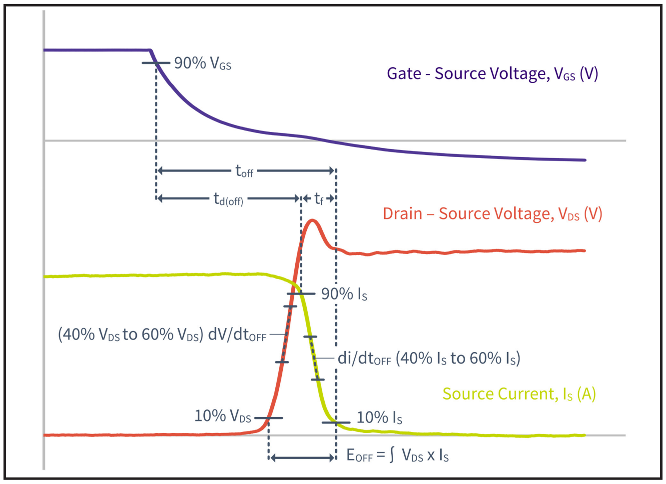


Figure 29. Turn-Off Transient Definitions

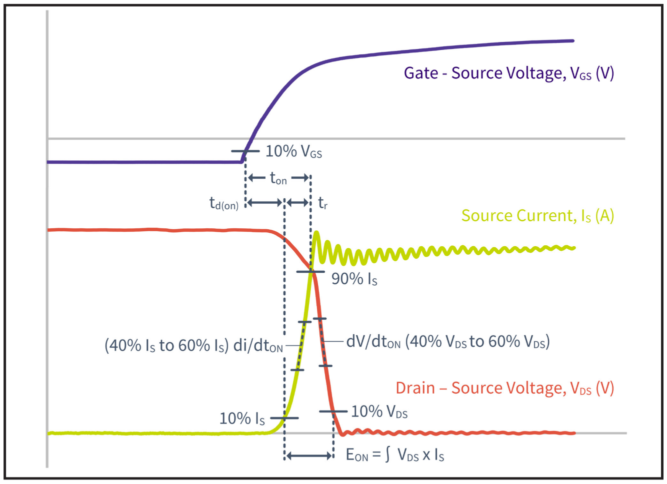


Figure 30. Turn-On Transient Definitions

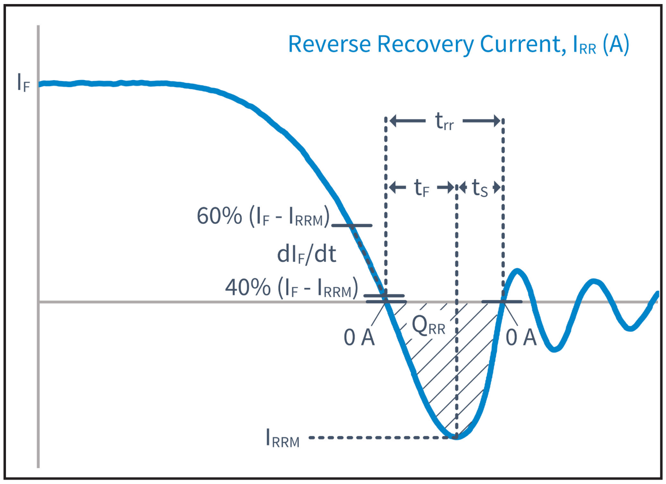


Figure 31. Reverse Recovery Definitions

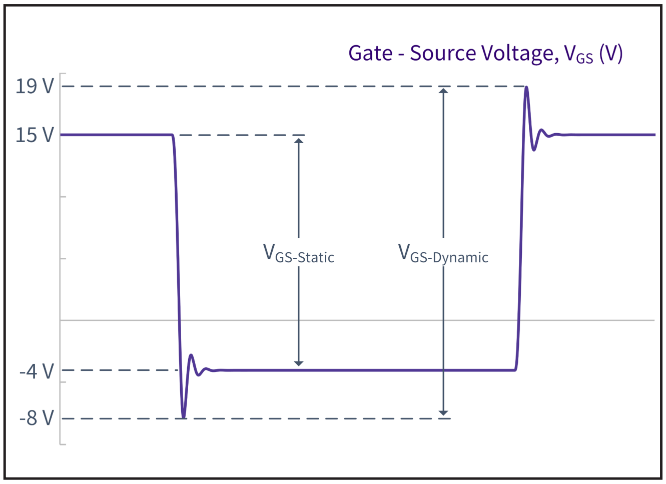
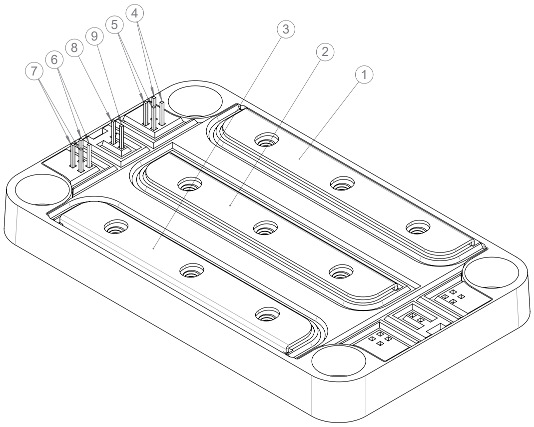
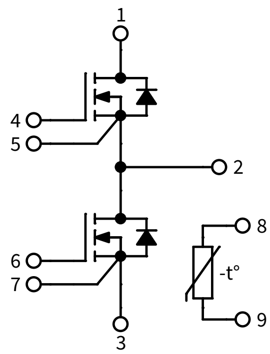


Figure 32. V_{GS} Transient Definitions

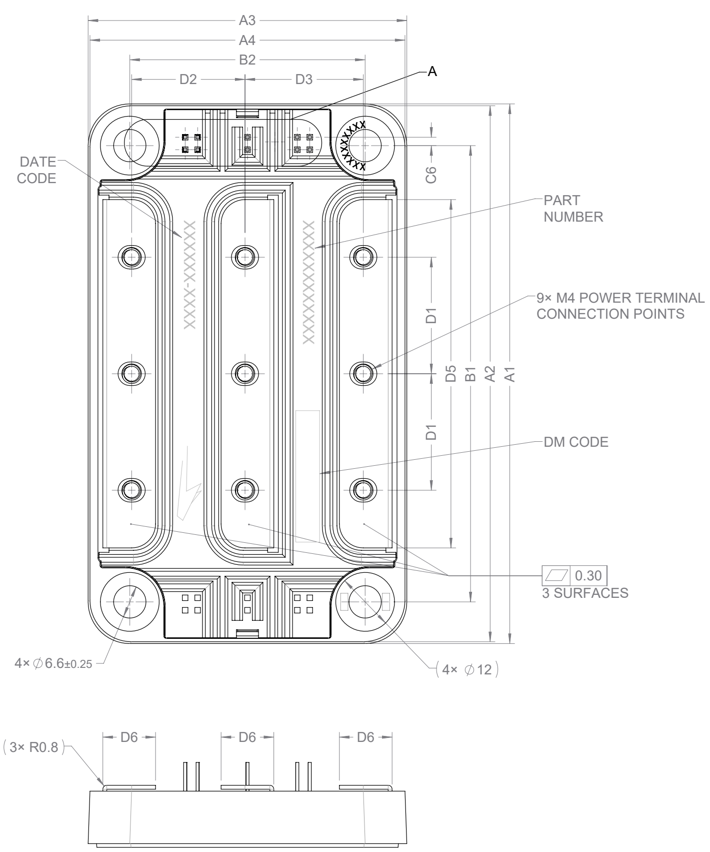
Schematic and Pin Out

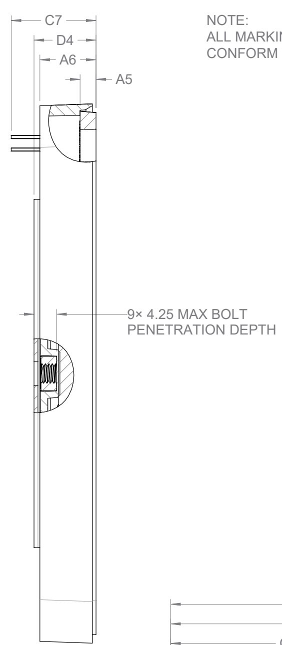


PIN OUT SCHEME	
PIN	LABEL
1	V+
2	Mid
3	V-
4	G1, Top row pins (2)
5	K1, Bottom row pins (2)
6	G2, Top row pins (2)
7	K2, Bottom row pins (2)
8	NTC1
9	NTC2



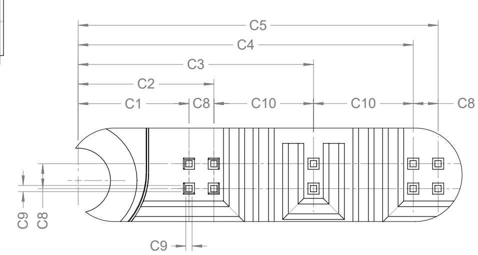
Package Dimensions (mm)





NOTE:
ALL MARKINGS SHALL CONFORM TO PRC-00786.

DIMENSION TABLE		
SYMBOL	DIMENSION	TOLERANCE
A1	110.00	±0.60
A2	109.25	±0.60
A3	65.00	±0.60
A4	64.25	±0.60
A5	3.25	±0.30
A6	11.45	±0.60
B1	93.00	±0.30
B2	48.00	±0.30
C1	11.30	±0.40
C2	13.84	±0.40
C3	24.00	±0.40
C4	34.16	±0.40
C5	36.70	±0.40
C6	1.71	±0.40
C7	17.30	±0.50
C8	2.54	±0.30
C9	0.64	±0.30
C10	10.16	±0.40
D1	23.75	±0.50
D2	23.13	±0.50
D3	24.13	±0.50
D4	12.20	±0.50
D5	71.00	±0.30
D6	10.75	±0.30



DETAIL A
SCALE: 4:1

Supporting Links & Tools

Evaluation Tools & Support

- PLECS Models
- LTSpice Models
- SpeedFit 2.0 Design Simulator™
- Technical Support Forum
- Dynamic Characterization Evaluation Tool for the High Performance 62mm (HM) Module Platform

Dual-Channel Gate Driver Board

- CGD1700HB3P-HM3: Wolfspeed Gate Driver Board
- CGD12HB00D: Differential Transceiver Daughter Board Companion Tool for Differential Gate Drivers

Application Notes

- CPWR-AN35: 62mm Thermal Interface Material Application Note
- CPWR-AN39: KIT-CRD-CIL12N-HM User Guide
- PRD-04814: Design Options for Wolfspeed® Silicon Carbide MOSFET Gate Bias Power Supplies

Notes & Disclaimer

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