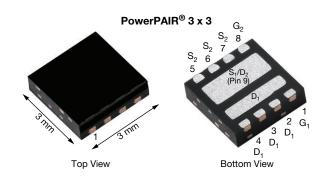


Vishay Siliconix

Dual N-Channel 30 V (D-S) MOSFET



PRODUCT SUMMARY MOSFET CHANNEL-1 AND CHANNEL-2					
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10 \text{ V}$	0.0094				
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5 \text{ V}$	0.0144				
Q _g typ. (nC)	3.7				
I _D (A)	33.4 ^a				
Configuration	Dual				

FEATURES





 High side and low side MOSFETs form optimized combination for 50 % duty cycle

RoHS COMPLIANT

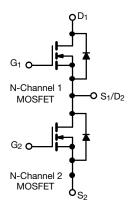
 • Optimized R_{DS} - Q_g and R_{DS} - Q_{gd} FOM elevates efficiency for high frequency switching

HALOGEN FREE

- 100 % R_a and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

APPLICATIONS

- Synchronous buck
- DC/DC conversion
- Half bridge
- POL



ORDERING INFORMATION	
Package	PowerPAIR 3 x 3
Lead (Pb)-free and halogen-free	SiZ342ADT-T1-GE3

ABSOLUTE MAXIMUM RATINGS $(T_A = 25 {}^{\circ}C$	C, unless other	wise noted)			
PARAMETER		CHANNEL-1 AND CHANNEL-2			
FARAINETER	SYMBOL	LIMIT	UNIT		
Drain-source voltage		V _{DS}	30	V	
Gate-source voltage		V _{GS}	+20 / -16		
	T _C = 25 °C		33.4		
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	T _C = 70 °C		26.7		
Continuous drain current (T _J = 150 °C)	T _A = 25 °C	I _D	15.7 b, c		
	T _A = 70 °C		12.5 b, c		
Pulsed drain current (t = 100 μs)		I _{DM}	100	A	
O " ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' '	T _C = 25 °C		13.9		
Continuous source current (MOSFET diode conduction)	T _A = 25 °C	I _S	3.1 b, c		
Single pulse avalanche current		I _{AS}	10		
Single pulse avalanche energy	L = 0.1 mH	E _{AS}	5	mJ	
	T _C = 25 °C		16.7		
Marchan and Parkarthan	T _C = 70 °C	_	10.7	14/	
Maximum power dissipation	T _A = 25 °C	P _D	3.7 b, c	w	
	T _A = 70 °C		2.4 b, c		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	0.0	
Soldering recommendations (peak temperature)	Ŭ .	260	→ °C		

Notes

a. $T_C = 25 \,^{\circ}C$

b. Surface mounted on 1" x 1" FR4 board

c. t = 10 s



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THERMAL RESISTANCE RATINGS					
PARAMETER			CHANNEL-1 AN	ID CHANNEL-2	
PARAMETER	AKAMETEK		TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient a, b	t ≤ 10 s	R _{thJA}	27	34	°C/W
Maximum junction-to-case (drain)	Steady state	R _{thJC}	6	7.5	G/ VV

Notes

- a. Surface mounted on 1" x 1" FR4 board
- b. Maximum under steady state conditions is 69 °C/W

SPECIFICATIONS (T _J = 25 °C	, ariioso otric	CHANNEL-1 AND CHANNEL-2						
PARAMETER	SYMBOL							
Static								
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30	-	-	V		
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1	-	2.4	V		
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = +20 \text{ V} / -16 \text{ V}$	-	-	± 100	nA		
Zero gate voltage drain current	I _{DSS}	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	μA		
	200	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 \text{ °C}$	-	-	5			
On-state drain current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30	-	-	Α		
Drain-source on-state resistance a	R _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	-	0.0078	.0078 0.0094			
Brain source on state resistance	T DS(on)	$V_{GS} = 4.5 \text{ V}, I_D = 7 \text{ A}$	1	0.0120	0.0144	Ω		
Forward transconductance ^a	9 _{fs}	$V_{DS} = 10 \text{ V}, I_D = 10 \text{ A}$	1	57	-	S		
Dynamic ^b								
Input capacitance	C _{iss}		-	580	-]		
Output capacitance	C _{oss}	\ 15\\\\ 0\\ f 1MI-	-	250	-	pF		
Reverse transfer capacitance	C _{rss}	$V_{DS} = 15 \text{ V. } V_{CS} = 0 \text{ V. } t = 1 \text{ MHz}$		30	-			
C _{rss} /C _{iss} ratio			=	0.052	0.103			
Total gate charge	0	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 15.7 \text{ A}$	-	8.1	12.2	nC		
Total gate charge	Q_g		ı	3.7	4.5			
Gate-source charge	Q_{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 15.7 \text{ A}$	-	2.4	-	110		
Gate-drain charge	Q _{gd}		-	0.67	-			
Gate resistance	R _g	f = 1 MHz	0.24	1.2	2.4	Ω		
Turn-on delay time	t _{d(on)}		-	10	20			
Rise time	t _r	$V_{DD} = 15 \text{ V}, R_L = 1.2 \Omega, I_D \cong 12.5 \text{ A},$	-	6	12			
Turn-off delay time	t _{d(off)}	$V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	18	36	1		
Fall time	t _f		-	8	16			
Turn-on delay time	t _{d(on)}		-	15	30	ns		
Rise time	t _r	$V_{DD} = 15 \text{ V}, R_L = 1.2 \Omega, I_D \cong 12.5 \text{ A},$	-	180	360			
Turn-off delay time	t _{d(off)}	$V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$	-	20	40			
Fall time	t _f	1	-	15	30			



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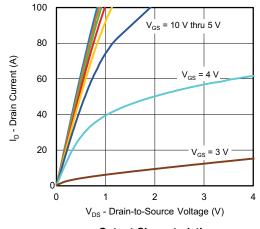
SPECIFICATIONS (T _J = 25 °C, t	unless othe	rwise noted)					
PARAMETER	CHANNEL-1 AND CHANNEL-2						
PANAMETER	SYMBOL TEST CONDITIONS			TYP.	MAX.	UNIT	
Drain-source Body Diode Characteristi	cs						
Continuous source-drain diode current	I _S	T _C = 25°C	-	-	13.9	۸	
Pulse diode forward current	I _{SM}		-	-	100	Α	
Body diode voltage	V_{SD}	$I_S = 12.5 \text{ A}, V_{GS} = 0 \text{ V}$	-	0.85	1.2	V	
Body diode reverse recovery time	t _{rr}		-	15	30	ns	
Body diode reverse recovery charge	Q_{rr}	I _F = 12.5 A, di/dt = 100 A/μs,	-	4.3	8.6	nC	
Reverse recovery fall time	ta	T _J = 25 °C	=	8	-	no	
Reverse recovery rise time	t _b		=	7	-	ns	

Notes

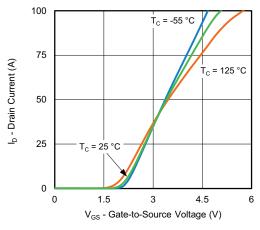
- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

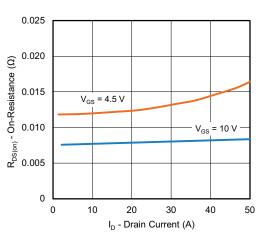




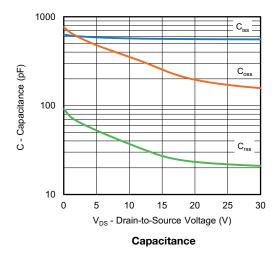
Output Characteristics

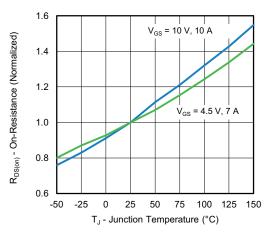


Transfer Characteristics

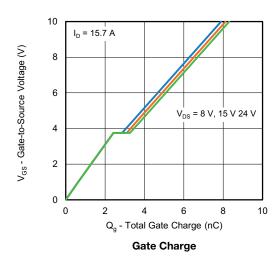


On-Resistance vs. Drain Current and Gate

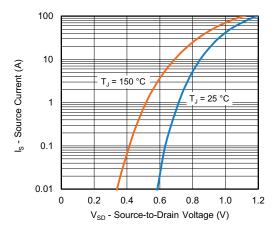




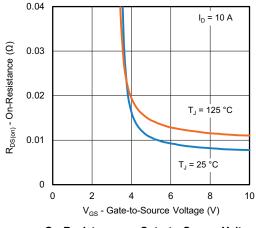
On-Resistance vs. Junction Temperature



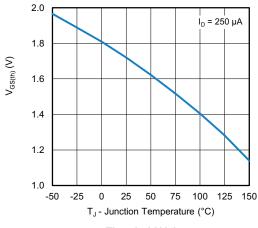




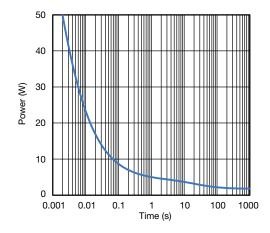
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

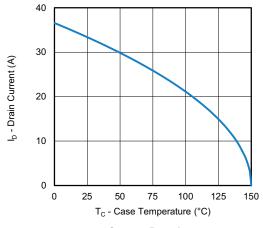


Threshold Voltage

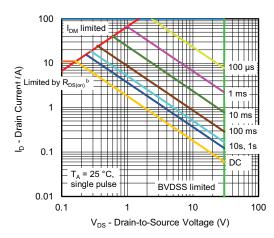


Single Pulse Power

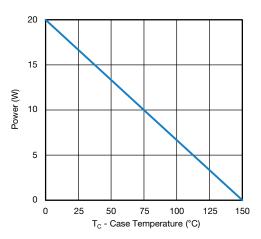




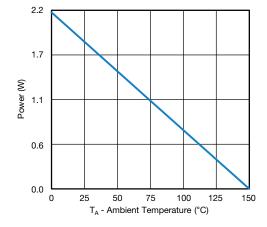
Current Derating ^a



Safe Operating Area, Junction-to-Ambient



Power, Junction-to-Case

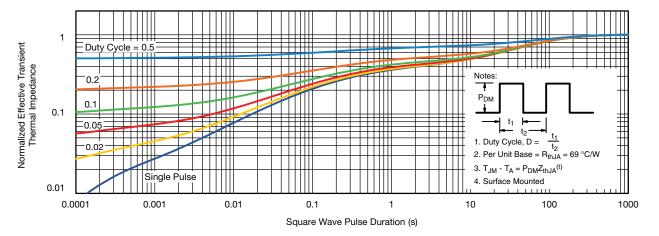


Power, Junction-to-Ambient

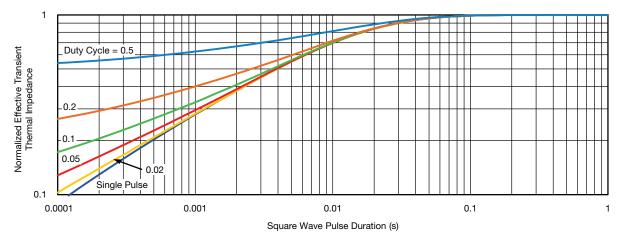
Notes

- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-ambient thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit
- b. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified





Normalized Thermal Transient Impedance, Junction-to-Ambient

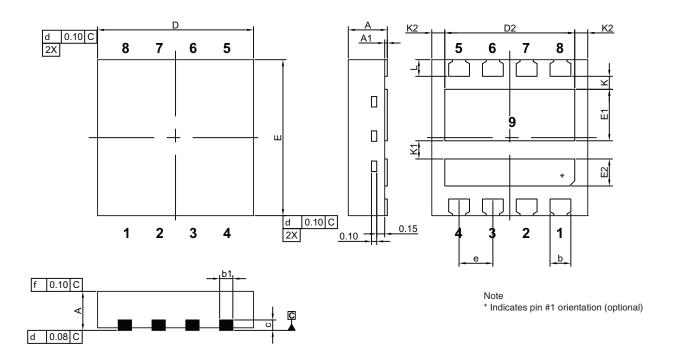


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?76711.



PowerPAIR® 3 x 3 Case Outline



		MILLIMETERS		INCHES			
DIM. MIN.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
Α	0.70	0.75	0.80	0.028	0.030	0.031	
A1	0.00		0.05	0.000		0.002	
b	0.35	0.40	0.45	0.014	0.016	0.018	
b1	0.20	0.25	0.38	0.008	0.010	0.015	
С	0.18	0.20	0.23	0.007	0.008	0.009	
D	2.90	3.00	3.10	0.114	0.118	0.122	
D2	2.35	2.40	2.45	0.093	0.094	0.096	
E	2.90	3.00	3.10	0.114	0.118	0.122	
E1	0.94	0.99	1.04	0.037	0.039	0.041	
E2	0.47	0.52	0.57	0.019	0.020	0.022	
е	0.65 BSC			0.026 BSC			
K	0.25 typ.				0.010 typ.		
K1	0.35 typ.				0.014 typ.		
K2	0.30 typ.				0.012 typ.		
L	0.27	0.32	0.37	0.011	0.013	0.015	

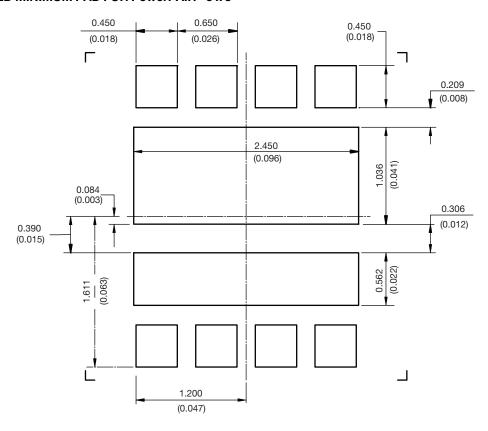
ECIN. 112-0347-nev. C, 10-Juli-12

DWG: 5998



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RECOMMENDED MINIMUM PAD FOR PowerPAIR® 3 x 3



Recommended PAD for PowerPAIR 3 x 3

Dimensions in millimeters (inches)

Keep-Out 3.5 mm x 3.5 mm for non terminating traces



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