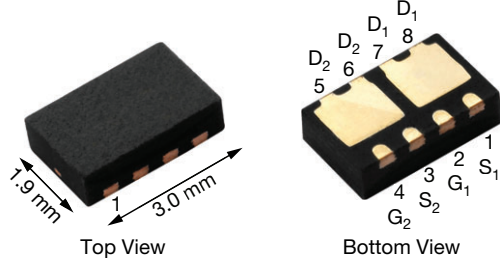


Dual N-Channel 30 V (D-S) MOSFET

PowerPAK® ChipFET® Dual



Marking code: CH

| PRODUCT SUMMARY | |
|--|--------|
| V_{DS} (V) | 30 |
| $R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V | 0.0192 |
| $R_{DS(on)}$ max. (Ω) at $V_{GS} = 6$ V | 0.0220 |
| $R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V | 0.0245 |
| Q_g typ. (nC) | 4.7 |
| I_D (A) ^a | 6 |
| Configuration | Dual |

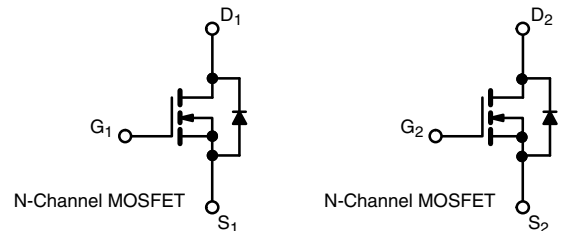
FEATURES

- TrenchFET® power MOSFET
- 100 % R_g and UIS tested
- New thermally enhanced PowerPAK® ChipFET® package
 - Small footprint area
 - Low on-resistance
 - Thin 0.8 mm profile
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
 COMPLIANT
 HALOGEN
FREE

APPLICATIONS

- DC/DC power supply



| ORDERING INFORMATION | |
|---------------------------------|------------------|
| Package | PowerPAK ChipFET |
| Lead (Pb)-free and halogen-free | Si5922DU-T1-GE3 |

| ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted) | | | |
|---|----------------|---------------|----------------------|
| PARAMETER | SYMBOL | LIMIT | UNIT |
| Drain-source voltage | V_{DS} | 30 | V |
| Gate-source voltage | V_{GS} | +20 / -16 | V |
| Continuous drain current ($T_J = 150$ °C) | I_D | $T_C = 25$ °C | 6 ^a |
| | | $T_C = 70$ °C | 6 ^a |
| | | $T_A = 25$ °C | 6 ^{a, b, c} |
| | | $T_A = 70$ °C | 6 ^{a, b, c} |
| Pulsed drain current ($t = 100$ μ s) | I_{DM} | 24 | A |
| Continuous source-drain diode current | I_S | $T_C = 25$ °C | 6 ^a |
| | | $T_A = 25$ °C | 1.9 ^{b, c} |
| Single pulse avalanche current | I_{AS} | 10 | mJ |
| Avalanche energy | E_{AS} | 5 | |
| Maximum power dissipation | P_D | $T_C = 25$ °C | 10.4 |
| | | $T_C = 70$ °C | 6.7 |
| | | $T_A = 25$ °C | 2.3 ^{b, c} |
| | | $T_A = 70$ °C | 1.5 ^{b, c} |
| Operating junction and storage temperature range | T_J, T_{stg} | -55 to +150 | °C |
| Soldering recommendations (peak temperature) ^{d, e} | | 260 | |

Notes

- Package limited
- Surface mounted on 1" x 1" FR4 board
- $t = 5$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



| THERMAL RESISTANCE RATINGS | | | | | |
|---|--------------|------------|---------|---------|------|
| PARAMETER | | SYMBOL | TYPICAL | MAXIMUM | UNIT |
| Maximum junction-to-ambient ^{a, b} | $t \leq 5$ s | R_{thJA} | 43 | 55 | °C/W |
| Maximum junction-to-case (drain) | Steady state | R_{thJC} | 9.5 | 12 | |

Notes

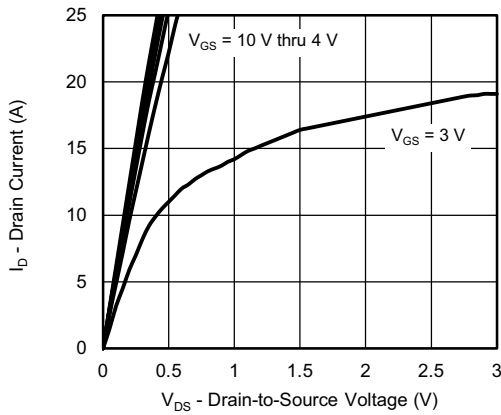
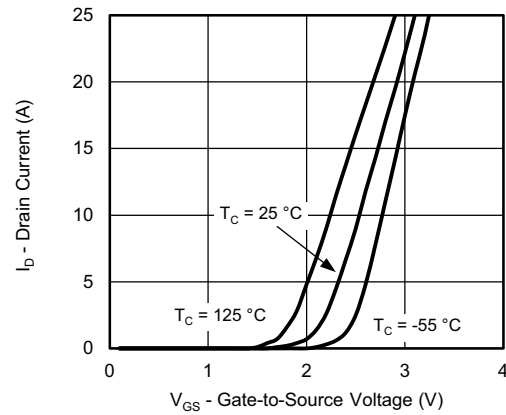
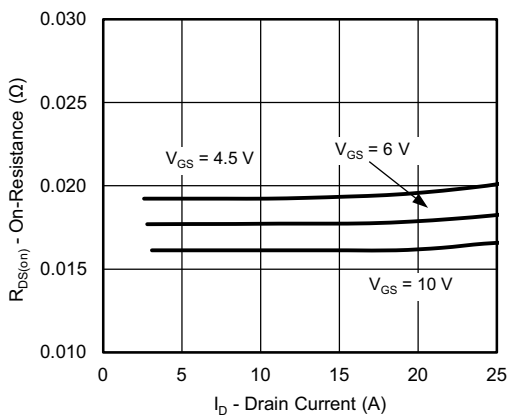
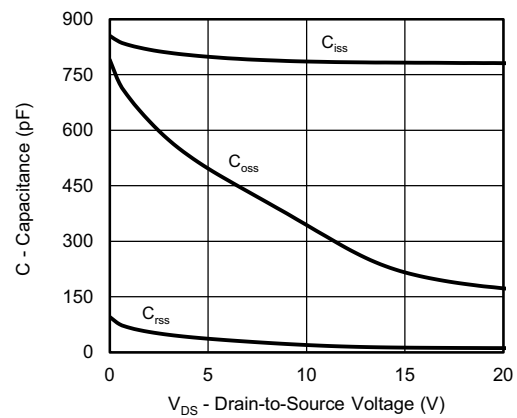
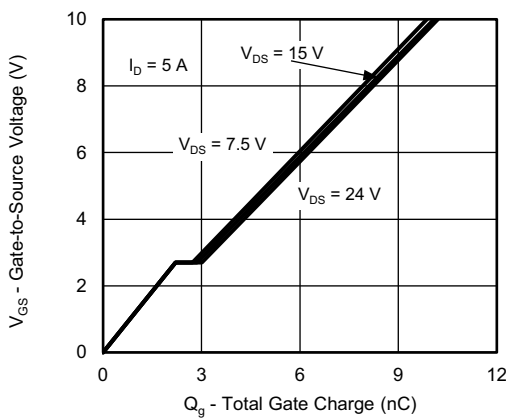
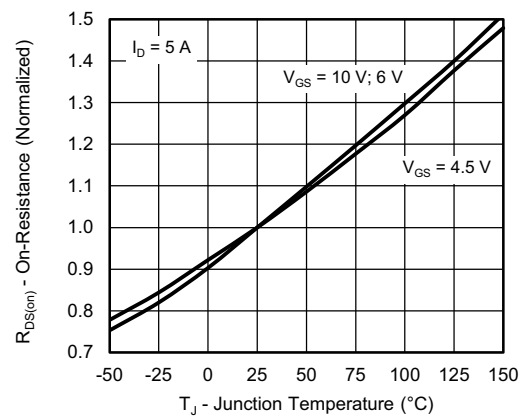
- a. Surface mounted on 1" x 1" FR4 board
- b. Maximum under steady state conditions is 105 °C/W

| SPECIFICATIONS ($T_J = 25$ °C, unless otherwise noted) | | | | | | |
|---|-------------------------|---|------|--------|-----------|----------|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | |
| Drain-source breakdown voltage | V_{DS} | $V_{GS} = 0$ V, $I_D = 250$ μ A | 30 | - | - | V |
| V_{DS} temperature coefficient | $\Delta V_{DS}/T_J$ | $I_D = 250$ μ A | - | 14.3 | - | mV/°C |
| $V_{GS(th)}$ temperature coefficient | $\Delta V_{GS(th)}/T_J$ | | - | -4.7 | - | |
| Gate-source threshold voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D = 250$ μ A | 1.2 | - | 2.2 | V |
| Gate-source leakage | I_{GSS} | $V_{DS} = 0$ V, $V_{GS} = +20$ V / -16 V | - | - | ± 100 | nA |
| Zero gate voltage drain current | I_{DSS} | $V_{DS} = 30$ V, $V_{GS} = 0$ V. | - | - | 1 | μ A |
| | | $V_{DS} = 30$ V, $V_{GS} = 0$ V, $T_J = 55$ °C | - | - | 10 | |
| On-state drain current ^a | $I_{D(on)}$ | $V_{DS} \geq 5$ V, $V_{GS} = 10$ V | 5 | - | - | A |
| Drain-source on-state resistance ^a | $R_{DS(on)}$ | $V_{GS} = 10$ V, $I_D = 5$ A | - | 0.0155 | 0.0192 | Ω |
| | | $V_{GS} = 6$ V, $I_D = 4$ A | - | 0.0170 | 0.0220 | |
| | | $V_{GS} = 4.5$ V, $I_D = 4$ A | - | 0.0190 | 0.0245 | |
| Forward transconductance ^a | g_{fs} | $V_{DS} = 10$ V, $I_D = 5$ A | - | 22 | - | S |
| Dynamic ^b | | | | | | |
| Input capacitance | C_{iss} | $V_{DS} = 15$ V, $V_{GS} = 0$ V, $f = 1$ MHz | - | 765 | - | pF |
| Output capacitance | C_{oss} | | - | 225 | - | |
| Reverse transfer capacitance | C_{rss} | | - | 14 | - | |
| C_{rss}/C_{iss} ratio | | | - | 0.018 | 0.036 | - |
| Total gate charge | Q_g | $V_{DS} = 15$ V, $V_{GS} = 10$ V, $I_D = 5$ A | - | 10 | 15 | nC |
| | | $V_{DS} = 15$ V, $V_{GS} = 4.5$ V, $I_D = 5$ A | - | 4.7 | 7.1 | |
| Gate-source charge | Q_{gs} | | - | 2.2 | - | |
| Gate-drain charge | Q_{gd} | | - | 0.65 | - | |
| Output charge | Q_{oss} | $V_{DS} = 15$ V, $V_{GS} = 0$ V | - | 6.5 | - | |
| Gate resistance | R_g | $f = 1$ MHz | 1.3 | 6.3 | 12.6 | Ω |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD} = 15$ V, $R_L = 3$ Ω , $I_D \cong 5$ A, $V_{GEN} = 10$ V, $R_g = 1$ Ω | - | 6 | 15 | ns |
| Rise time | t_r | | - | 25 | 50 | |
| Turn-off delay time | $t_{d(off)}$ | | - | 15 | 30 | |
| Fall time | t_f | | - | 10 | 20 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD} = 15$ V, $R_L = 3$ Ω , $I_D \cong 5$ A, $V_{GEN} = 4.5$ V, $R_g = 1$ Ω | - | 17 | 35 | |
| Rise time | t_r | | - | 45 | 90 | |
| Turn-off delay time | $t_{d(off)}$ | | - | 16 | 30 | |
| Fall time | t_f | | - | 27 | 50 | |
| Drain-Source Body Diode Characteristics | | | | | | |
| Continuous source-drain diode current | I_S | $T_C = 25$ °C | - | - | 6 | A |
| Pulse diode forward current ($t = 100$ μ s) | I_{SM} | | - | - | 24 | |
| Body diode voltage | V_{SD} | $I_S = 5$ A, $V_{GS} = 0$ V | - | 0.81 | 1.2 | V |
| Body diode reverse recovery time | t_{rr} | $I_F = 5$ A, $di/dt = 100$ A/ μ s, $T_J = 25$ °C | - | 21 | 40 | ns |
| Body diode reverse recovery charge | Q_{rr} | | - | 10 | 20 | nC |
| Reverse recovery fall time | t_a | | - | 12 | - | ns |
| Reverse recovery rise time | t_b | | - | 9 | - | |

Notes

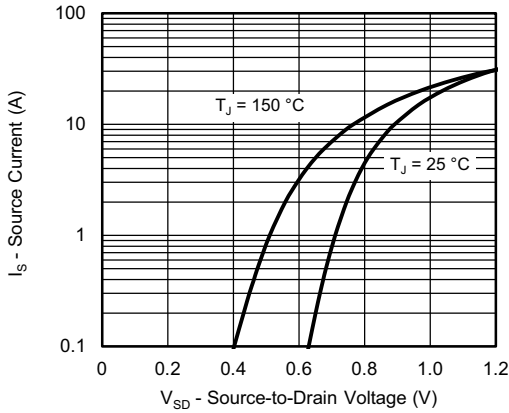
- a. Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

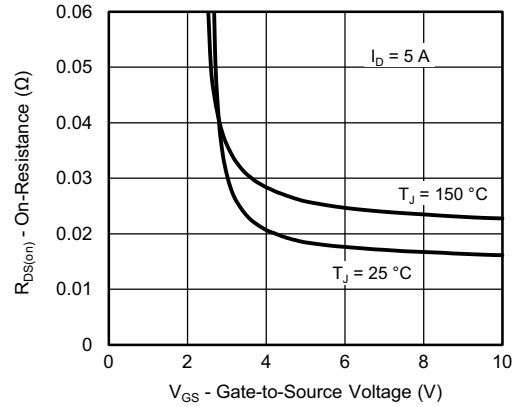
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature



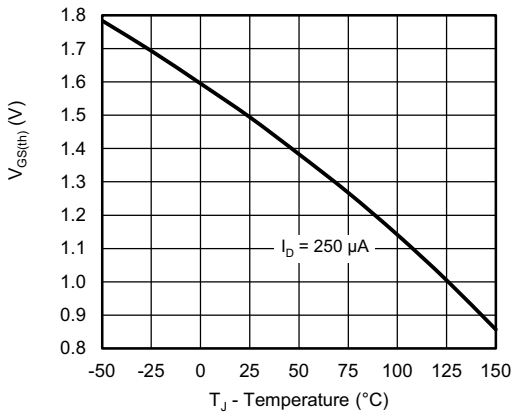
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



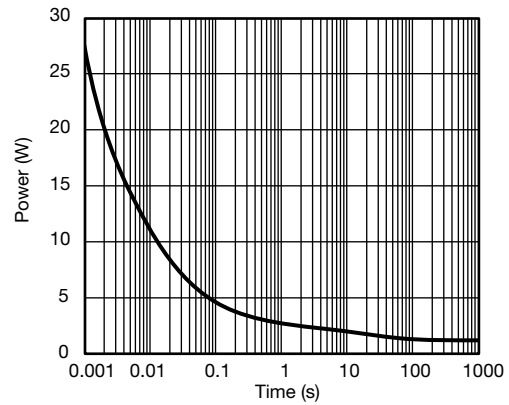
Source-Drain Diode Forward Voltage



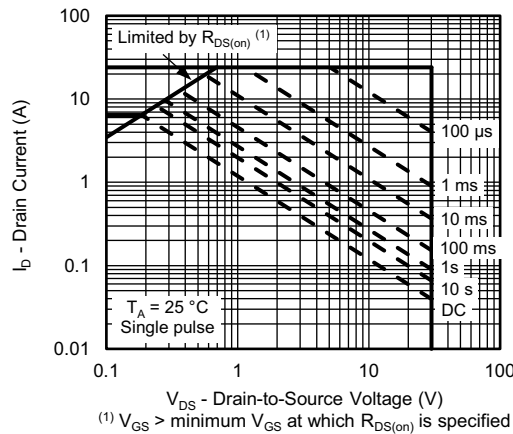
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



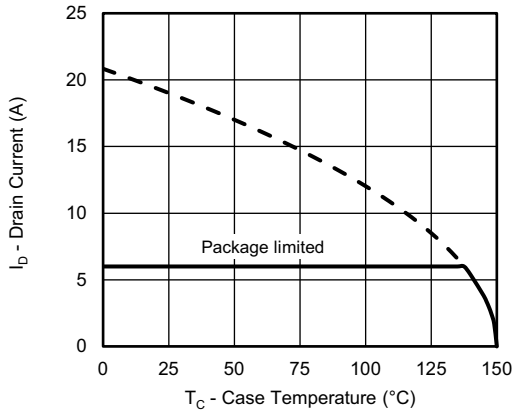
Single Pulse Power, Junction-to-Ambient



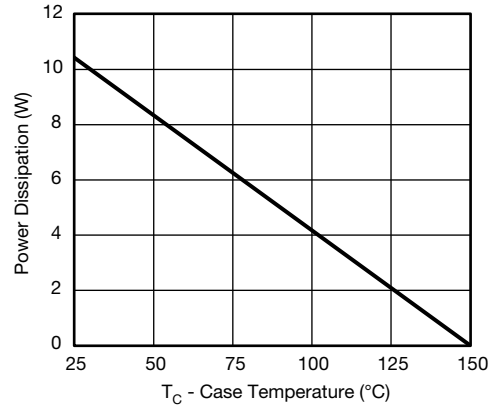
Safe Operating Area



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



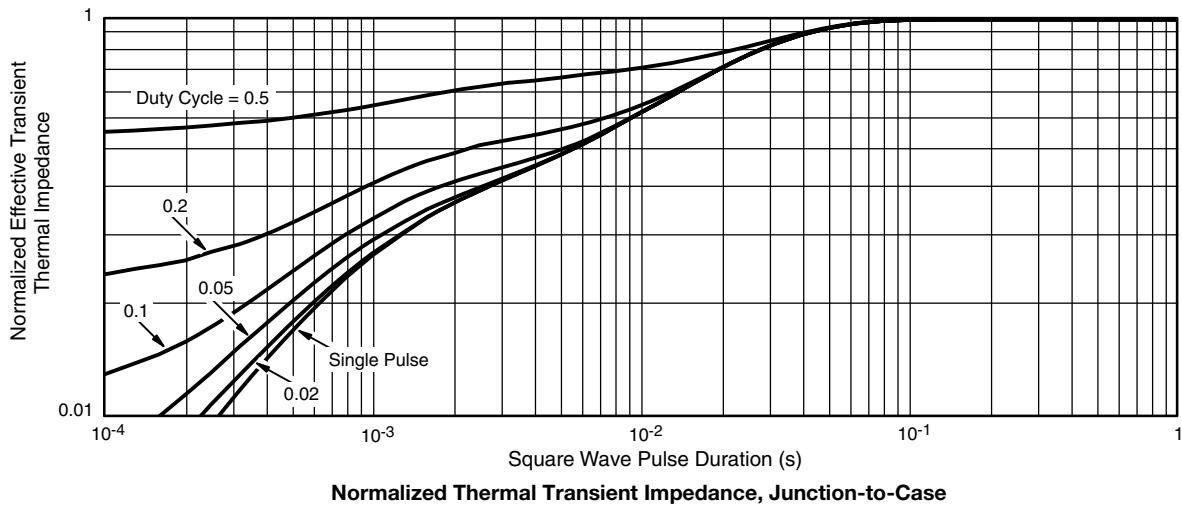
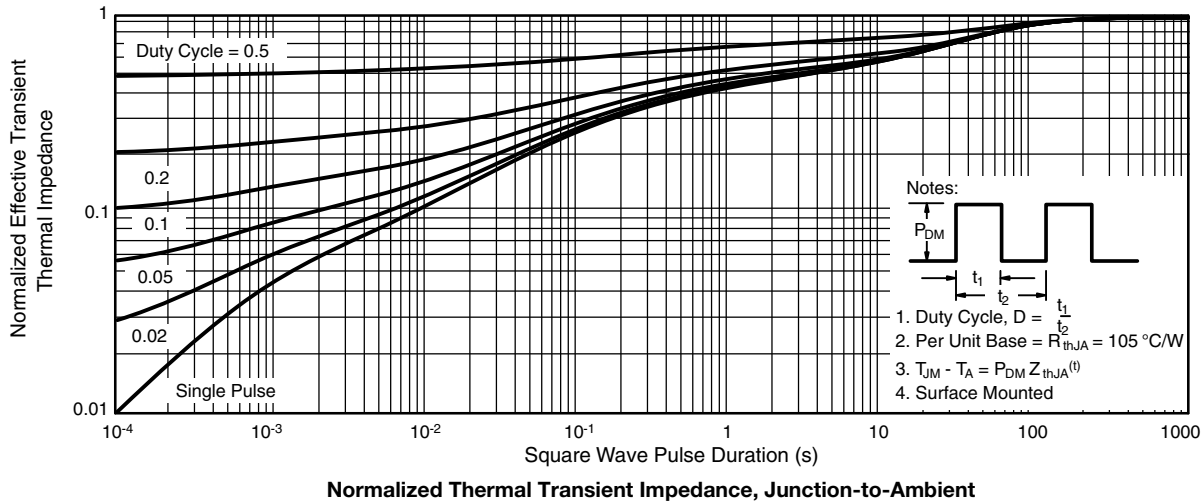
Power Derating

Note

- a. The power dissipation P_D is based on T_J (max.) = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?76056.

PowerPAK[®] ChipFET[®] Case Outline

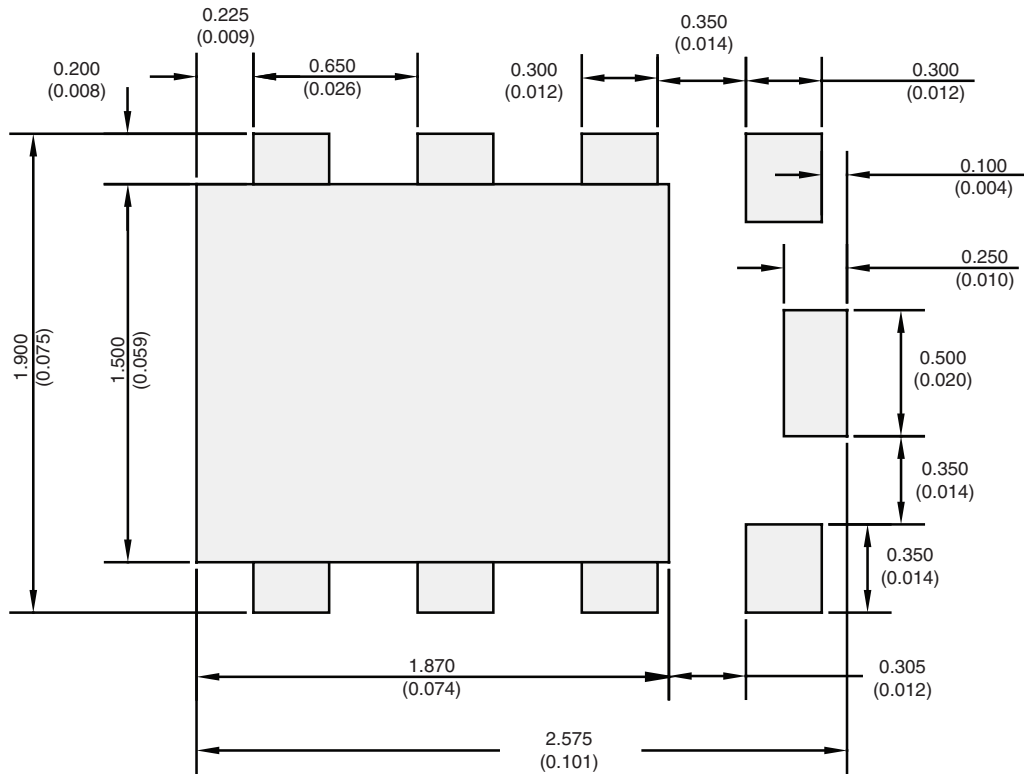


| DIM. | MILLIMETERS | | | INCHES | | |
|----------------------------|-------------|------|------|-----------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.85 | 0.028 | 0.030 | 0.033 |
| A1 | 0 | - | 0.05 | 0 | - | 0.002 |
| b | 0.25 | 0.30 | 0.35 | 0.010 | 0.012 | 0.014 |
| C | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| D | 2.92 | 3.00 | 3.08 | 0.115 | 0.118 | 0.121 |
| D1 | 1.75 | 1.87 | 2.00 | 0.069 | 0.074 | 0.079 |
| D2 | 1.07 | 1.20 | 1.32 | 0.042 | 0.047 | 0.052 |
| D3 | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| E | 1.82 | 1.90 | 1.98 | 0.072 | 0.075 | 0.078 |
| E1 | 1.38 | 1.50 | 1.63 | 0.054 | 0.059 | 0.064 |
| E2 | 0.92 | 1.05 | 1.17 | 0.036 | 0.041 | 0.046 |
| E3 | 0.45 | 0.50 | 0.55 | 0.018 | 0.020 | 0.022 |
| e | 0.65 BSC | | | 0.026 BSC | | |
| H | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| K | 0.25 | - | - | 0.010 | - | - |
| K1 | 0.30 | - | - | 0.012 | - | - |
| K2 | 0.20 | - | - | 0.008 | - | - |
| K3 | 0.20 | - | - | 0.008 | - | - |
| L | 0.30 | 0.35 | 0.40 | 0.012 | 0.014 | 0.016 |
| C14-0630-Rev. E, 21-Jul-14 | | | | | | |
| DWG: 5940 | | | | | | |

Note

- Millimeters will govern

RECOMMENDED MINIMUM PADS FOR PowerPAK® ChipFET® Single



Recommended Minimum Pads
Dimensions in mm/(Inches)

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